Upgrade of the ALICE Inner Tracking System

L. Musa - CERN

FCC-ee mini-workshop on Detector Requirements
CERN, 17 June, 2015

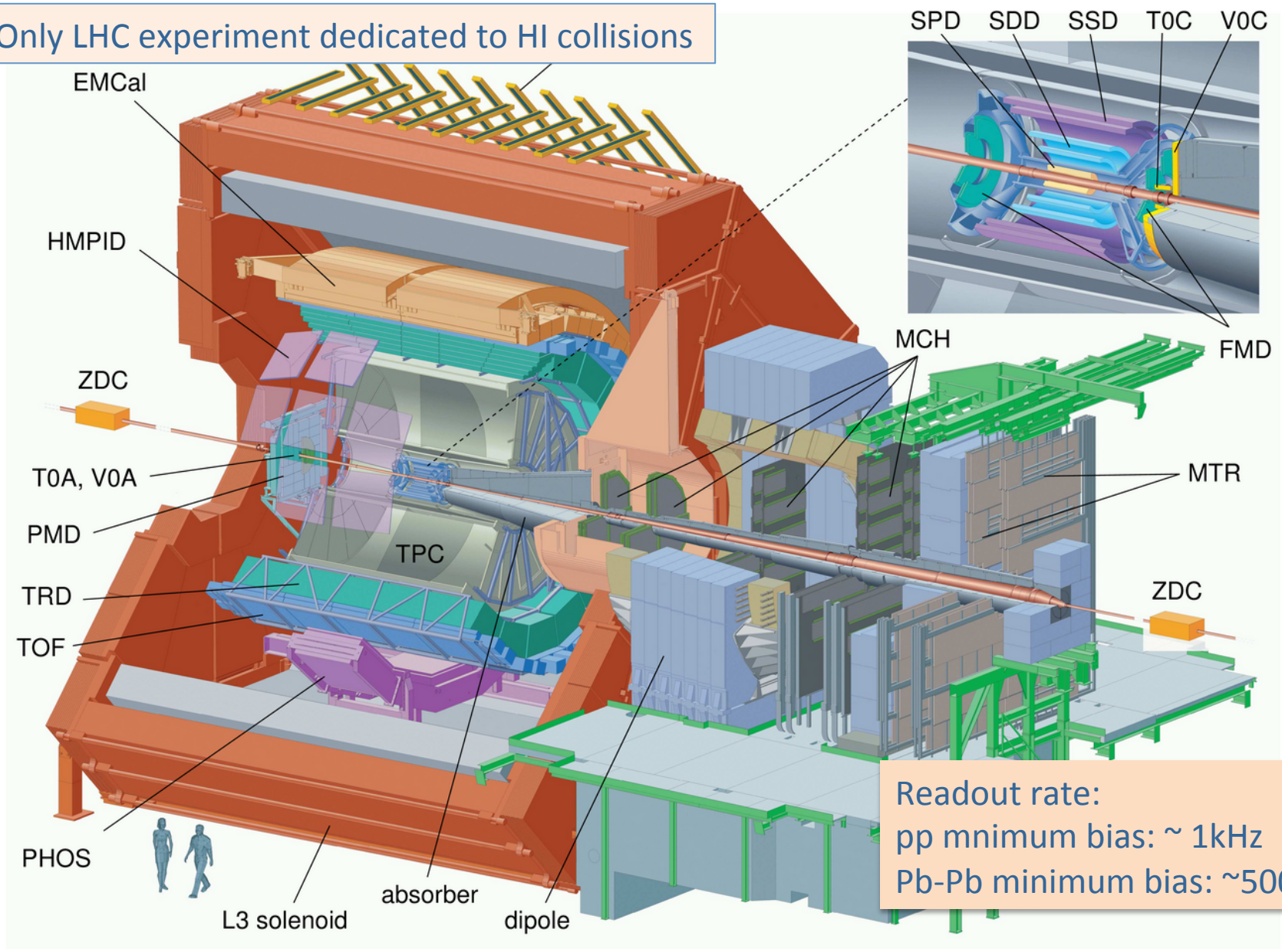
Upgrade of the ALICE Inner Tracking System

OUTLINE

- ALICE current set-up and Inner Tracking System
- ITS upgrade motivations and design objectives
- ITS upgrade layout and main components
- Detector simulated performance

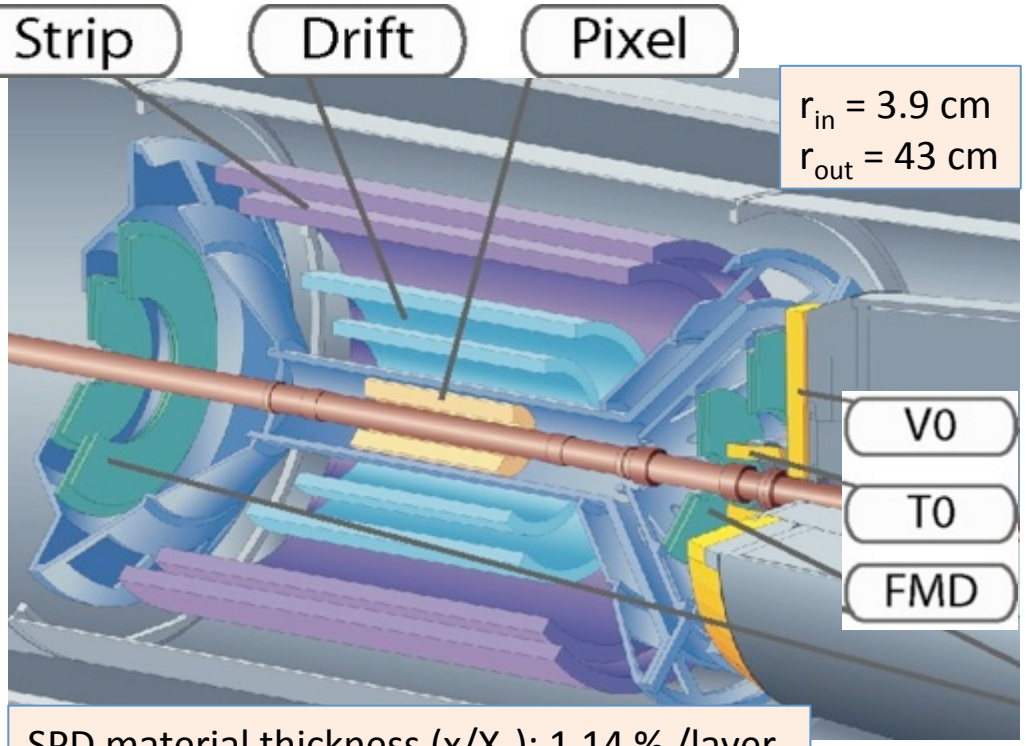
The Current ALICE Detector

Only LHC experiment dedicated to HI collisions

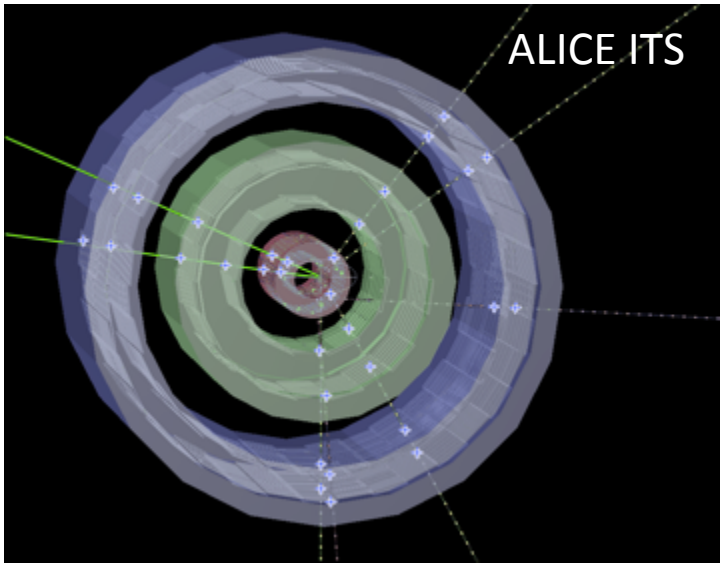


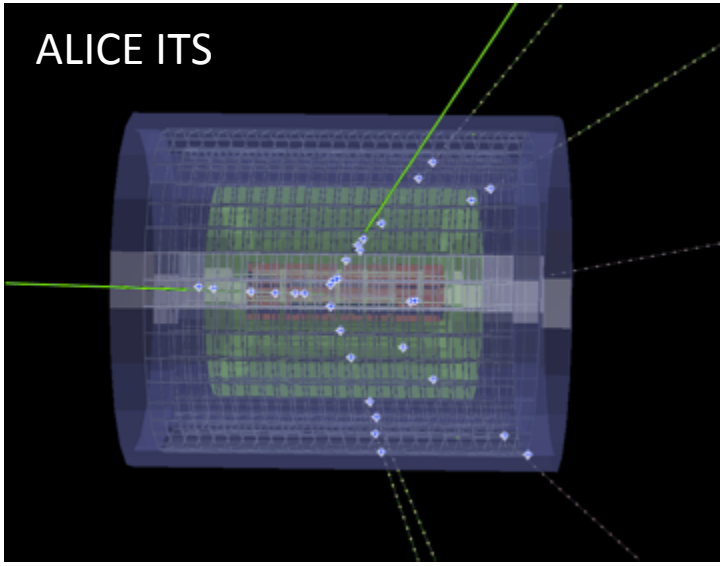
Readout rate:
pp mnimum bias: ~ 1kHz
Pb-Pb minimum bias: ~500 Hz

The Current ALICE Inner Tracking System



SPD material thickness (x/X_0): 1.14 % /layer





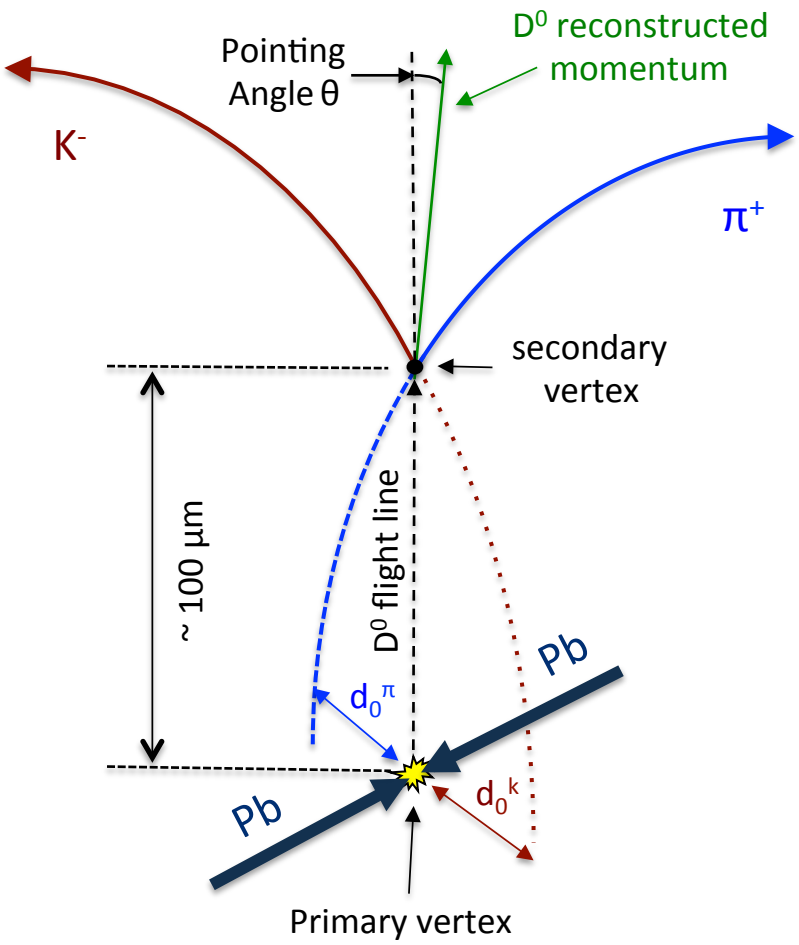
Current ITS

6 concentric barrels, 3 different technologies

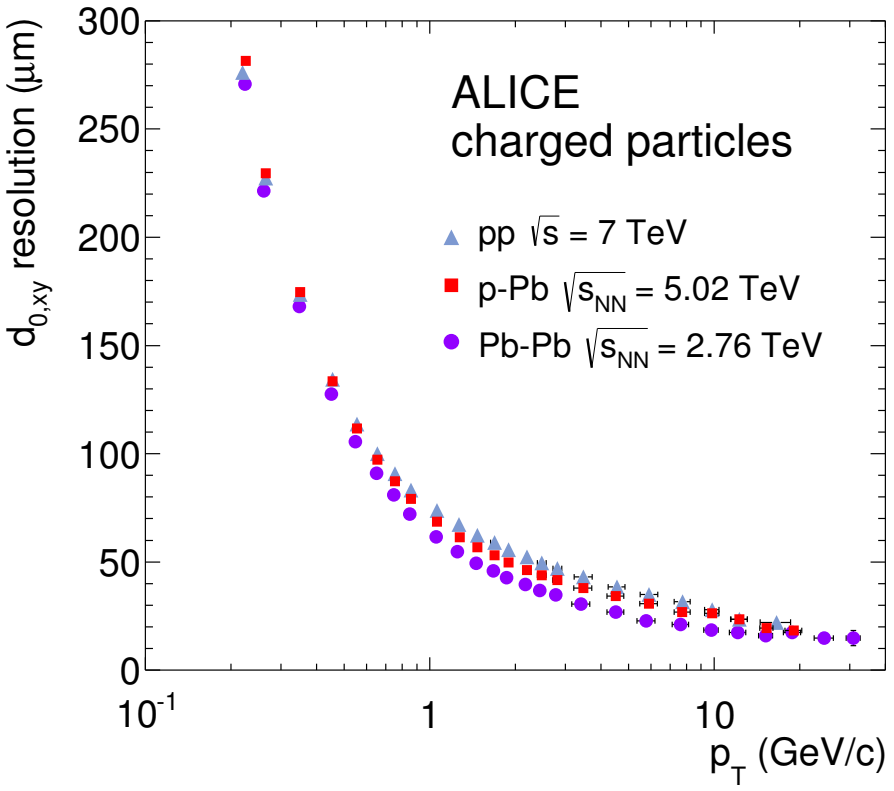
- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

ITS – Secondary vertex determination

Example: D^0 meson



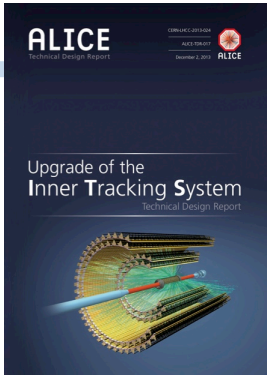
Very weak dependence on the colliding system



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

Analysis based on decay topology and invariant mass technique

ITS upgrade design objectives



CERN-LHCC-2013-24

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm ➡ 23mm
- Reduce x/X_0 /layer: ~1.14% ➡ ~ 0.3% (for inner layers)
- Reduce pixel size: currently 50μm x 425μm ➡ O(30μm x 30μm)

J. Phys. G (41) 087002

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers ➡ 7 layers
  - silicon drift and strips ➡ pixels

3. Fast readout

- readout Pb-Pb interactions at > 100 kHz and pp interactions at ~ several 10^5 Hz (currently limited at 1kHz with full ITS)

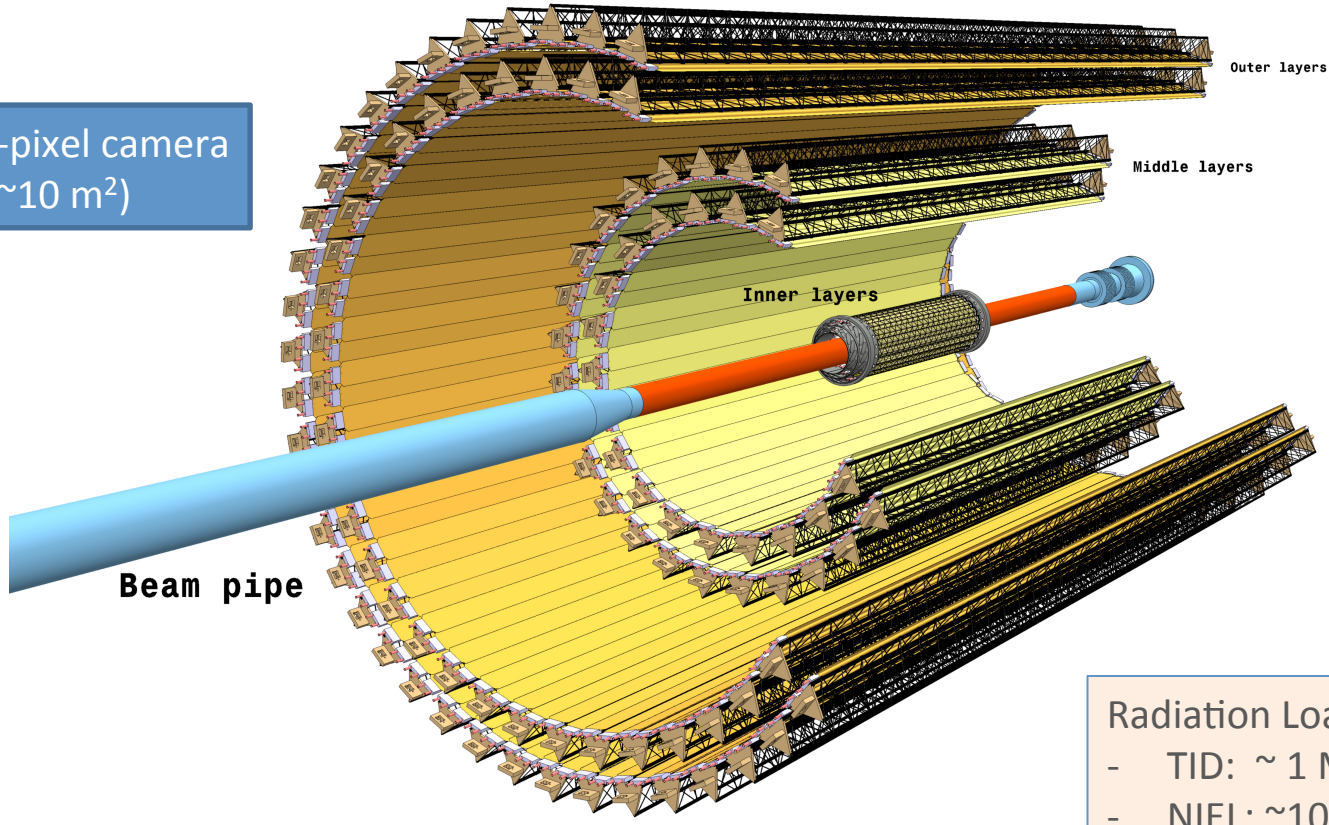
4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

Install detector during LHCC LS2 (2018-19)

New ITS Layout

12.5 G-pixel camera
(~10 m^2)



Radiation Load
- TID: ~ 1 Mrad
- NIEL: ~10^{13} 1MeV n_{eq} / cm^2

7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

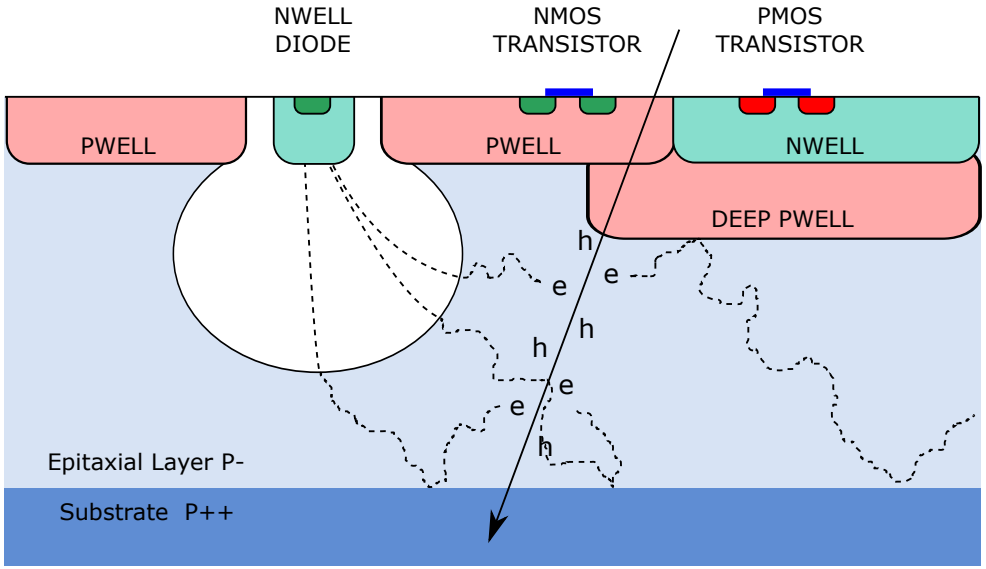
3 Inner Barrel layers (**IB**)

4 Outer Barrel layers (**OB**)

Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

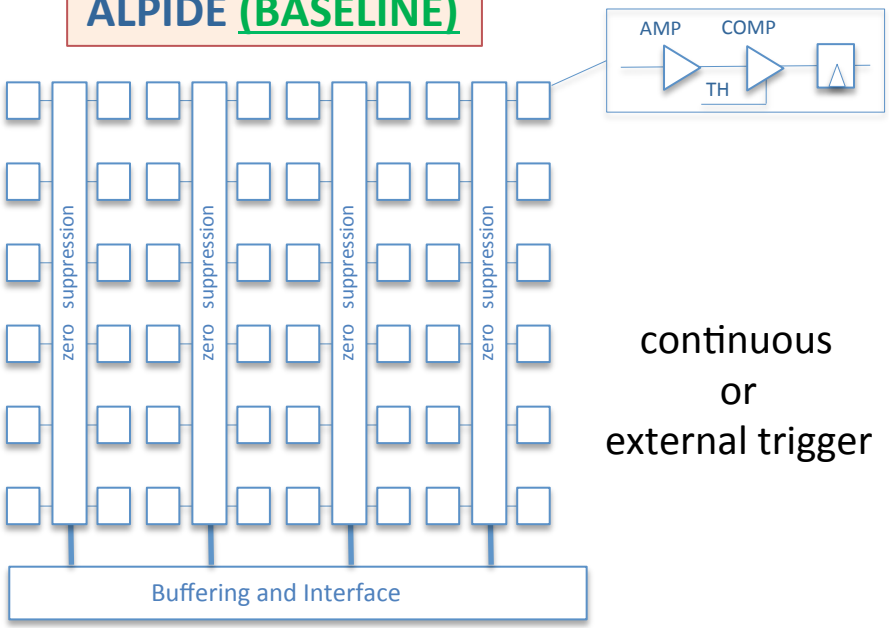
- Gate oxide 3nm

➔ Circuit rad-tolerant

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20μm - 40μm thick) on p-type substrate
- Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

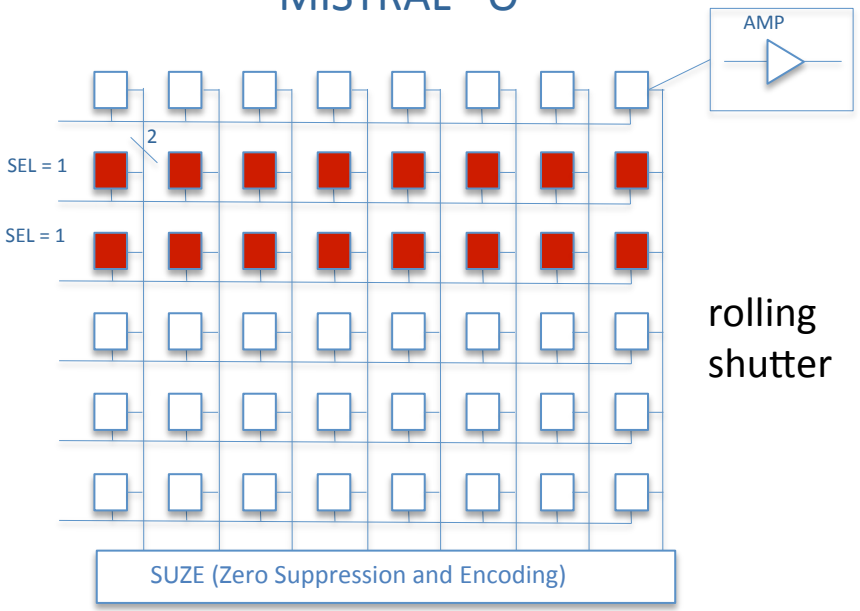
ITS Pixel Chip – two architectures

ALPIDE (BASELINE)



continuous
or
external trigger

MISTRAL - O



rolling
shutter

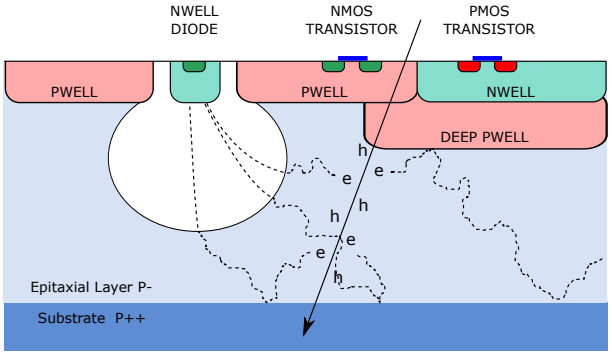
Pixel pitch	28μm x 28μm
Event time resolution	<2μs
Power consumption	39mW/cm^2
Dead area	1.1 mm x 30mm

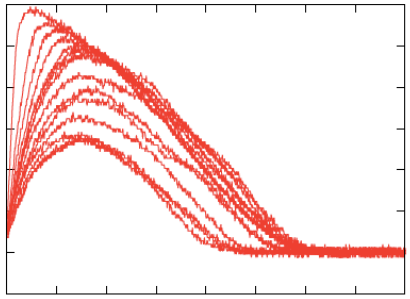
Pixel pitch	36μm x 64μm
Event time resolution	~20μs
Power consumption$^{(*)}$	97mW/cm^2
Dead area	1.7 mm x 30mm

ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

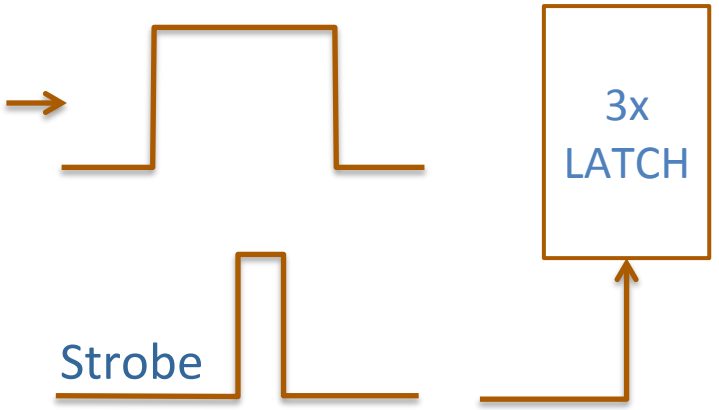
$^{(*)}$ might further reduce to 73mW/cm^2

ALPIDE Principle of Operation





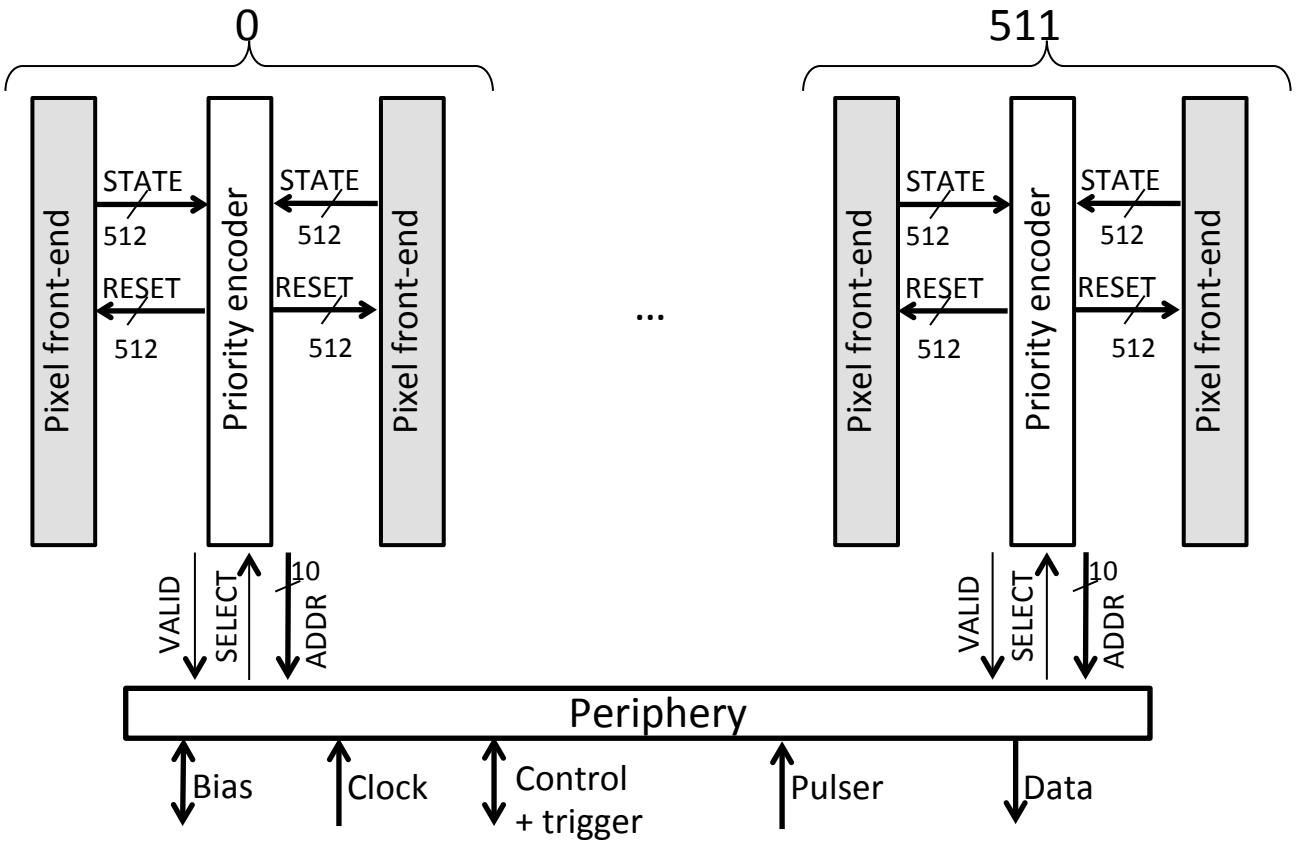
particle hit



Front-end acts as a delay line

- Sensor and front-end continuously active
- Upon particle hit front end forms a pulse with ~ 1-2 µs rise time
- Threshold is applied to form binary pulse
- Hit is latched into memory if strobe is applied during binary pulse

ALPIDE Principle of Operation



Hit driven architecture

- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit ➔ low power

pALPIDE-1 (May 2014) – first full-scale prototype

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Final pixel pitch: 28μm x 28μm
- Power consumption: < 40mW/cm^2
- Interface pads over matrix
- 1 register/pixel, no final interface

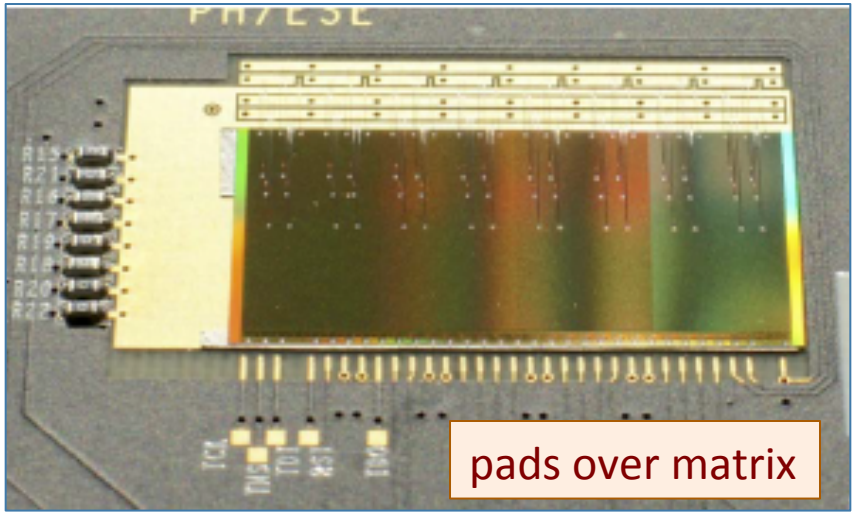
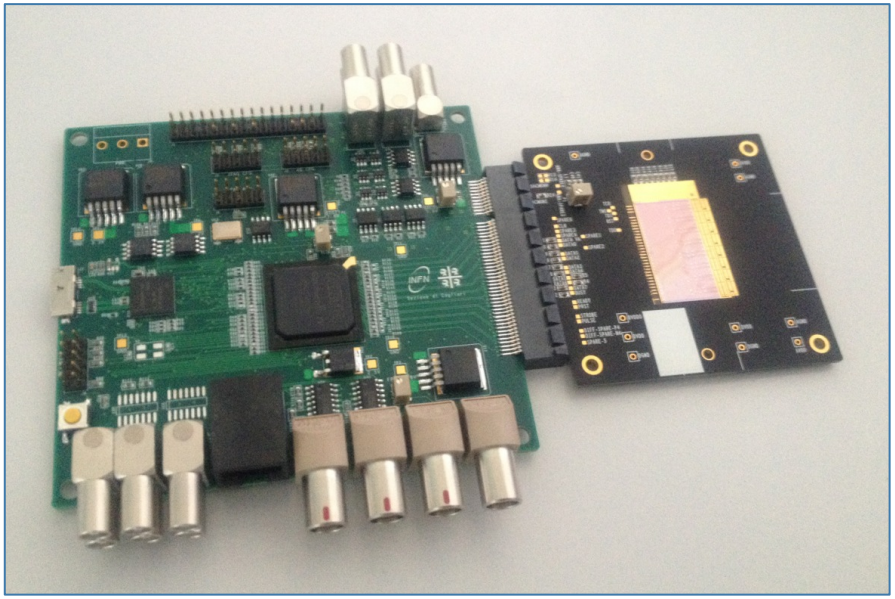
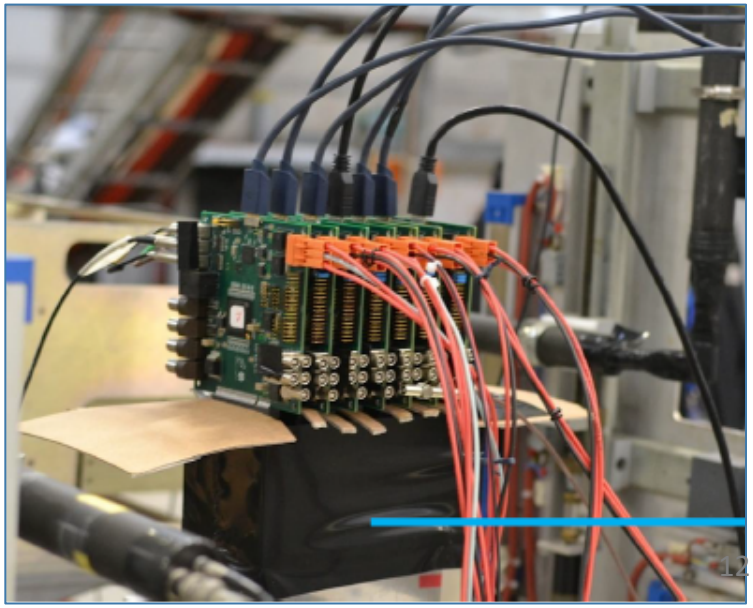


Figure: picture of pALPIDE-1

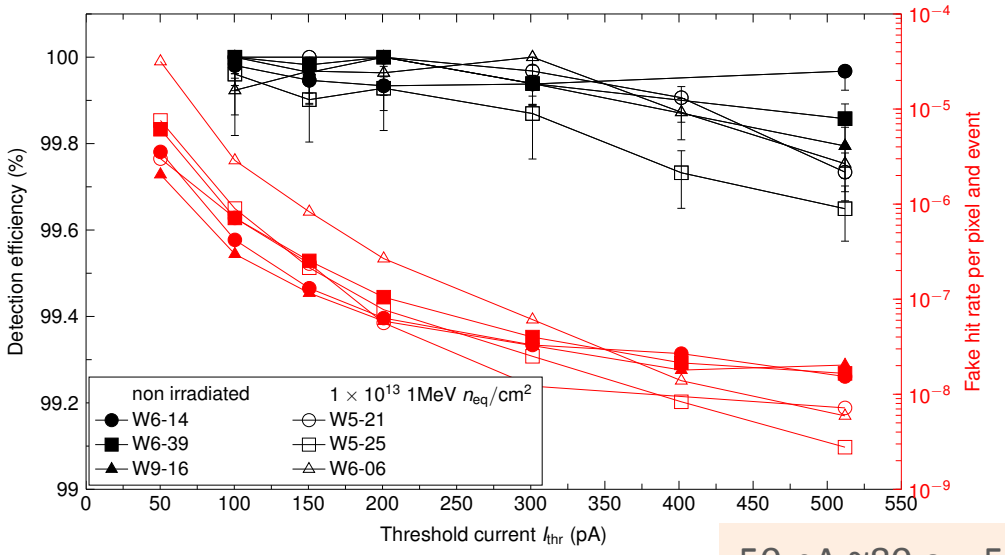
7-plane telescope based on pALPIDE-1 chip



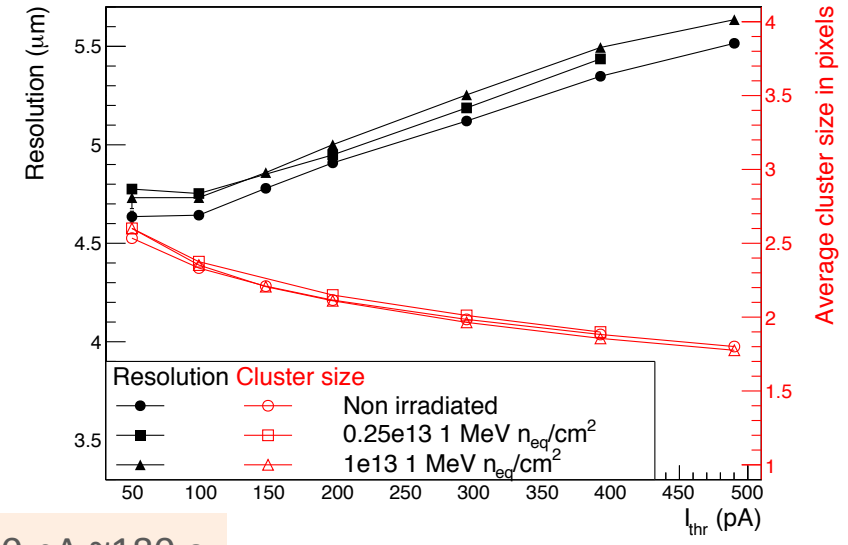


pALPIDE-1 – PS test beam (Sep & Dec 2014)

Efficiency and fake hit rate



Spatial resolution



50 pA ~80 e, 500 pA ~180 e

CERN PS: 5 – 7 GeV π^- (Dec 2014)

- Results refer to 50 μm thick chips:
  - 3 non irradiated and
  - 3 irradiated with 10^{13} 1MeV n_{eq} / cm²

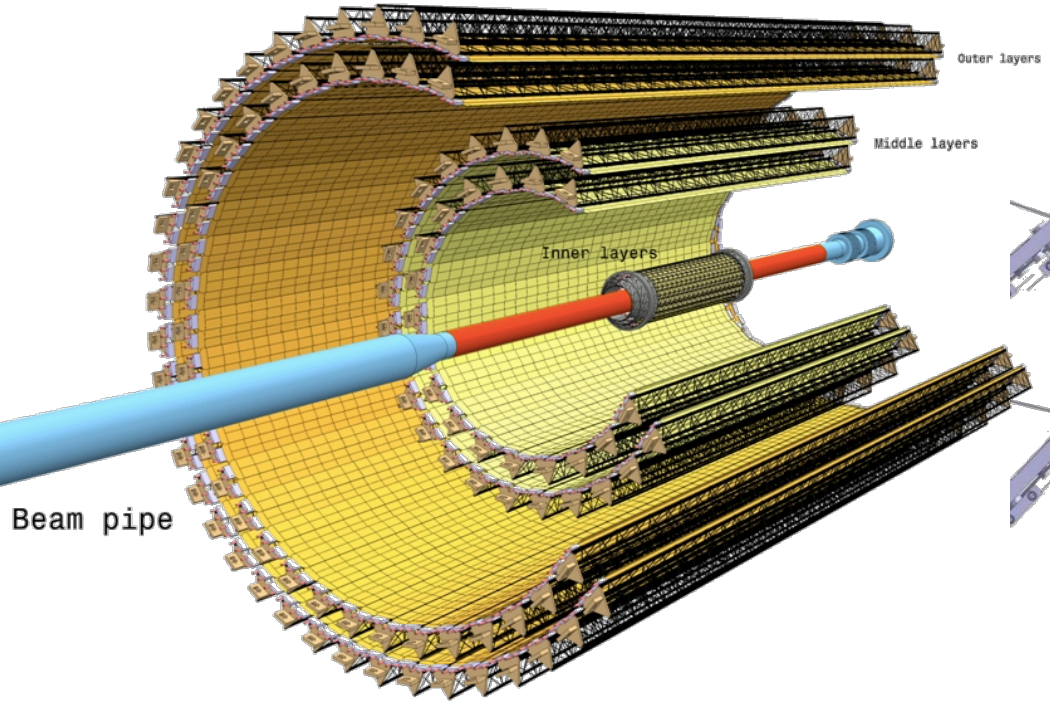
CERN PS: 5 – 7 GeV π^- (Sep 2014)

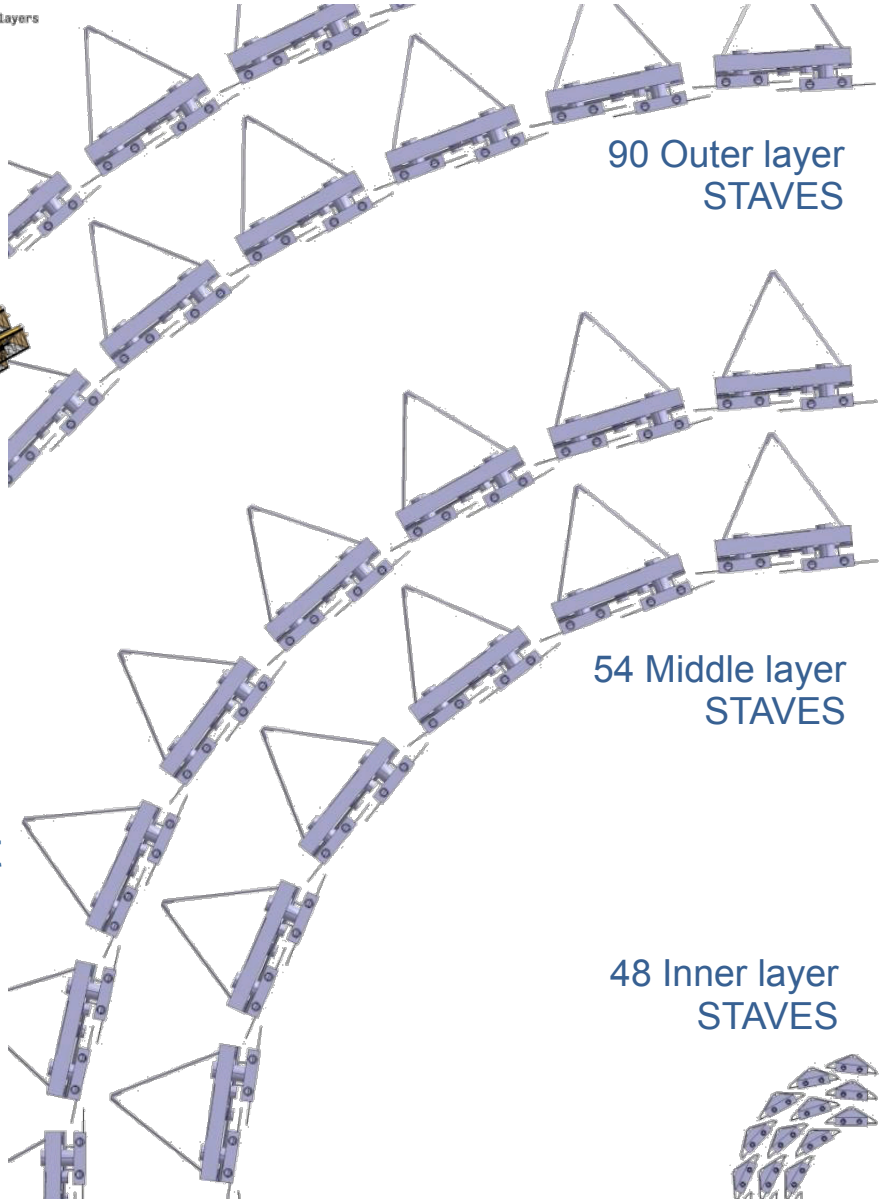
- Results refer to 50 μm thick chips:
  - non irradiated
  - irradiated with 0.25×10^{13} n / cm²
  - irradiated with 10^{13} n / cm²

$\lambda_{fake} << 10^{-5}$ / event/pixel @ $\varepsilon_{det} > 99\%$ ➡ very large margin over design requirements

$\sigma_{det} \sim 5$ μm ➡ large margin of operation

New ITS layout

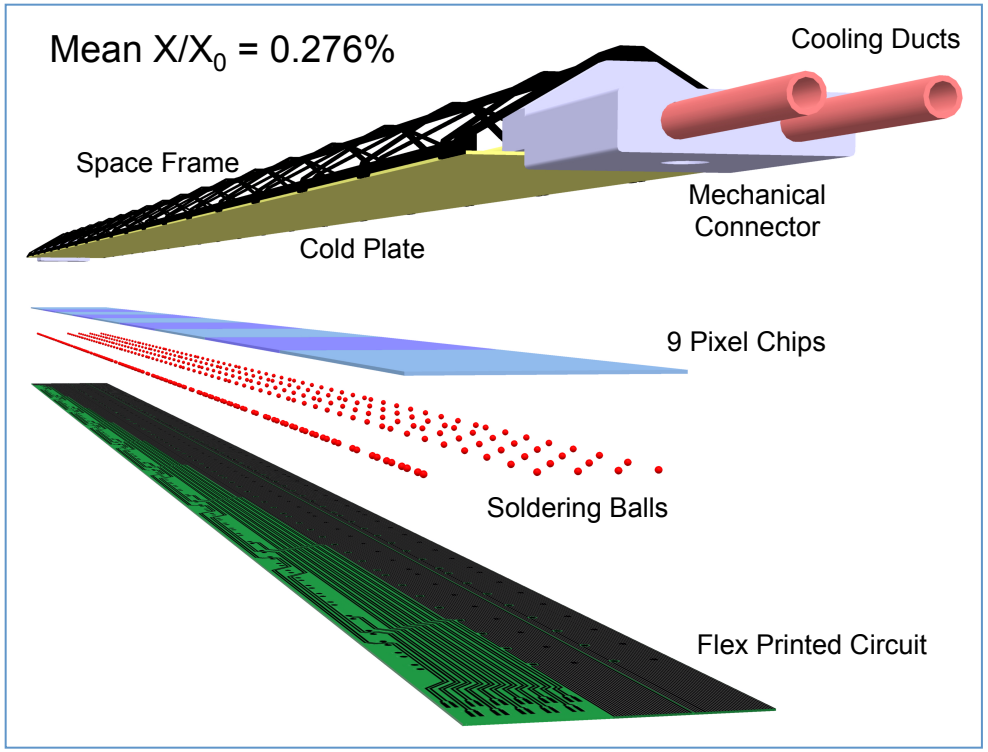


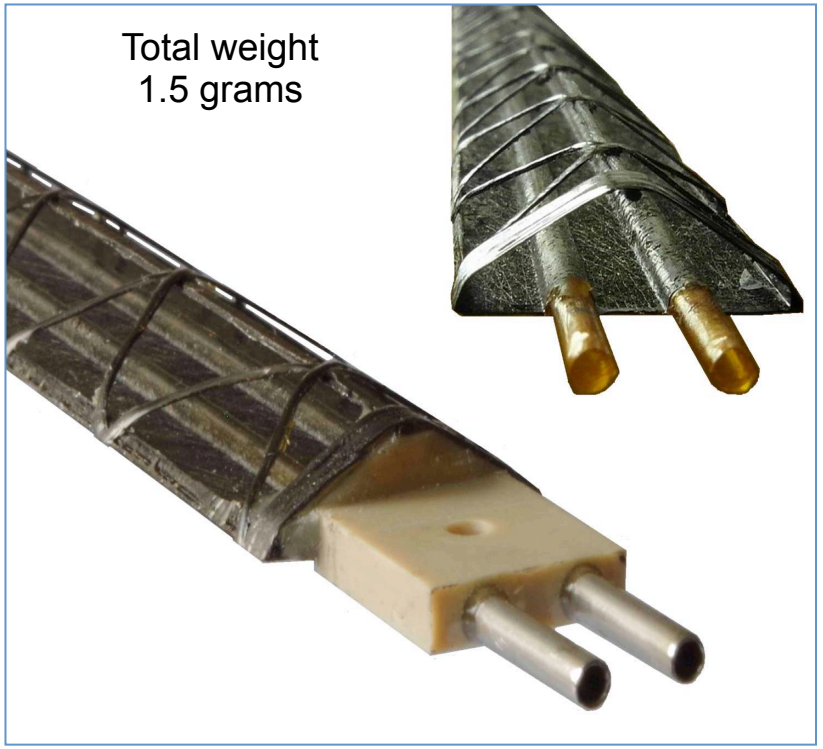


ITS layers are (azimuthally) segmented in staves, which are mechanically independent

Radial coverage 23mm÷405mm

New ITS Layout - Inner Barrel Stave





<Radius> (mm): 23,31,39

Length in z (mm): 290

Nr. of staves: 12, 16, 20

Nr. of chips/stave: 9

Nr. of chips/layer: 108, 144, 180

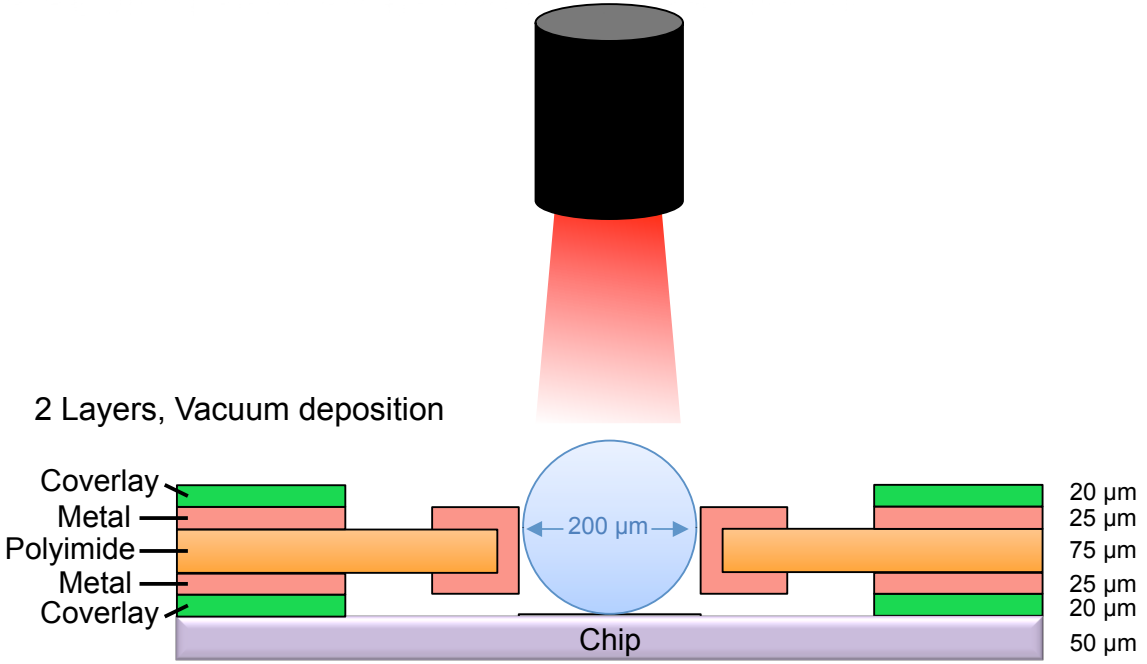
Material thickness: ~ 0.3% X_0

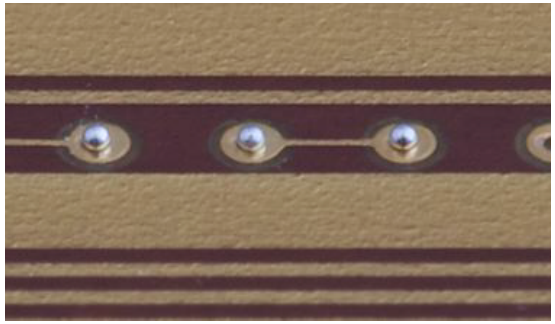
Power density: < 100 mW/cm^2

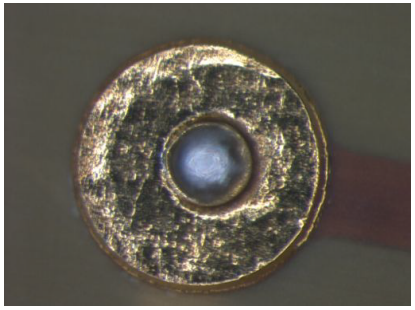
Throughput (@100kHz): < 80 Mb/s × cm^{-2}

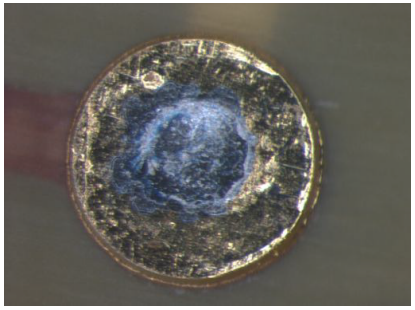
Interconnection of pixel chip to flex PCB

Laser soldering: Interconnection of Pixel chip on flexible printed circuit







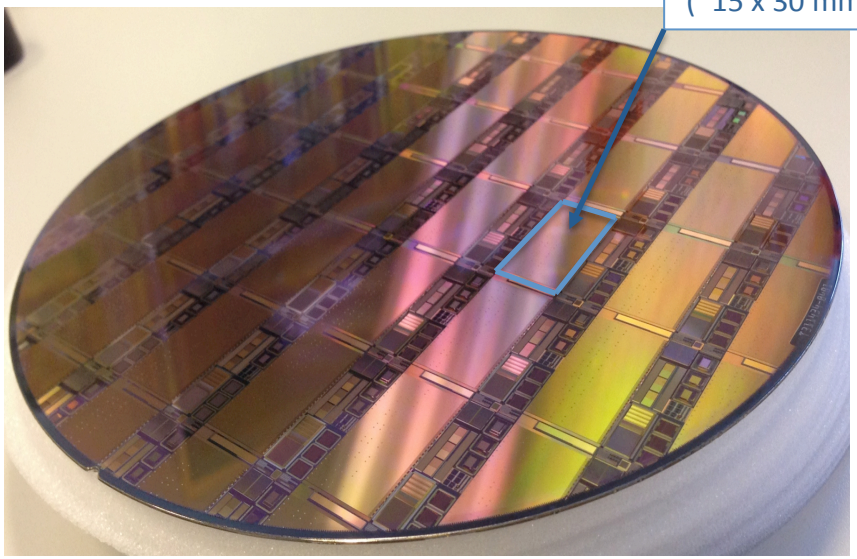


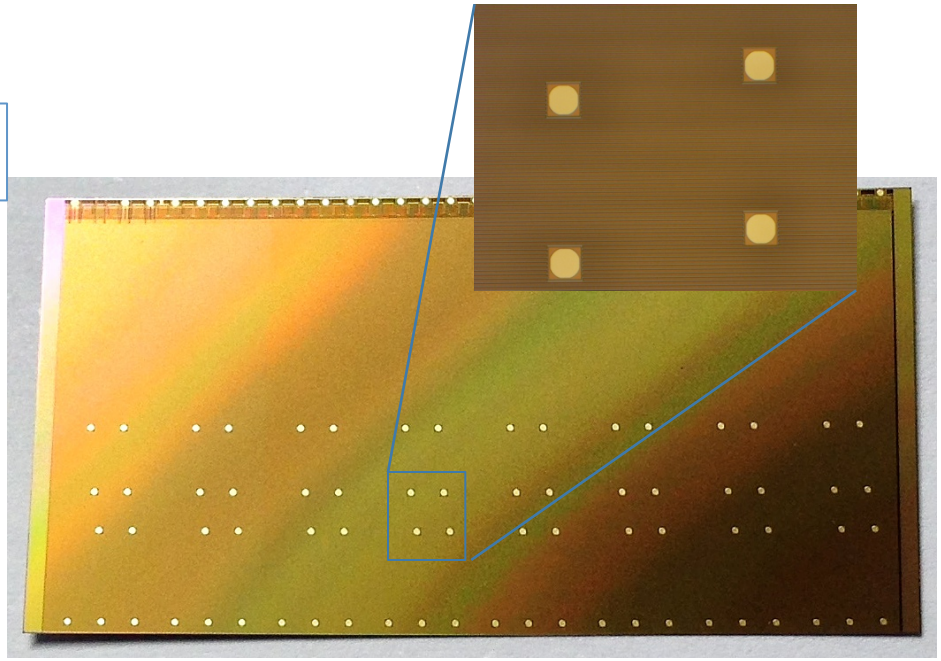
Pixel chip – interconnection to flex PCB

Solder Pads

- to solder the chip on the FPC, Al pads need Ni-Au plating (wet-able surface)
- plating is done on wafer using electroless Ni-Au plating, prior to thinning and dicing
- R&D experience 2012-now: plating of about 50 wafers (pad wafers and CMOS wafers)

Status
Market survey concluded
Tendering starting soon



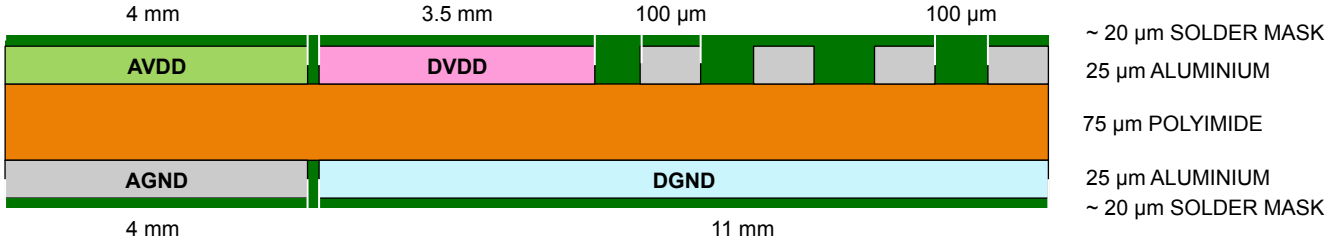


Contact pads are distributed over the matrix (custom designed)

Inner Barrel Stave – flexible printed circuit

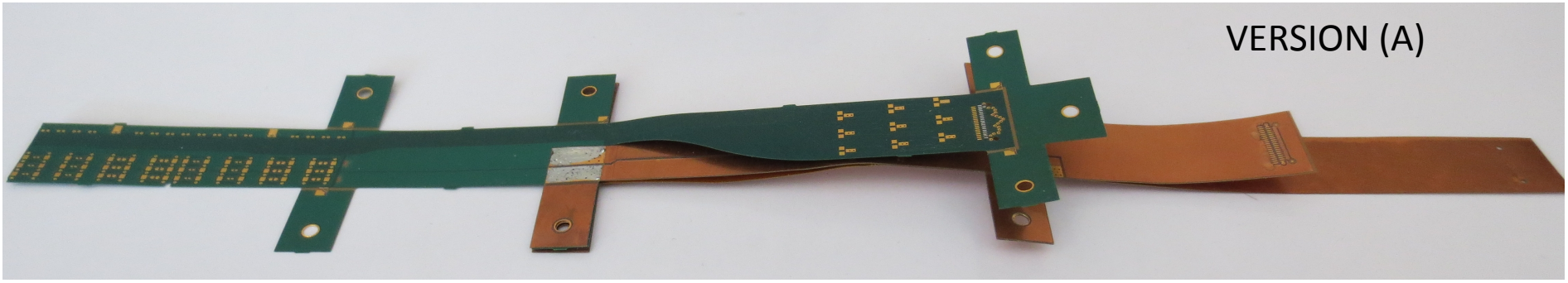
IB Flexible Printed Circuit prototypes (Al power planes and signal tracks)

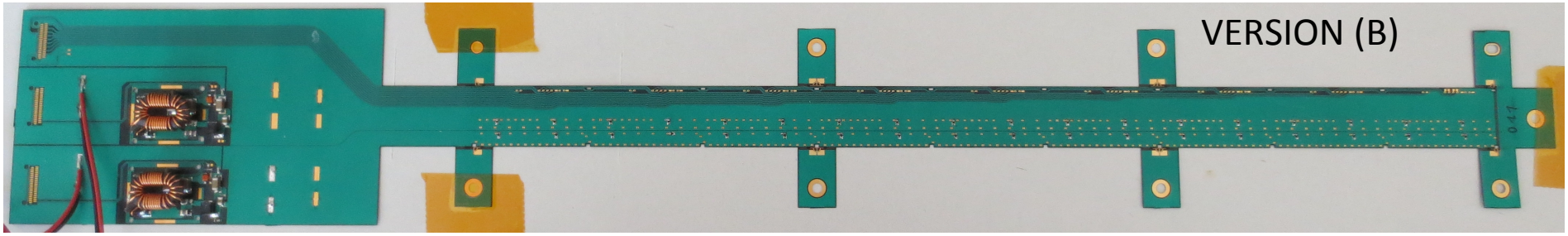
Metallised vias of 220μm diameter



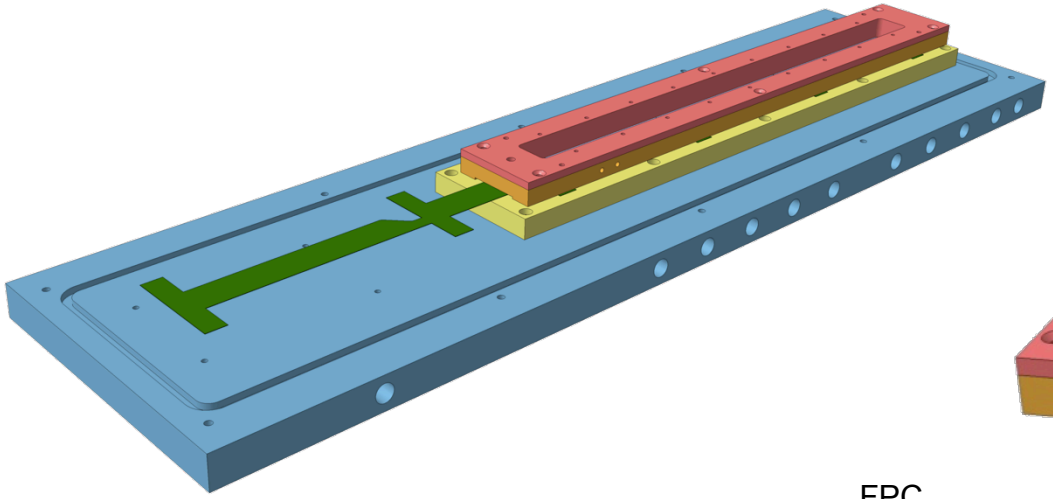
Status

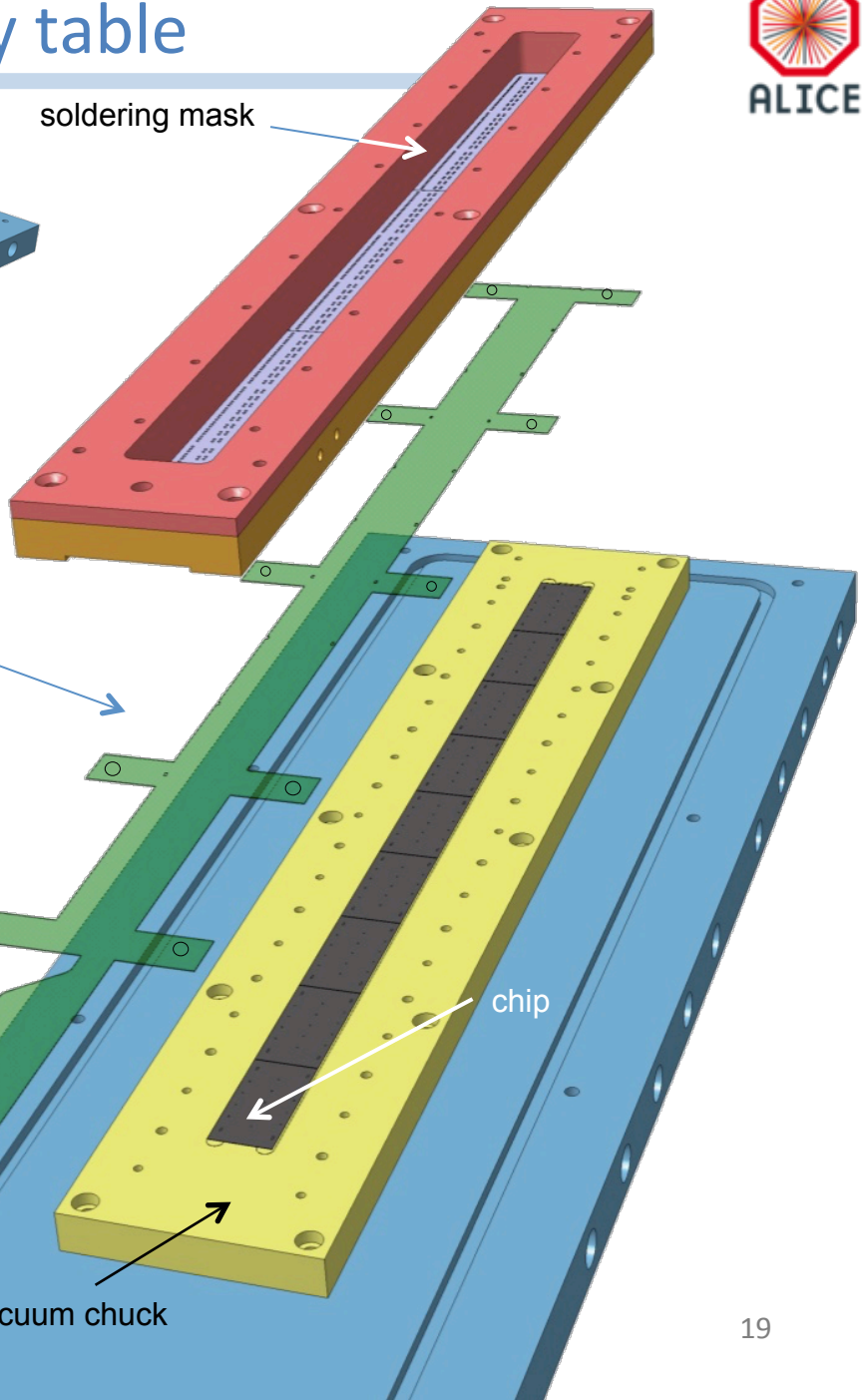
Two FPC versions (differ for the location of DC-DC converters) ready to be tested with ALPIDE-2

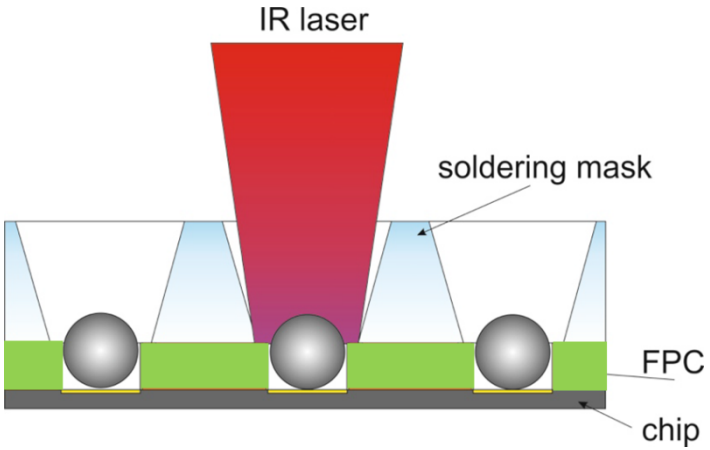




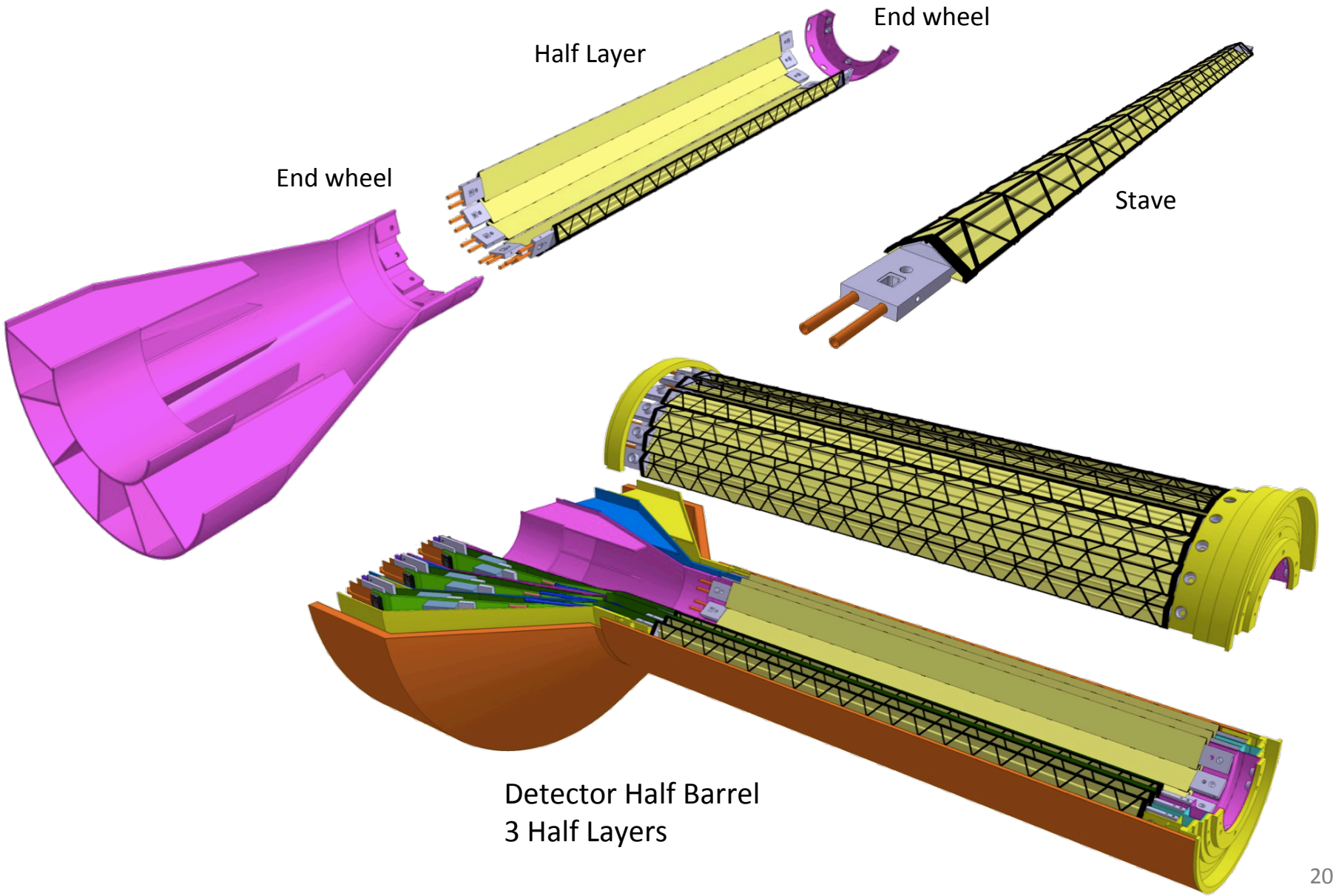
Inner Barrel Stave – HIC assembly table





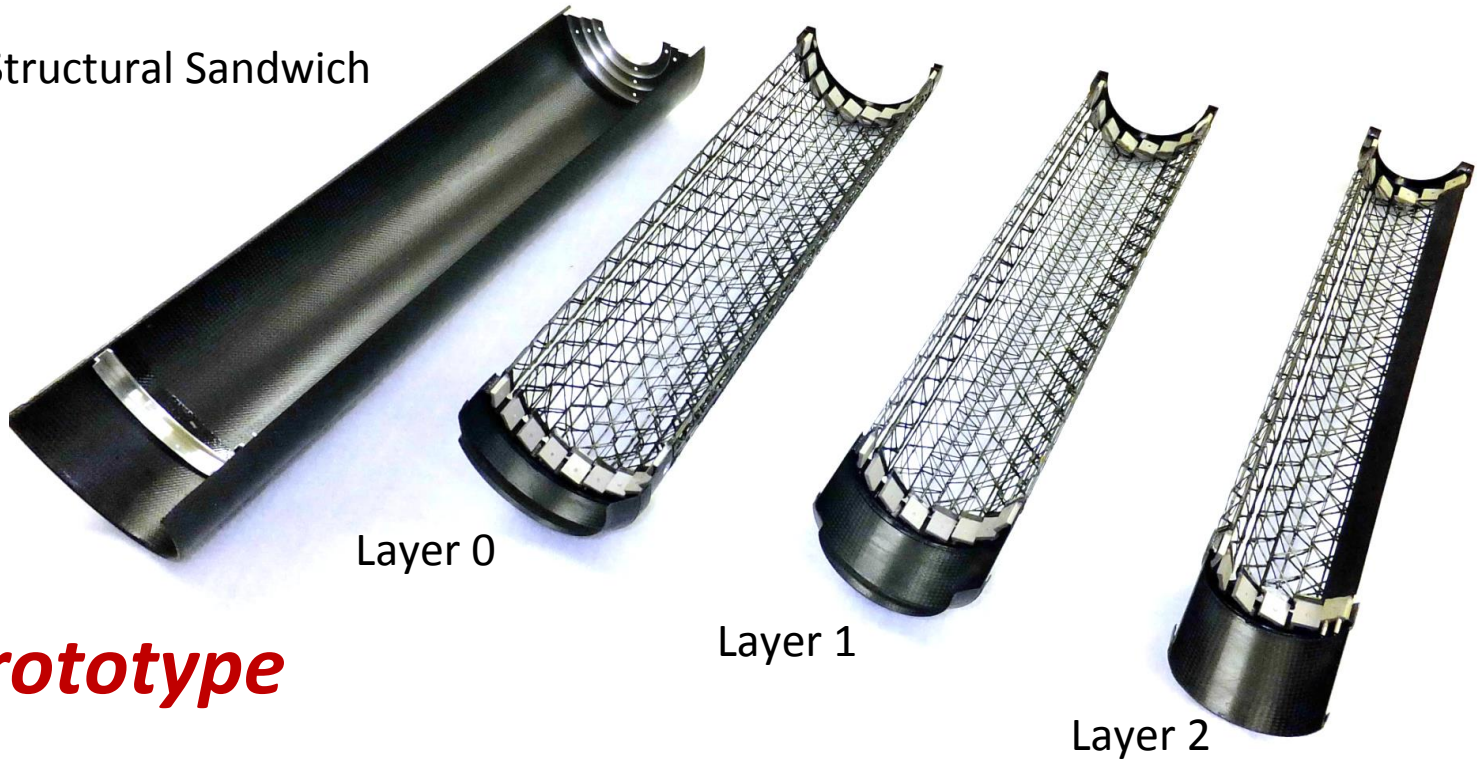


Inner Barrel

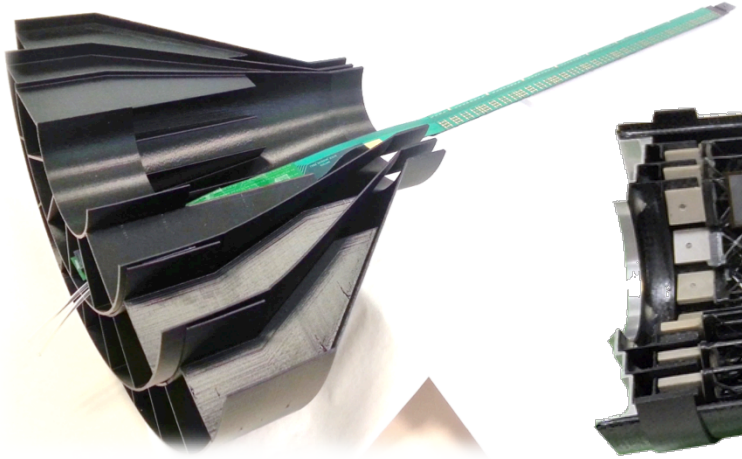


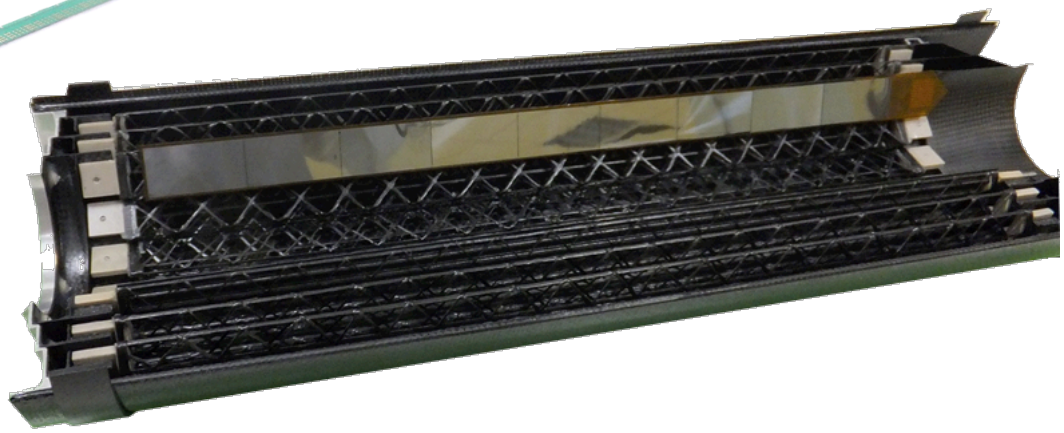
Detector Half Barrel
3 Half Layers

Inner Barrel – full-scale prototype

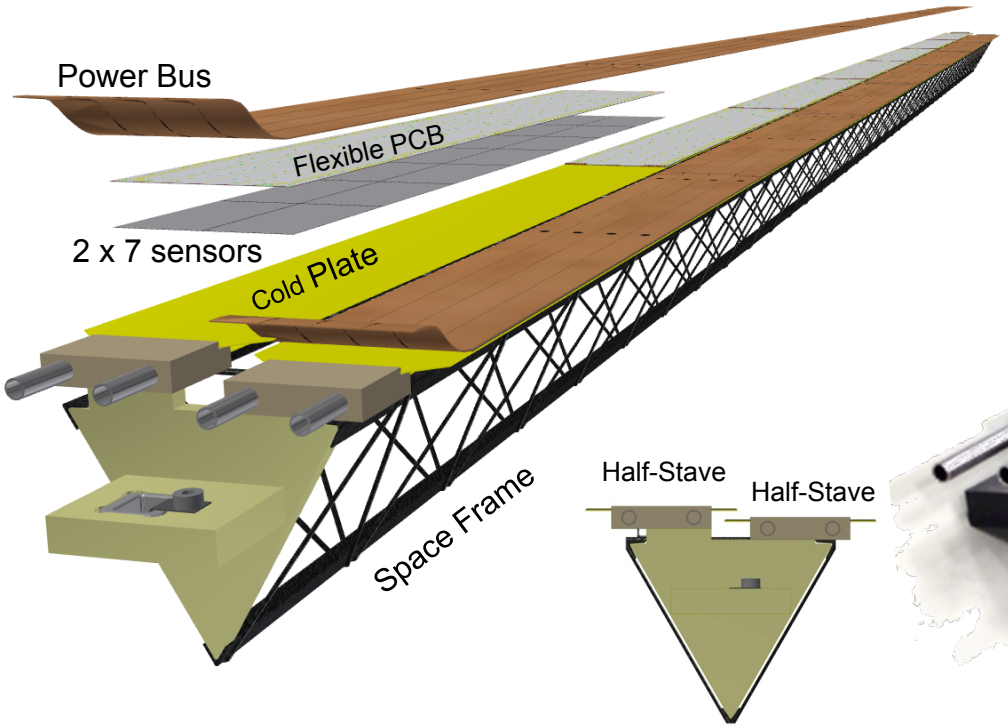


Prototype





ITS Outer Barrel



Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Length (mm): 900 (ML), 1500 (OL)

Nr. staves: 24, 30, 42, 48

Nr. modules/stave: 4 (ML), 7 (OL)

Nr. Chips/layer: 6048 (ML), 17740(OL)

Material thickness: ~ 1% X_0

Power density < 100 mW / cm^2

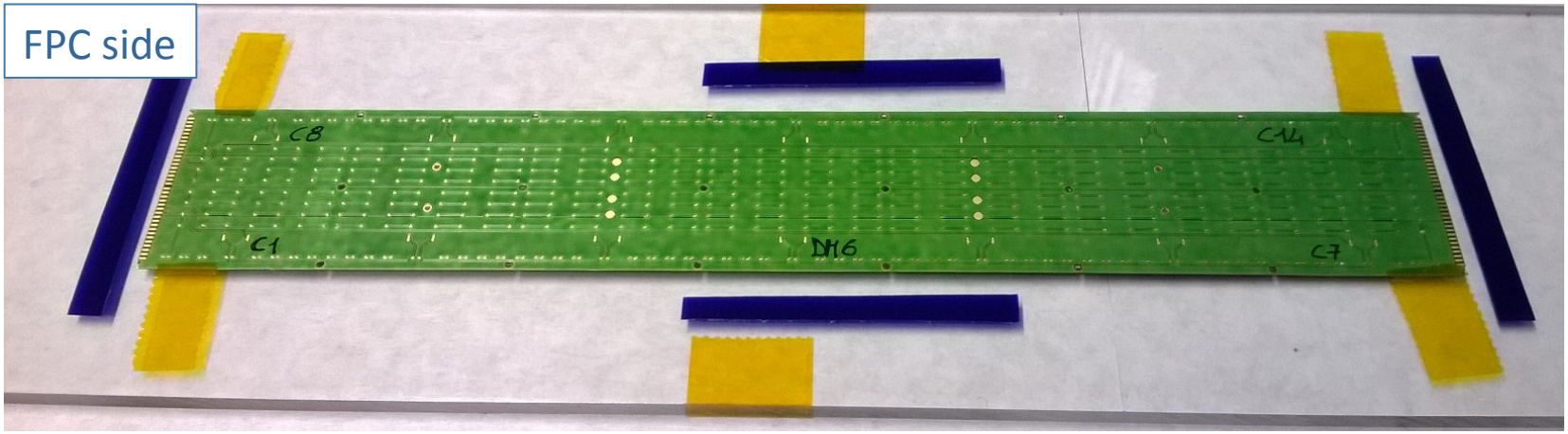
Throughput (@100kHz): < 3Mb/s × cm^{-2}

ITS Outer Barrel

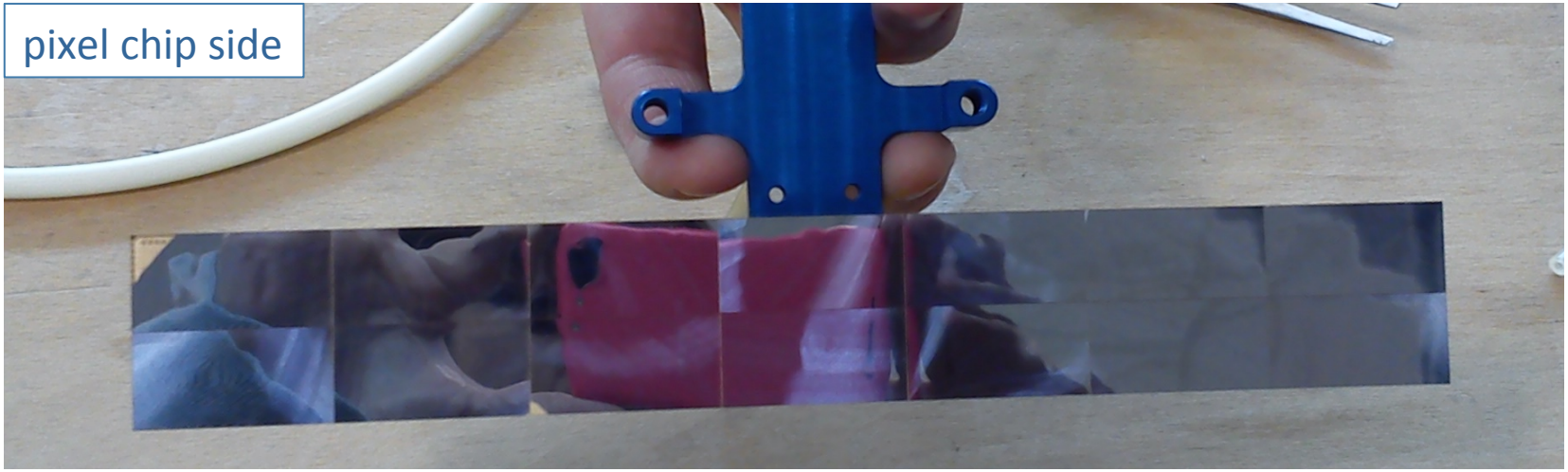
HIC: Interconnection of pixel chip on flexible printed circuit (FPC)

Bari

FPC side

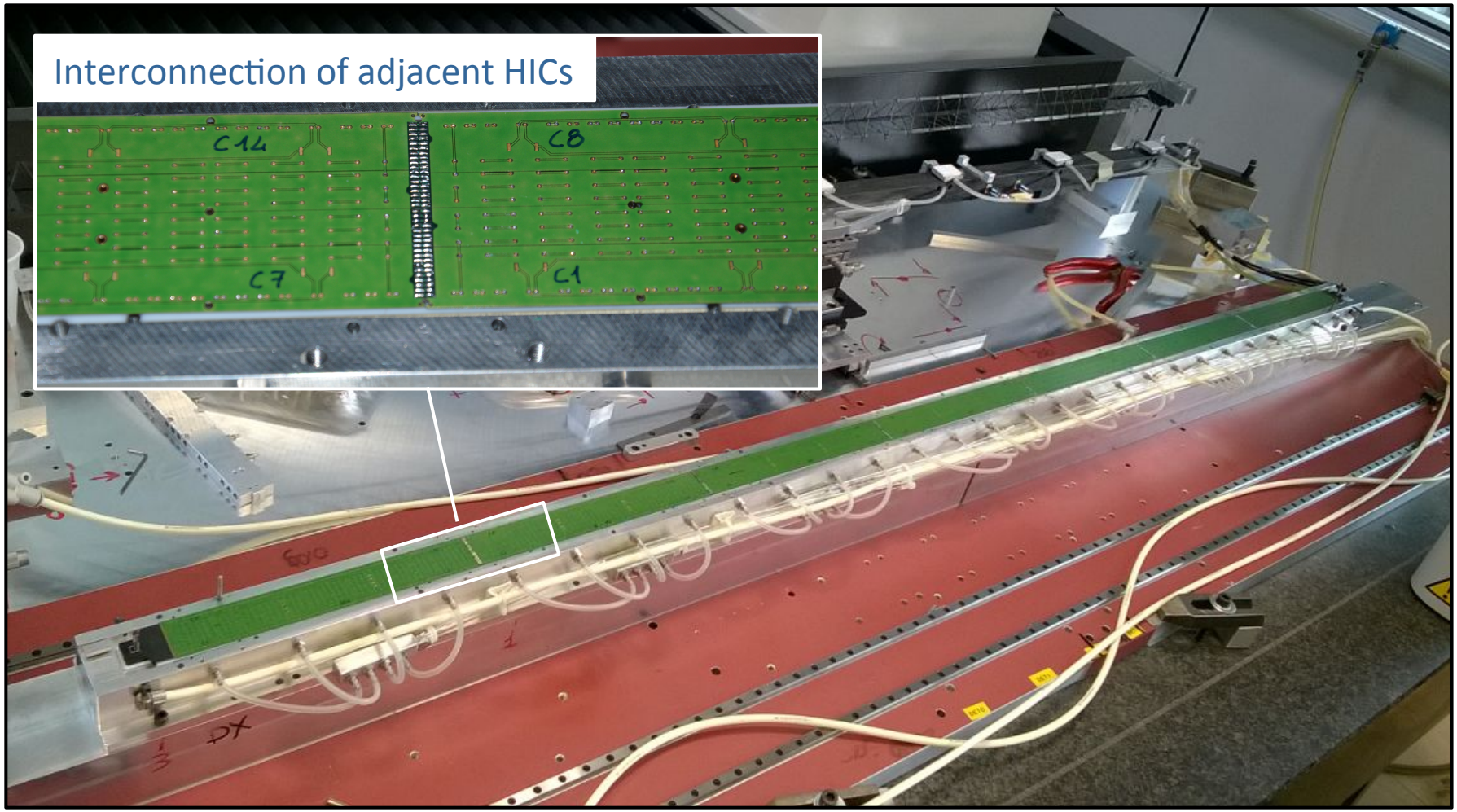


pixel chip side

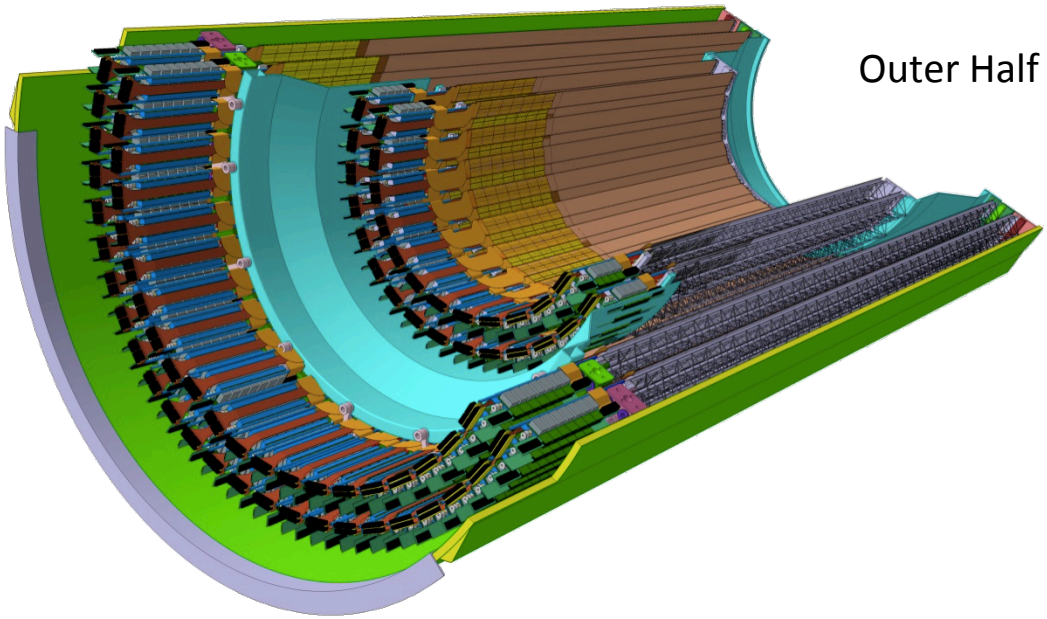


ITS Outer Barrel

Half-stave equipped with dummy HICs (dummy silicon chips)

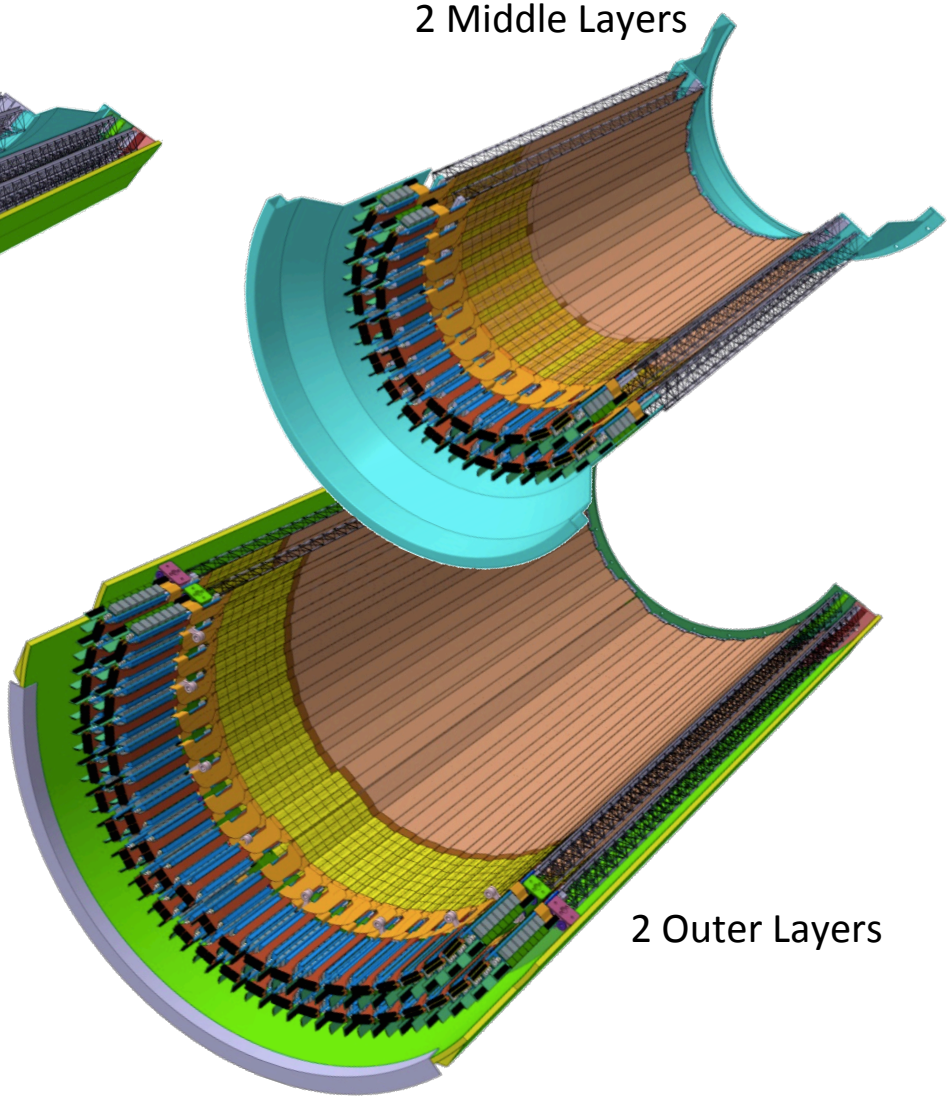


ITS Outer Detector Barrel

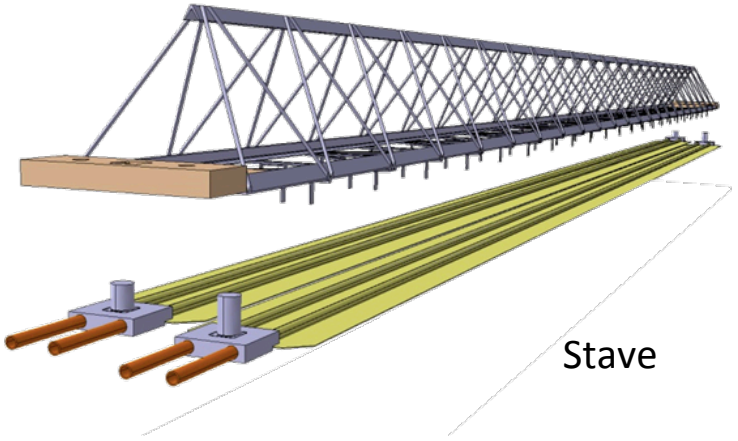


Outer Half Barrel

2 Middle Layers

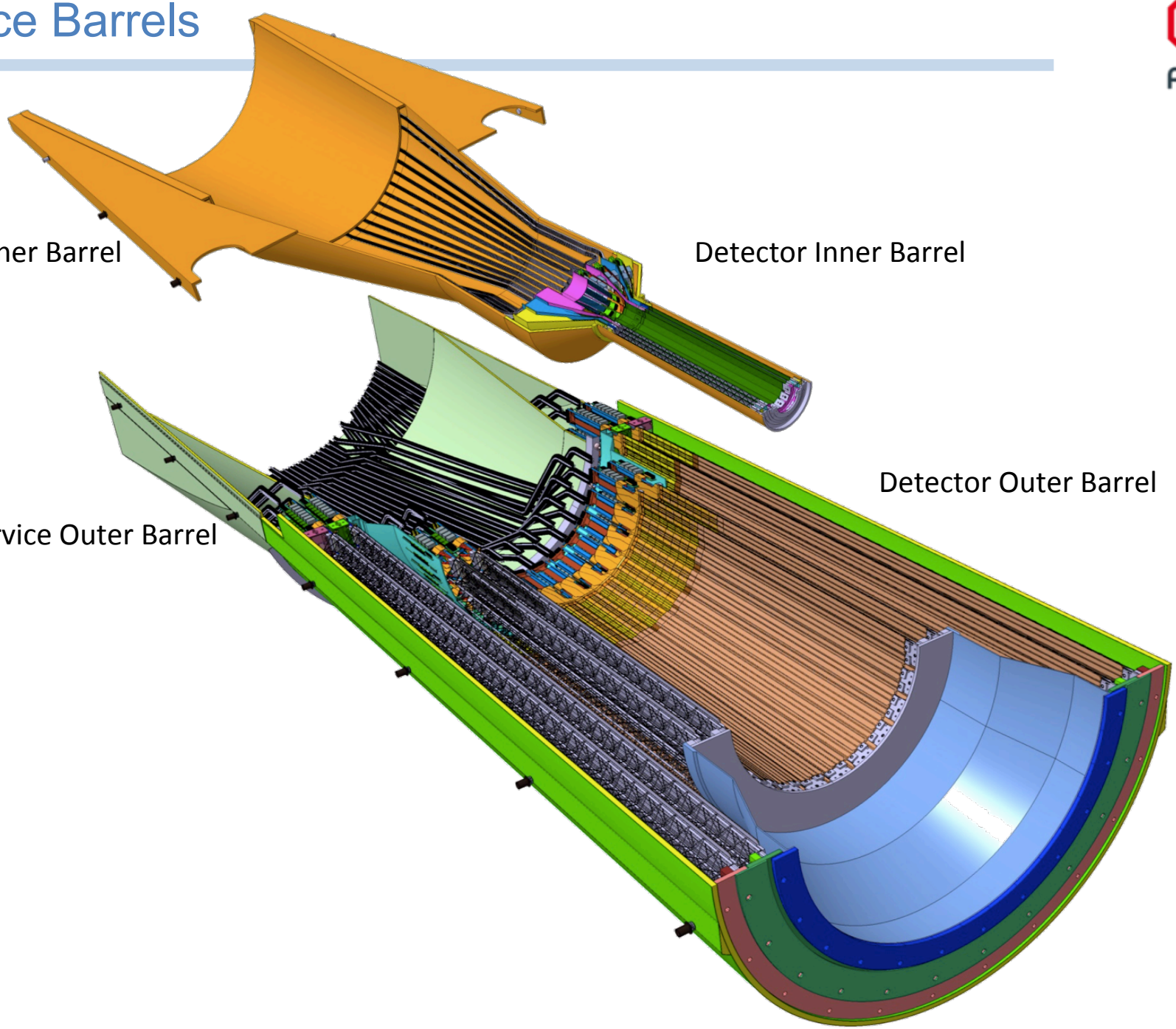


2 Outer Layers



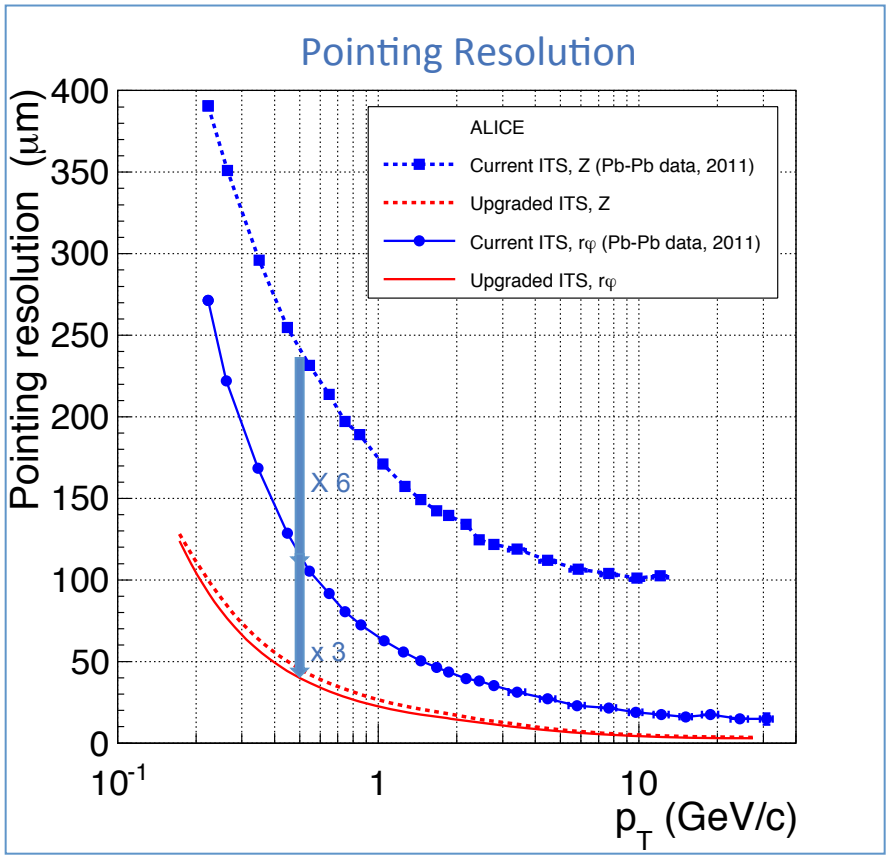
Stave

Service Barrels

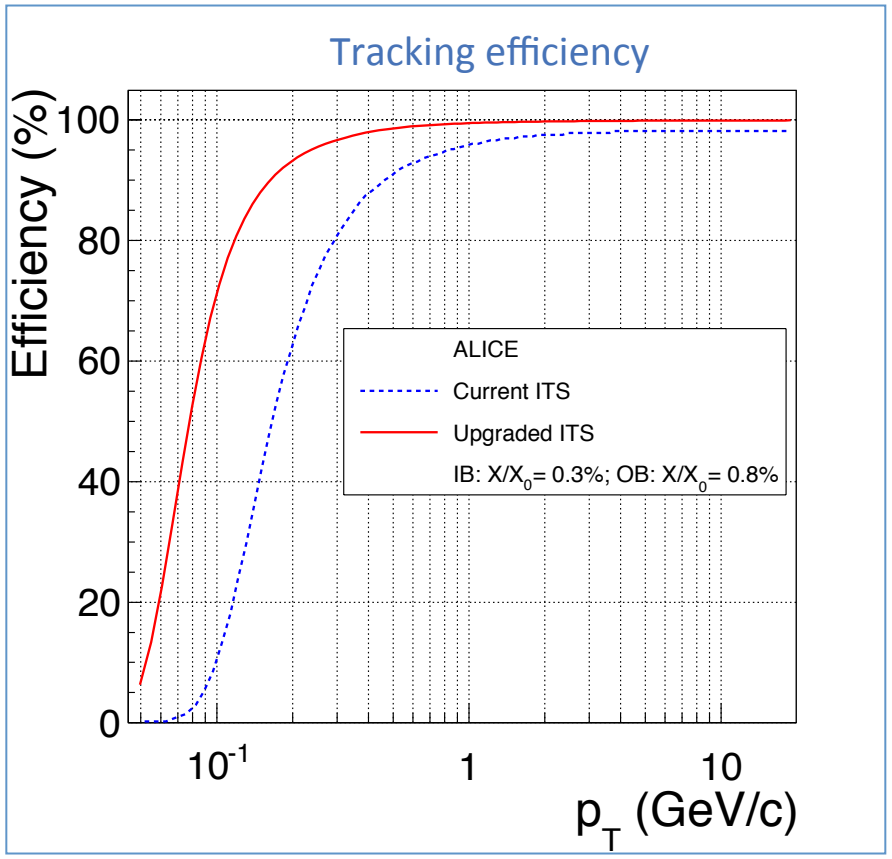


Performance of new ITS (MC simulations)

Impact parameter resolution

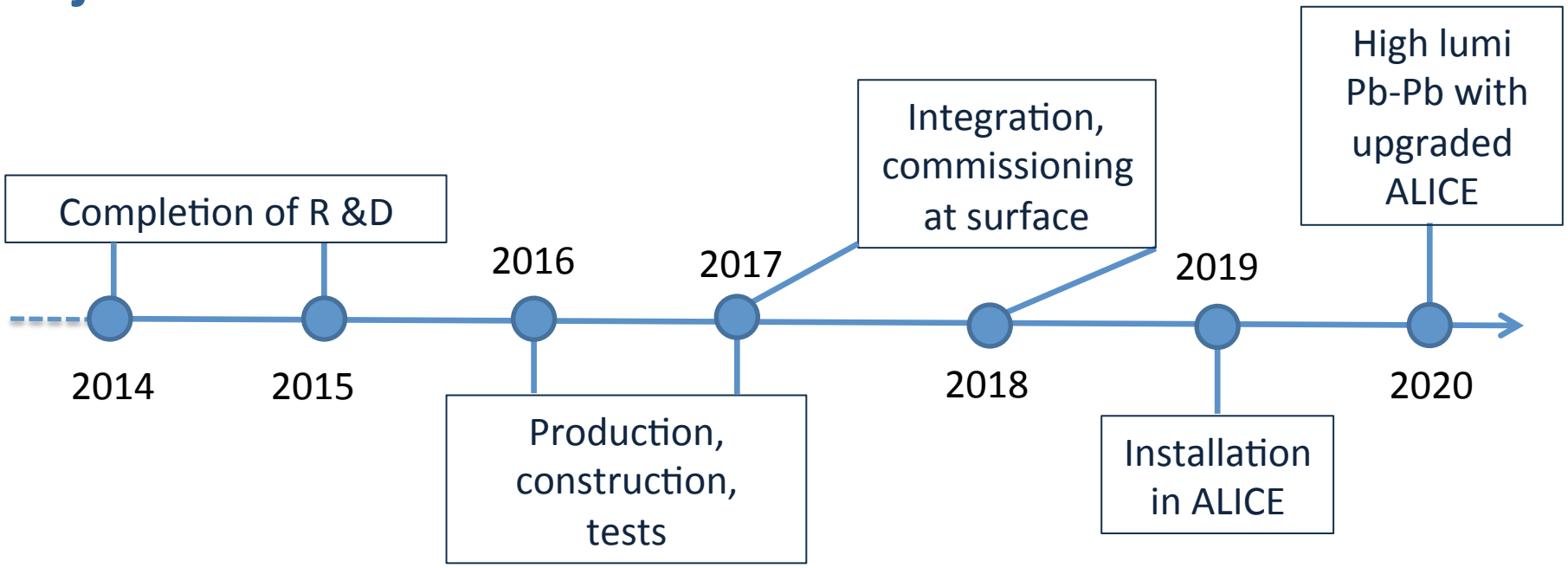


Tracking efficiency (ITS standalone)



~40 μm at p_T = 500 MeV/c

Project Timeline and Collaboration



ALICE ITS Collaboration

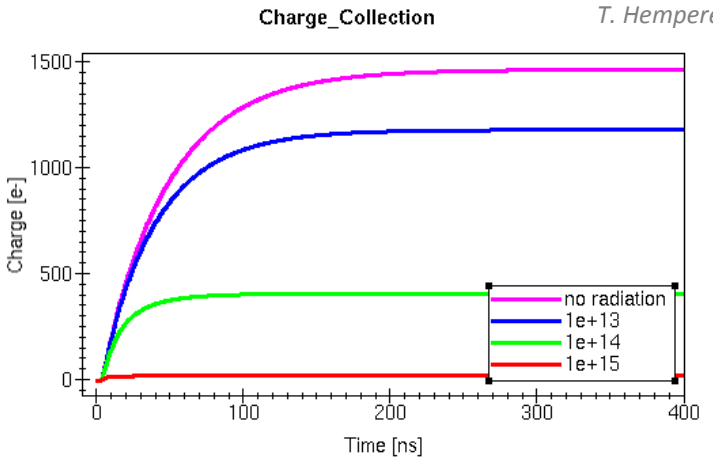
CERN, China (Wuhan), Check Republic (Prague), France (Grenoble, Strasbourg), Italy (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino), Indonesia (LIPI), Korea (Pusan, Inha, Yonsei), Netherlands (Nikhef, Utrecht), Pakistan (CIIT-Islamabad), Russia (St. Petersburg), Slovakia (Kosice), Thailand (Suranaree, SLRI, TMEC), UK (Daresbury, Liverpool, RAL), Ukraine (Kharkov), USA (Austin, Berkeley)

Institute = participated in current ITS

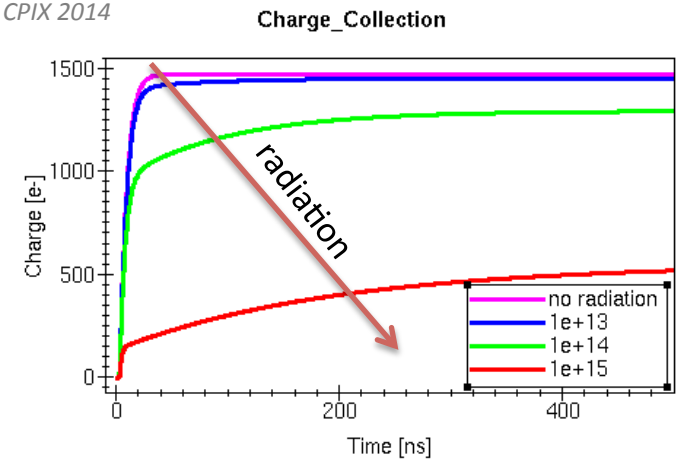
SPARES

ITS Pixel Chip – starting material

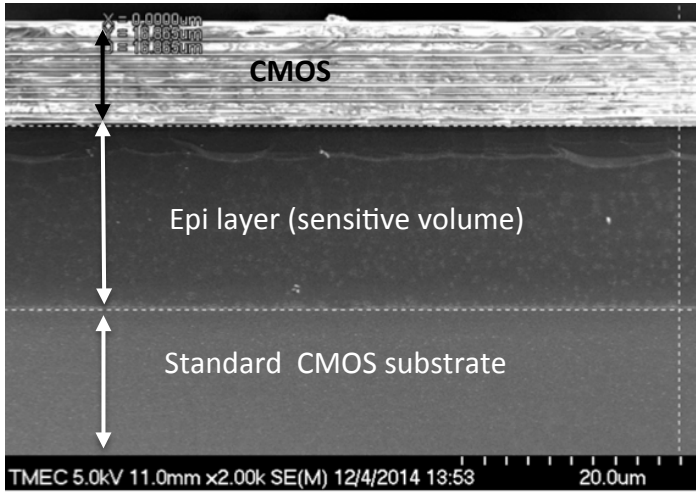
Charge collection time and recombination depend on doping concentration (Si resistivity) and radiation induced dislocations



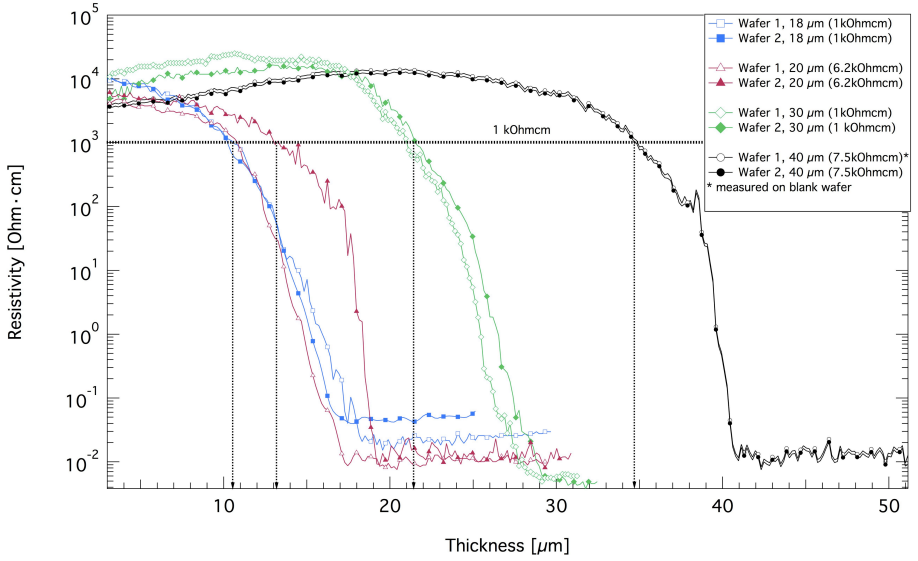
Substrate: 10 Ohm cm, NWELL: @1V PW: @ 0V



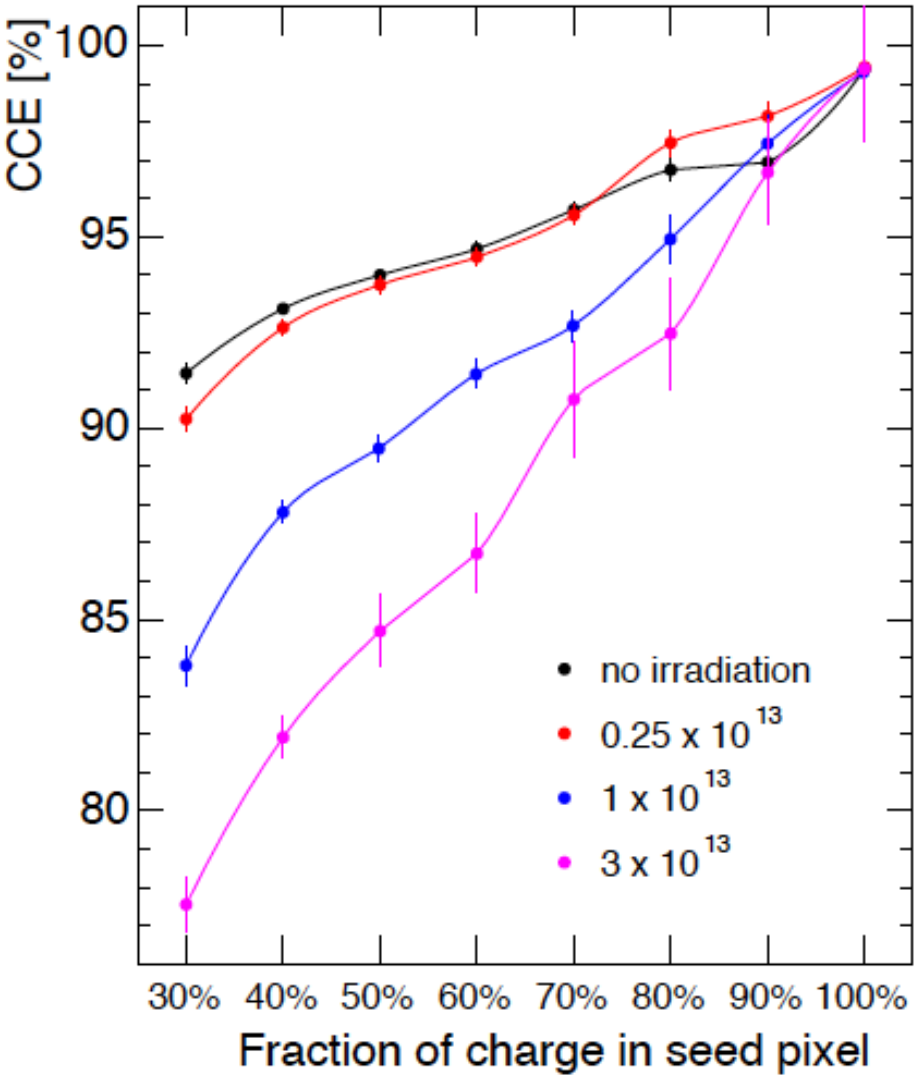
Substrate: 2k Ohm cm, NWELL: @1V PW: @ 0V

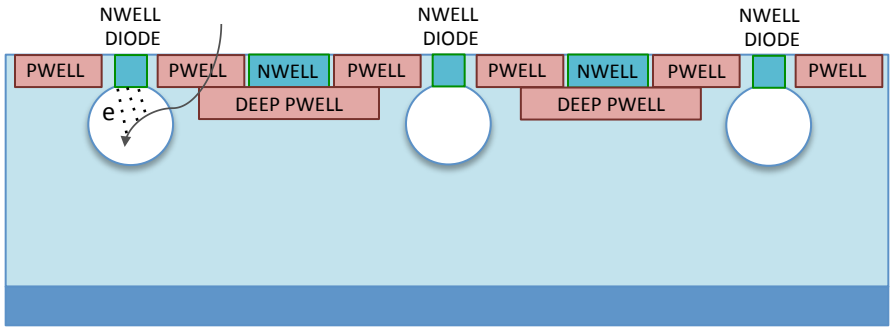


SEM picture: epi thickness 20µm



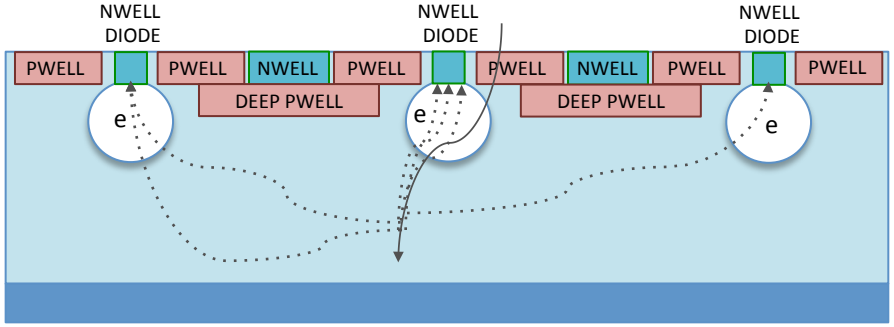
ITS Pixel Chip – charge recombination





^{55}Fe X-ray absorption close to collection diode

- small diffusion => small recombination
- **Signal collected in a single pixel**

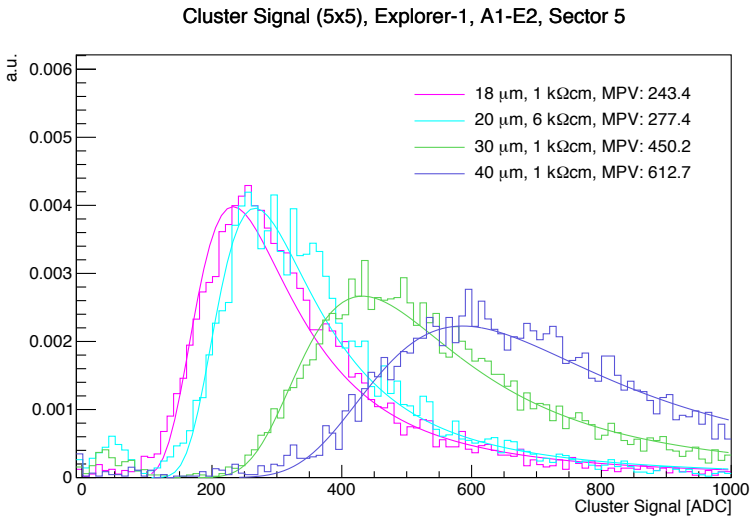


^{55}Fe X-ray absorption far from collection diode

- large diffusion => large recombination
- **signal spreads over several pixels**

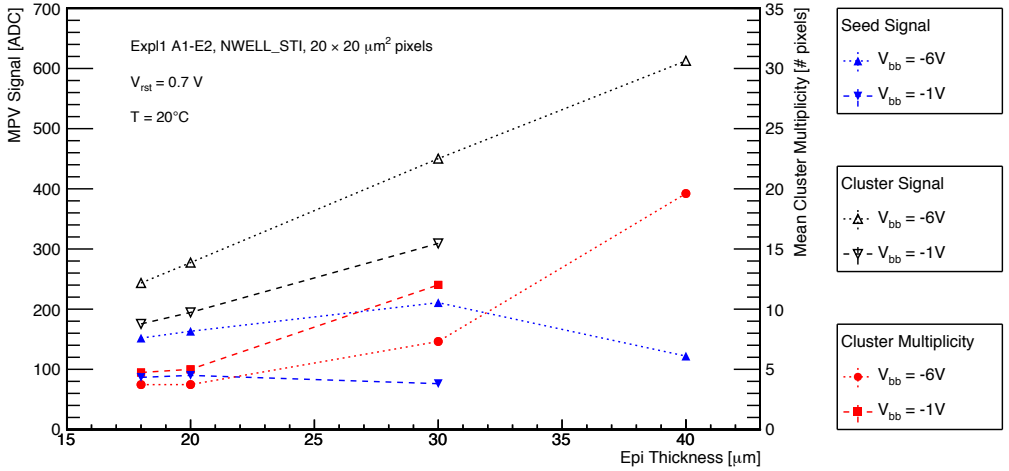
ITS Pixel Chip – starting material

Thicker epitaxial layers will yield more charge but … diffusion increases cluster size



J. Van Hoorne, TIPP2014

J. Phys. G (41) 087002



Measurements done at Desy test beam with 3.2 Gev/c positrons

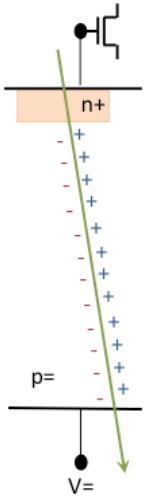
- Cluster charge increases linearly with epi-layer thickness
- Cluster size increases with epi-layer thickness

optimum epi thickness (maximum seed signal) increases by increasing depletion volume

ITS Pixel Chip – starting material

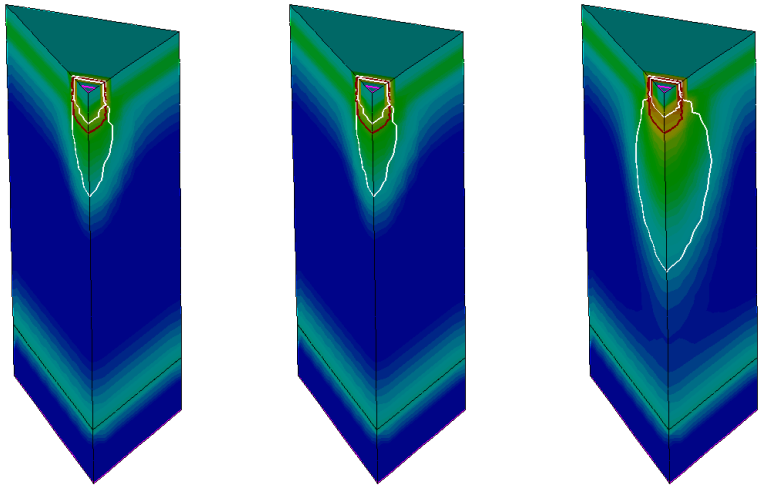
Low input capacitance decisive to achieve large S/N at low power

(W. Snoeys, NIMA 731 (2013) 125-130)



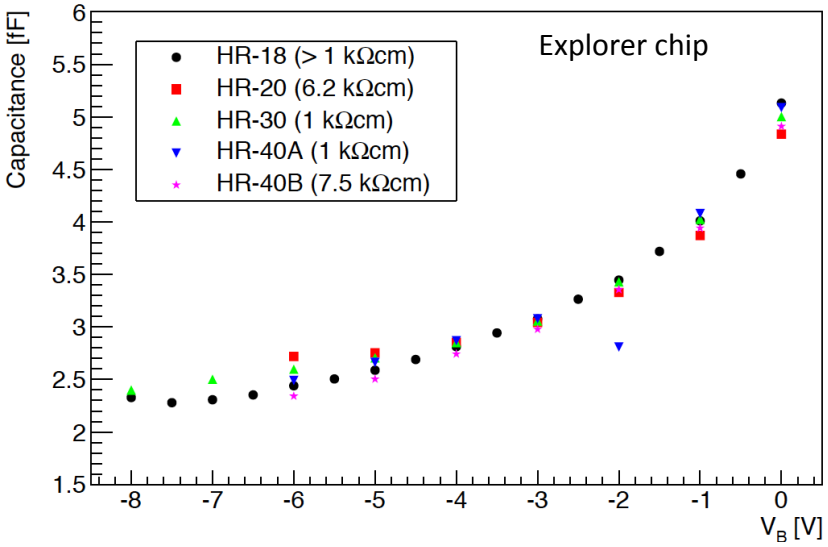
NWELL DIODE output signal = Q /C

- Minimize spread of charge over many pixels
- minimize capacitance:
  - ➡ small diode surface
  - ➡ large depletion volume



-1V, 1x10^{13} cm^{-3} -1V, 1x10^{12} cm^{-3} -6V, 1x10^{12} cm^{-3}

Diode 3µm x 3µm square n-well , White line: boundaries of depletion region



☞ Pixel input capacitance decreases with increasing reverse bias, in agreement with simulated size of depletion region

☞ Minor influence of epi resistivity for current pixel layout

PIXEL Chip – General Requirements

Parameter	Inner Barrel	Outer Barrel
Silicon thickness	50 μm	
Spatial resolution	5 μm	10 μm
chip dimensions	15 mm x 30 mm	
Power density	< 300 mW/cm^2	< 100 mW/cm^2
Event time resolution	< 30 μs	
Detection efficiency	> 99%	
Fake hit rate	< 10^{-5} per readout frame	
TID radiation hardness (*)	2700 krad	100 krad
NIEL radiation hardness (*)	1.7x10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq} / cm^2

(*) 10 x radiation load integrated over approved programme (~ 6 years of operation)

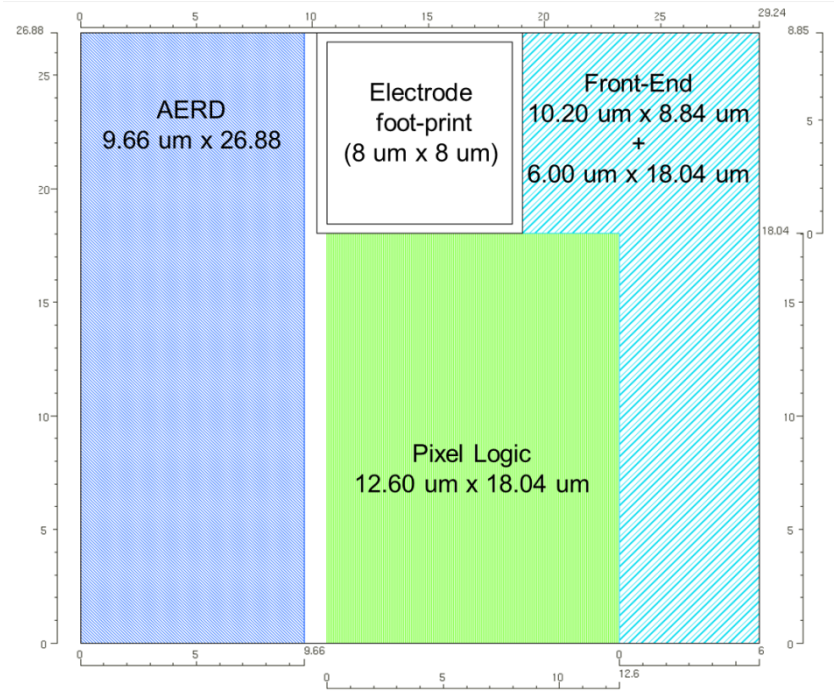
pALPIDE-3 - single pixel floorplan and laoyut

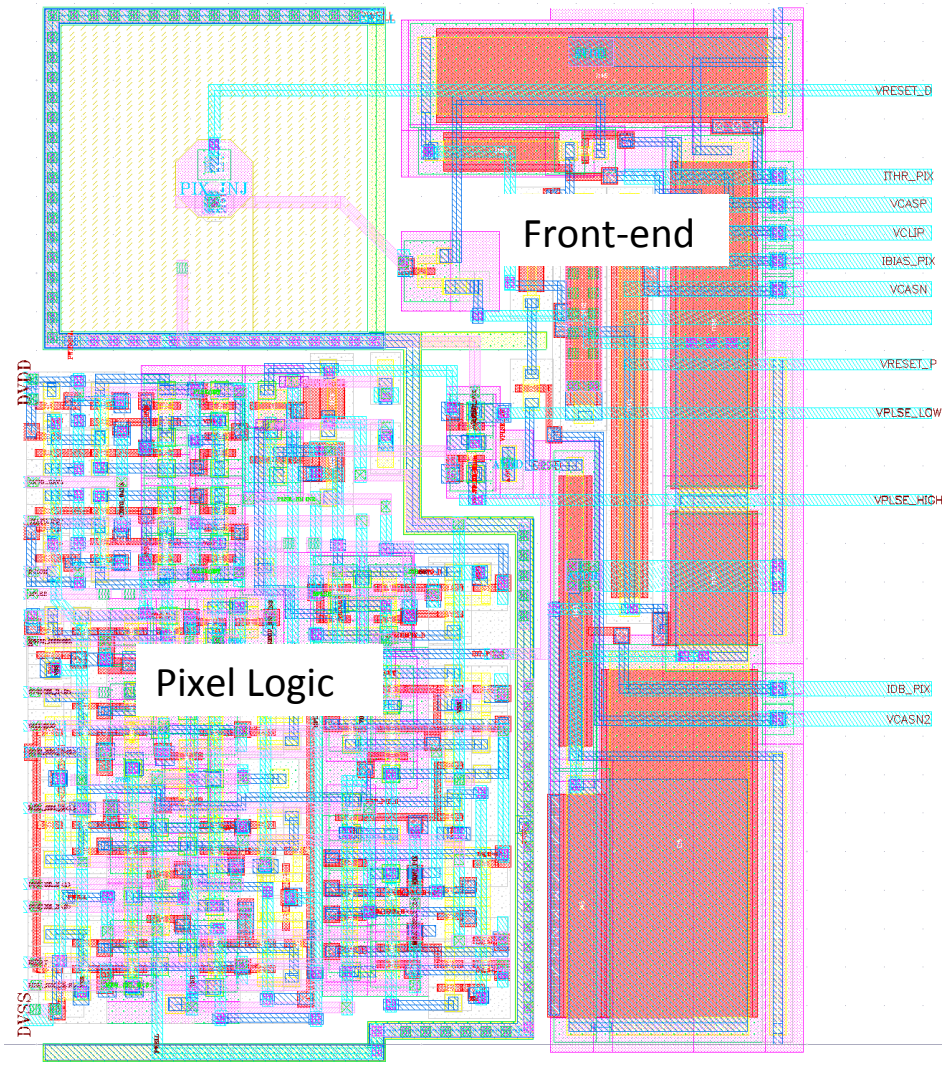
Final pixel size: 29.250 μm × 26.880 μm (w × h)

Collection diode 8 um
- 2 μm nwell width
- nwell-pwell spacing 3 μm

150 transistors

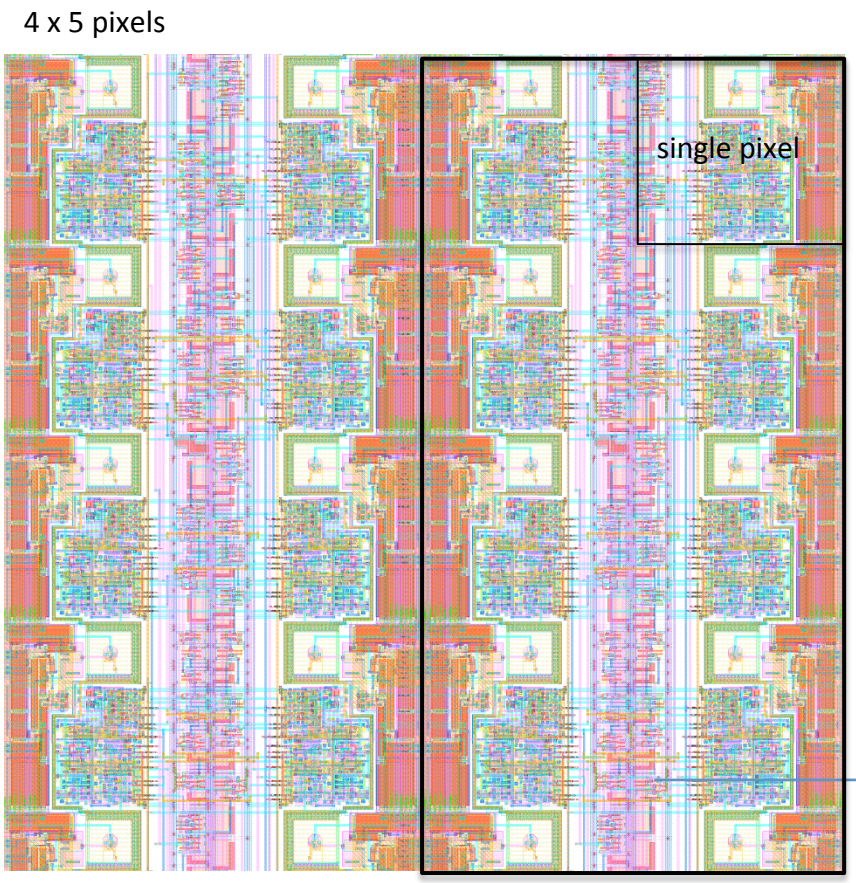
W 29.24 um
H 26.88 um





pALPIDE-3 – matrix layout

Pixel matrix (1024×512) size: 29.952 mm × 13.763 mm



Priority Encoder implemented with standard cells

8 sectors
128 columns/sector
width 3.74 mm/sector

Pixel double column

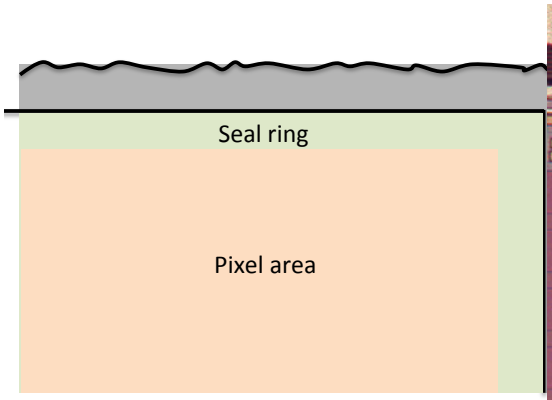
Pixel chip - thinning & dicing

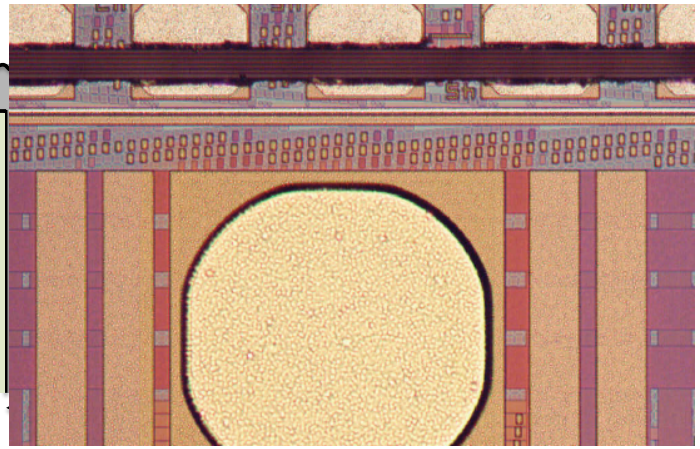
- Diamond wheel pre-dice before grind (DBG) → extended experience (all types of wafers) with Rockwood (France)

- **Main challenge:** picking of large dies after dicing and grinding (50µm thick chip)
  → **Development of special tools/procedures**

Requirements

- Max. extension from the sealring: 25 µm
- Chipout/cracks contained within 25 µm extension region
- No cracks or chip outs touch the seal ring
- Thickness variation: (50 ± < 5) um





Experience (DBG) **with blanks, pad wafers and fully processed CMOS wafers**

Experience to handle **large dies (pALPIDEfs)**

✔ 90 wafers diced and thinned to 50 µm

Status

Market survey in preparation, will be followed by tender in late summer 2015

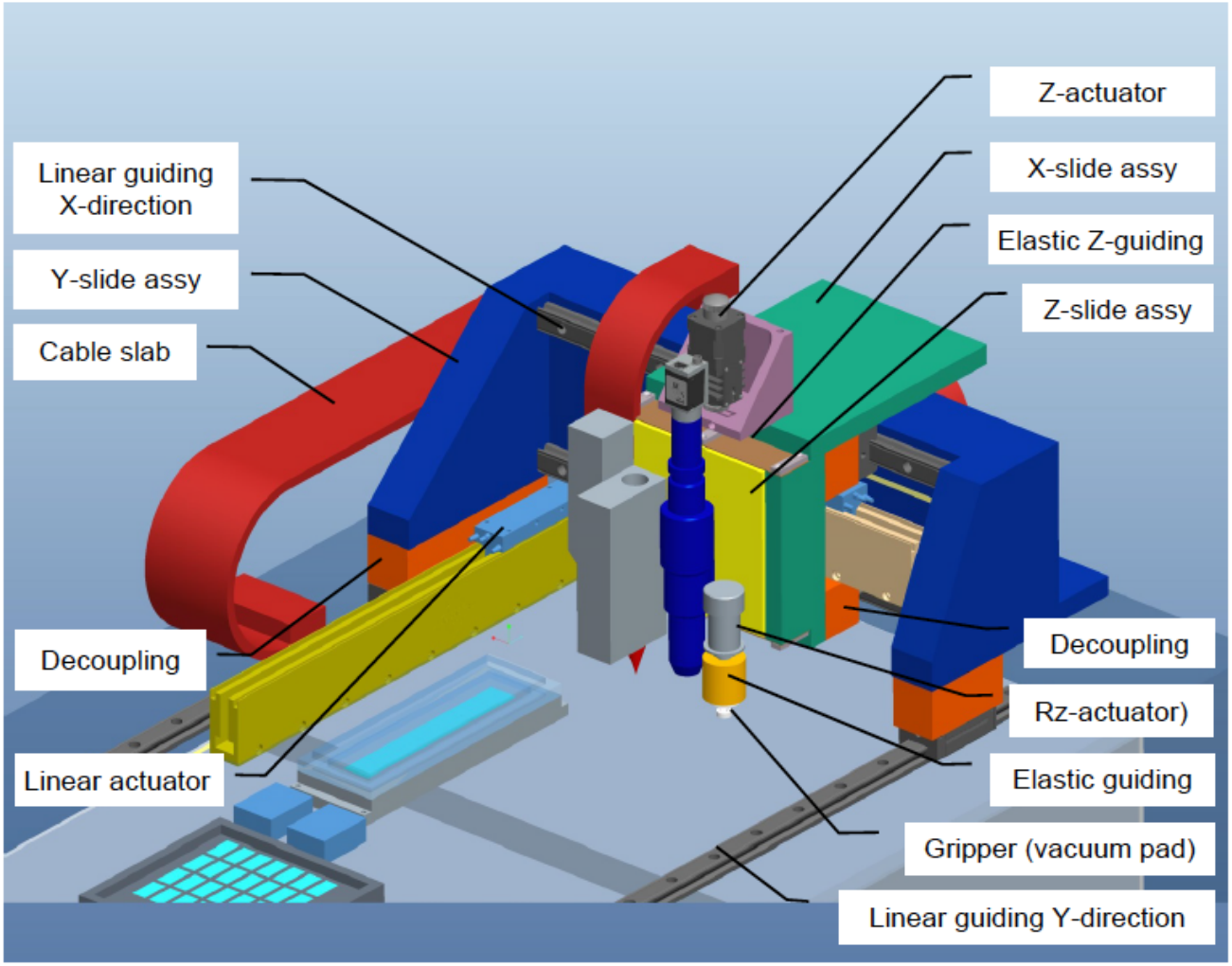
Module Assembly Machine

IB and OB module assembly

- Semi-automatic procedure
- custom machine (specialized company)

Status

- Contract adjudicated to IBS (NL)
- Delivery of first prototype October 15



6 Machines

Inner Barrel & MFT

- CERN

Outer Barrel

- Bari
- Strasbourg
- Liverpool
- Pusan
- Wuhan

Same machines used also for chip testing

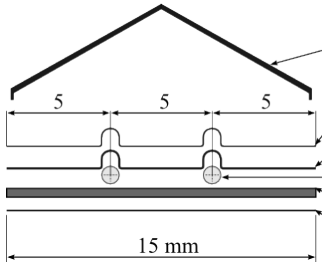
- CERN
- Pusan

Independent machine for chip testing

- Yonsei (Seoul)

Inner Barrel Stave - thermal test

Transversal section:



P_{in}= 1 bar
T_{in}=15.8° C

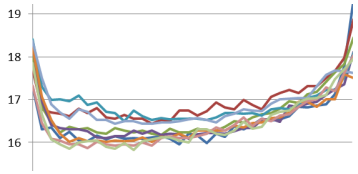
Q= 3 L/h

T_{out}=16.6 °C
P_{out}= 0.7 bar

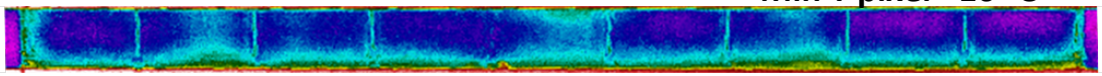
Heating is provided by dummy metalized chip : thickness= 50 µm chip + 20/200 nm Titanium /Platinum

Nominal

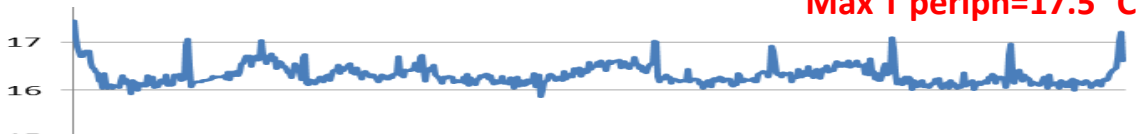
Periphery: 0.145 W/chip
Pixels: 0.03 W/chip



Min T pixel =16° C

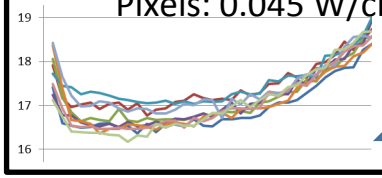


Max T periph=17.5° C

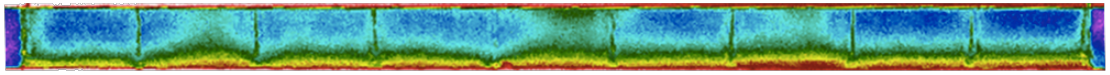


50% safety factor

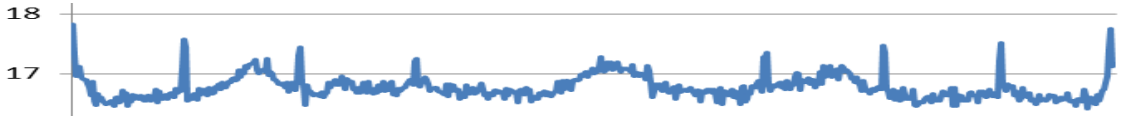
Periphery: 0.217 W/chip
Pixels: 0.045 W/chip



Min T pixel =16.5° C



Max T periph=18.5° C



status
verification of thermal behaviour with
- non uniform power dissipation
- uniform layer of glue

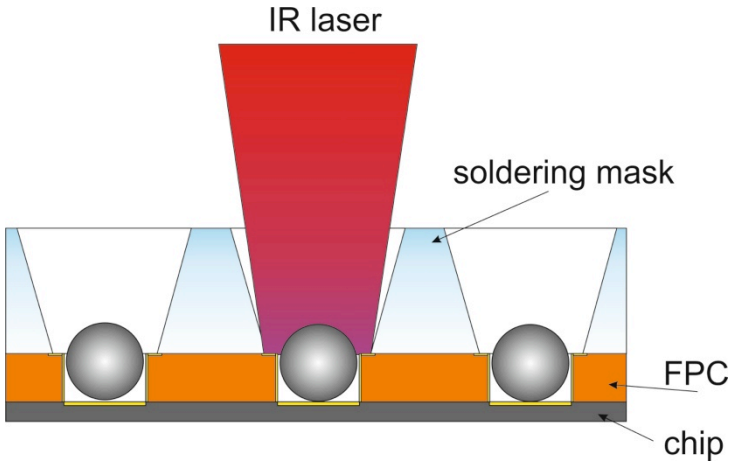
ongoing
verification of thermal behaviour with
- non uniform power dissipation
- no glue at the periphery (2mm) of the chip

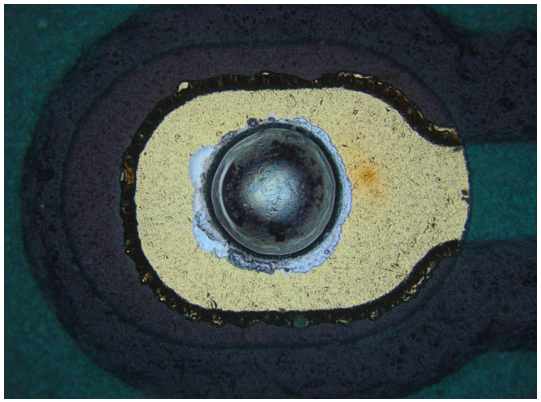
no glue
glue
no glue

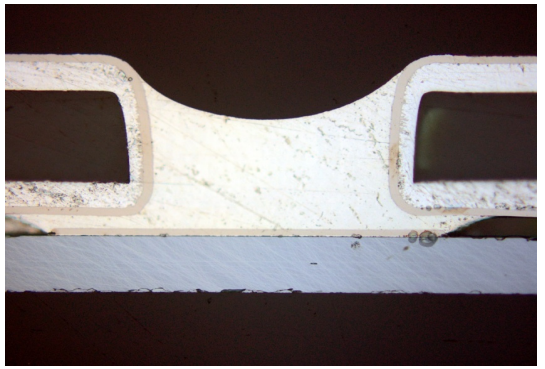
Interconnection of pixel chip to flex PCB

Laser Soldering

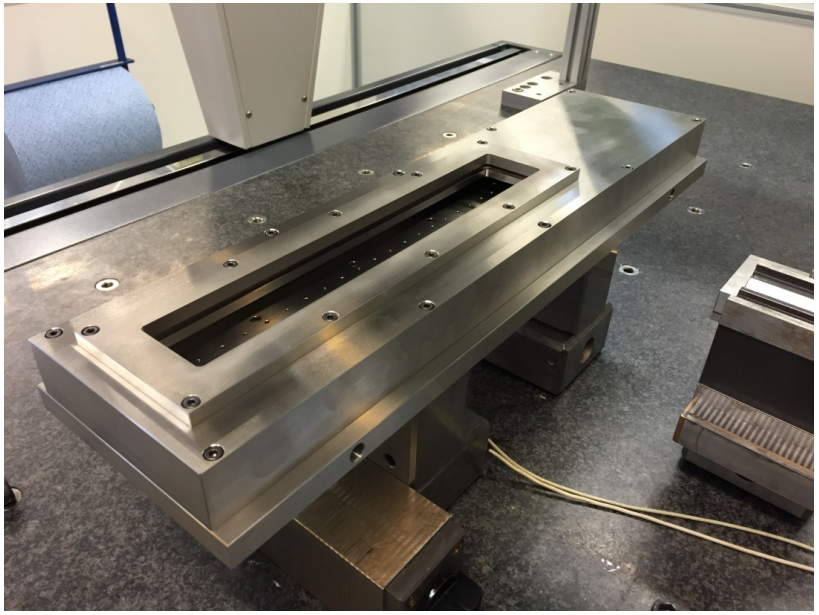
- Flux-less soldering of 200 μm diameter Sn/Ag(96.5/3.5) balls (227 °C melting T) in vacuum (≤10^{-1} mbar)
- IR diode laser, 976 nm, 25 W, 50 mm focal length, 250 μm beam spot size
- Laser power modulated by pyrometer, programmable T profile ensures precise limitation of heating
- Soldering mask (in Macor® or Rubalit ®) used to press FPC on chip and guide soldering balls inside FPC vias
- Solder provides electrical and mechanical connection → no glue



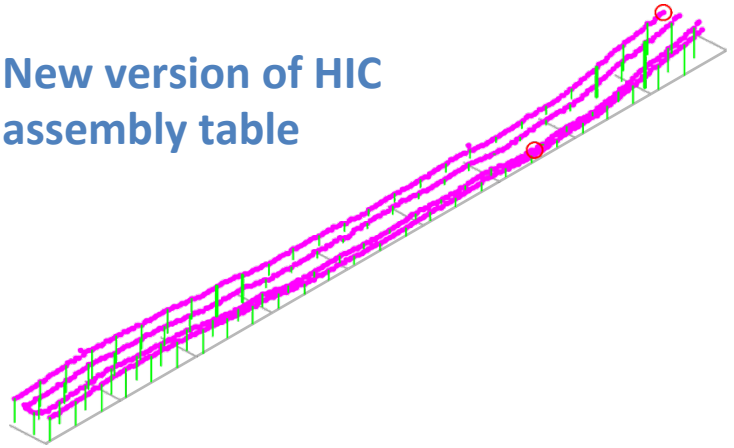




New ITS Layout - Inner Barrel Stave

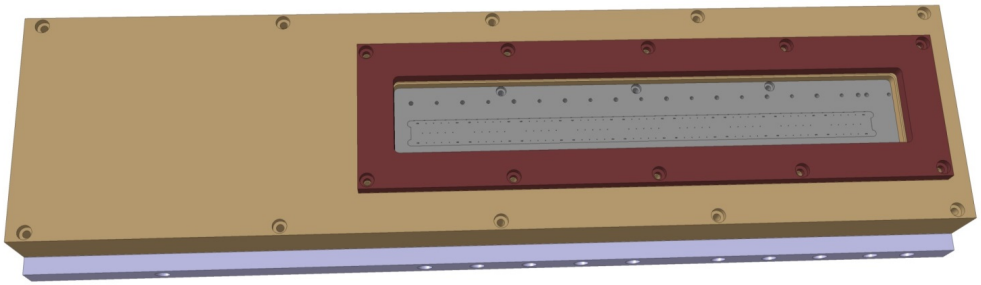


New version of HIC assembly table



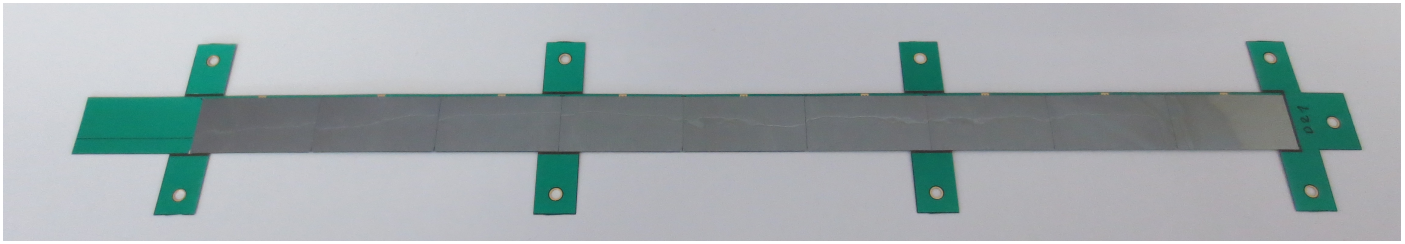
Metrology verification

Vacuum chuck planarity: < 15 μm



Chuck planarity (already good for the current version) will be further improved for final version:

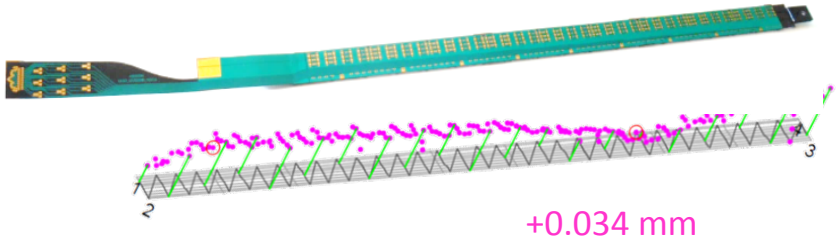
- target: ~ 5 μm



Inner Barrel Stave

Stave HIC+ Space frame assembly

Dimensional accuracy

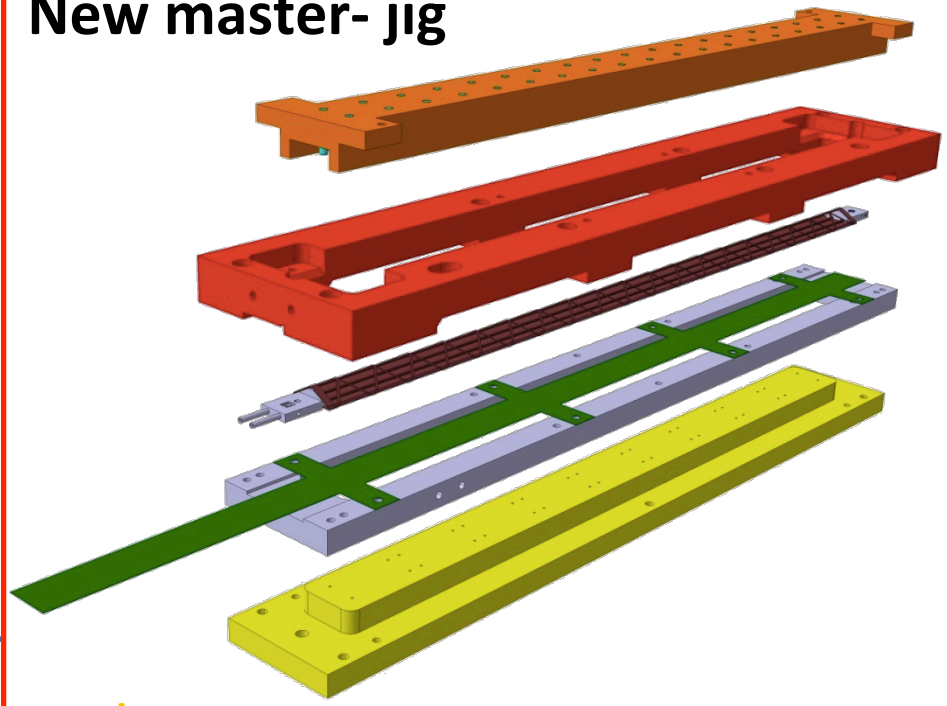


+0.034 mm
- 0.034 mm

status

New master jig (ready) will improve stave accuracy

New master- jig



ongoing

New master jig produced and shipped from the Company, arrival at CERN this week

Space frame production

status

Available : n. 20 spaceframe

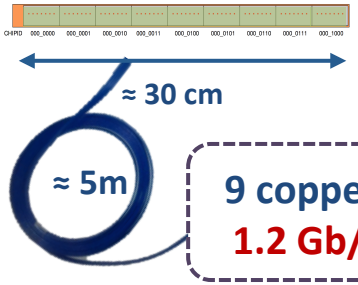
Ongoing

pre-production continues to prepare for final series production

Layout and curing process optimization: planarity achieved ± 0,028÷0,040 mm

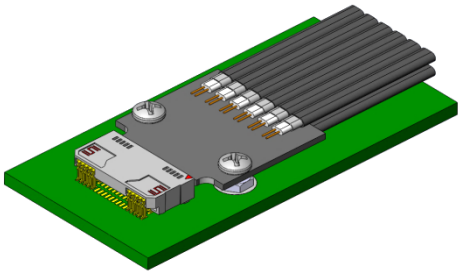
Readout Unit – system overview

Inner layers (0, 1, 2) staves:
9 masters for each stave

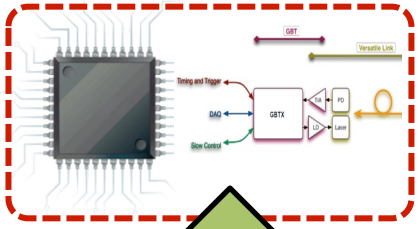


9 copper pairs, 1.2 Gb/s each

12 pairs Twinax copper assembly

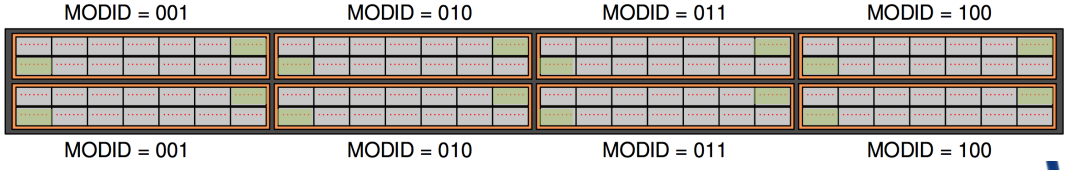


Readout Unit



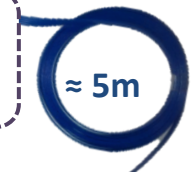
CRU

Mid layers (3, 4) staves: 8 modules per stave, 2 master each

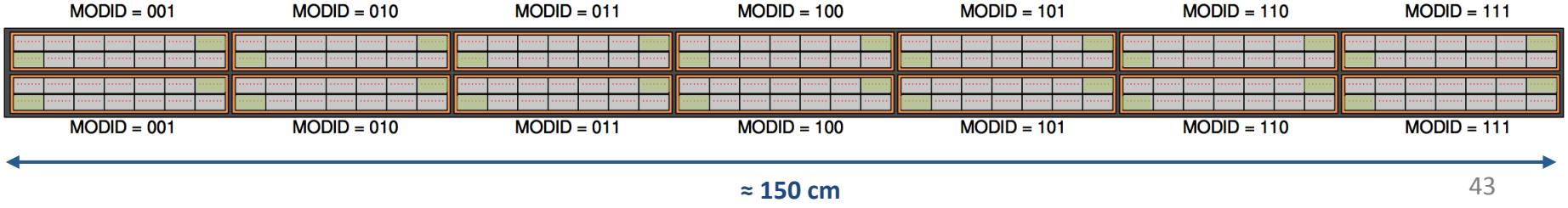


16 copper pairs, 400 Mb/s each

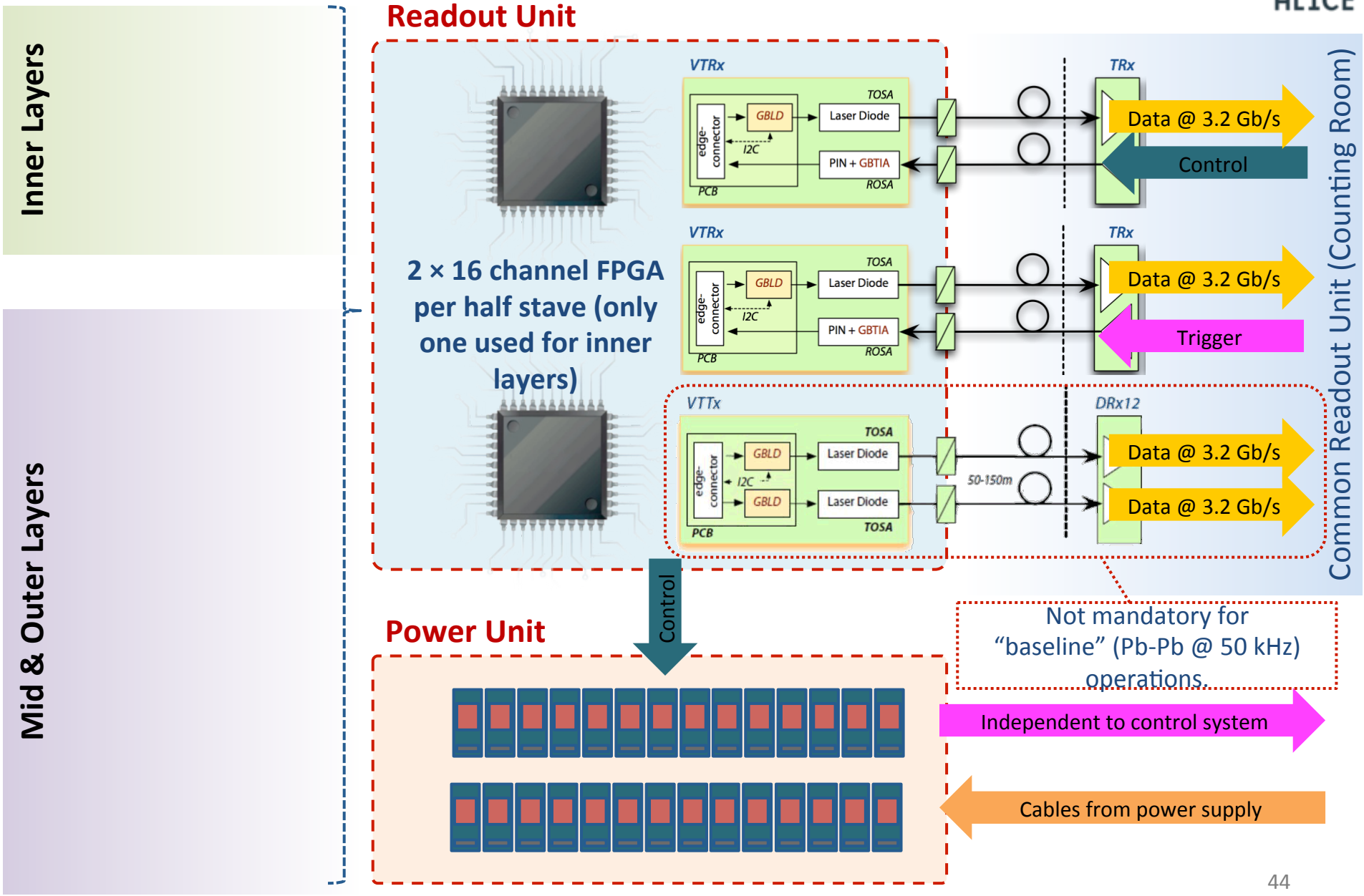
28 copper pairs, 400 Mb/s each



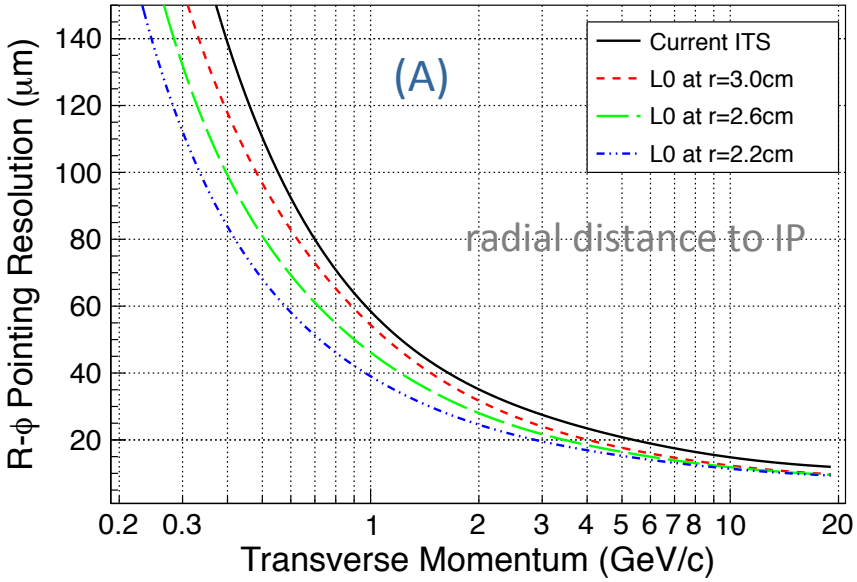
Outer layers (5, 6) staves: 14 modules per stave, 2 master each

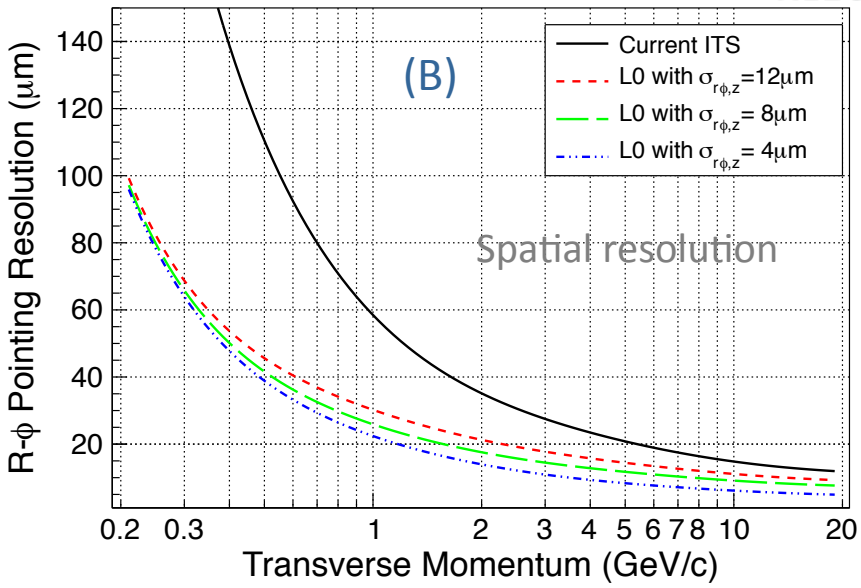


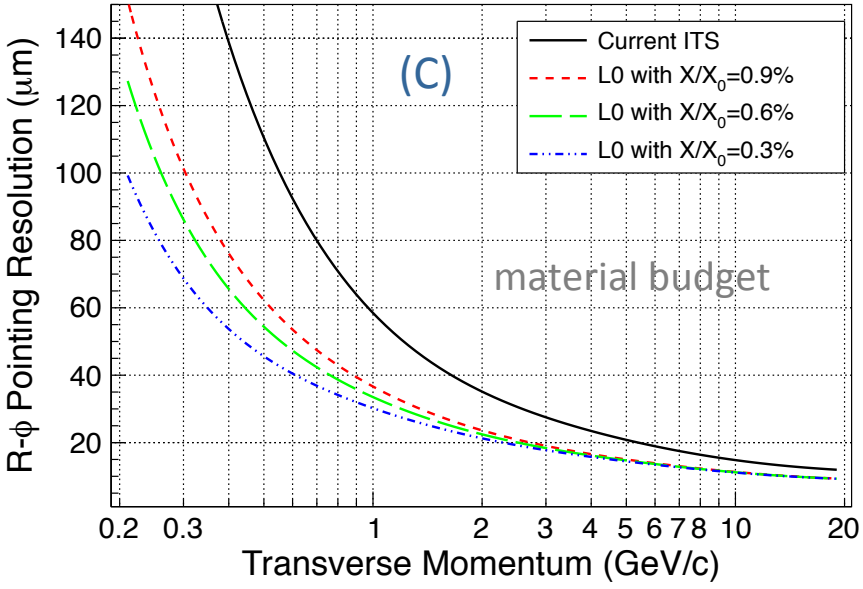
Readout – single modular Readout Unit for all layers



Impact parameter studies (ALICE ITS Upgrade)







- Current ALICE ITS
  - ✧ radial position of first layer: 39mm
  - ✧ x/X_0: 1.14% per layer
  - ✧ spatial resolution (r-phi): 12 μm
- A) current ITS + L0: x/X0 = 0.3%, res.=4μm;
- B) current ITS + L0: r = 22mm, x/X_0 = 0.3%;
- C) current ITS + L0: r = 22mm, x/X_0 = 0.3%;

ALICE ITS Upgrade CDR, CERN-LHCC-2012-12