SAMPA

Digital Block

Status & Progress

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SAMPA - DSP

- In the last months from the Last Design review the following tasks have been realized in relation to the SAMPA digital block:

- Source / Functionality
  - Implementation of the configuration block for the new TPC channel reordering scheme
  - Changes in the data pipeline
  - Corrections in the filters (Baseline correction)
    - Arithmetic
    - Exceptions

  - Implementation of the triple module redundancy (TMR) on:
    - channel data-path configurations
    - filter pipeline configuration
    - full global chip registers are now TMR protected too
    - Full TMR status on Next Slide

  - Implementation of the Analog Baseline trimming registers and outputs
  - Linting of the source code
  - Changes in the Neighbor module datapath and new memory configuration
    - Sync routine to search for the first packet
    - Hamming corrections of the received headers

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- On Implementation / Backend Side
  - Changes in the Neighbor module datapath and new memory configuration
    - Reuse of existing IP s to make the module
      - Header memory (same as channels)
      - Data, made of 4 instances of a previous requested memory 1K

  - Implementation of the DFT (Design for Test) scheme
  - Implementation of a faster sync module for the neighbor input to meeting timming
  - Initial floorplan of the updated sources were performed
    - Tried out in Backend flow
    - New floorplan developed and adapted to the new requisites
      - TMR
      - TPC - Serial out reorder

- Adoption of the New TSMC13 design kit release from VCAD in 2015 in the new runs

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- Tasks In progress now:

- In relation to source:
  - Changes in the data pipeline
    - Remove data jams before the buffer memory
      - Faster data write needed
      - Will trigger the removal of several FIFOs
        - Save power and area
      - Several changes in DFU, ZSU and Ring Buffer triggered
        - More work...
        - Very difficult to test and validate
          - Long simulations
          - Not possible to multi process...
    - Changes in the clock domains triggered by the data flow too

- Development of the test-benches
  - Filters
  - Full chip dataflow

- Running backend flow for the new codes and providing feedback to the development stage

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- TMR STATUS
  - Complete implemented
  - Easy TMR select in the modules
    - Filters Datapath
      - TMR not enable in the moment
        - Area limitations

1	Percent	Comment	TMR type
pt_logic	100		intermodular
wr_pt_logic	100		intermodular
rd_pt_logic	100		intermodular
ring_buffer	100		only syncs
rb_input	100		
rb_ouput	100		
serialout	100		
clkgen	100		intermodular
heartbeat	100		intermodular
empty	100		intermodular
sync	100		intermodular
synchronizer	100		intermodular
synchronizer_ae	100		intermodular
synchronizer_re_toggle	100		intermodular
globrgu	100		module
lcore	100		only syncs
tmr_reg	100		intermodular
trg_gen	100		only syncs
bxcount	100		intermodular
evtman	100		intermodular
rstman	100		intermodular
NBRB	-	no flipflops	
nb_input	100		intermodular
NBinput	100		intermodular
neighbor	100		only syncs
holder	100		intermodular
dfu	100		intermodular
zsu	100		intermodular
bc3	100		intermodular
bc2	100		intermodular
IIRfilter	-	only data flow	
presamples	100		intermodular
chrgu	100		module

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- Most Important Pending Tasks:

- In relation to source:

  1-) Changes in Data formatting unit -> ring buffer -> Memory interface

  2-) Neighbor block
  - we have timing issues there, and this need to be fixed to work at least in half of the input freq
    - multicycling

  3-) ERRORs block...
  - We should account for errors and problems found in TMR, state machines and in the memory test scheme

  4-) implement a quickly and simple memory test (checkerboard) when the test mode start

  5-) BC1
  - we want to make some improvement on VPD, like did in BC2...

  6-) DS (tail cancelation)
  - The team is not sure about the correctness of the filter, it is almost there, but probably need some small fixes
    - Feed back over one case of use should be important (Set of Coefficients)

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- Most Important Pending Tasks:

  7-) “toppic 0”, Testbenches for:

  - BC1
  - BC2
  - BC3 (probably concluded, 100% coverage, used random data)
  - ZSU (In progress, ~70% coverage at the moment)
  - DFU
  - DS

  - Full data flow of the chip
    - In progress
      - Very slow

  - Full data flow in gate level
    - First results from backend are ready
      - Starting to adapt the TBWs for this
        - Even slower to run

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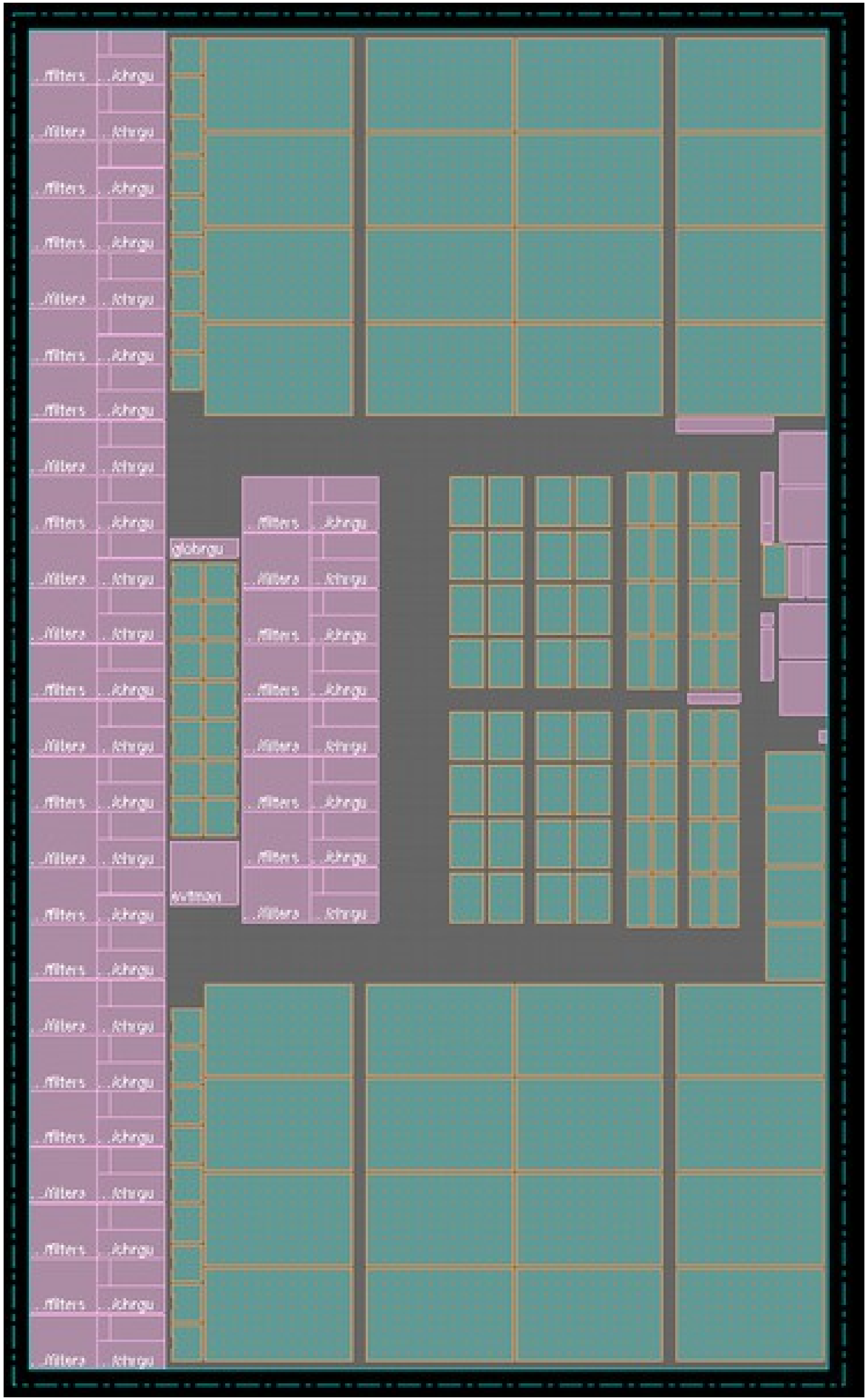
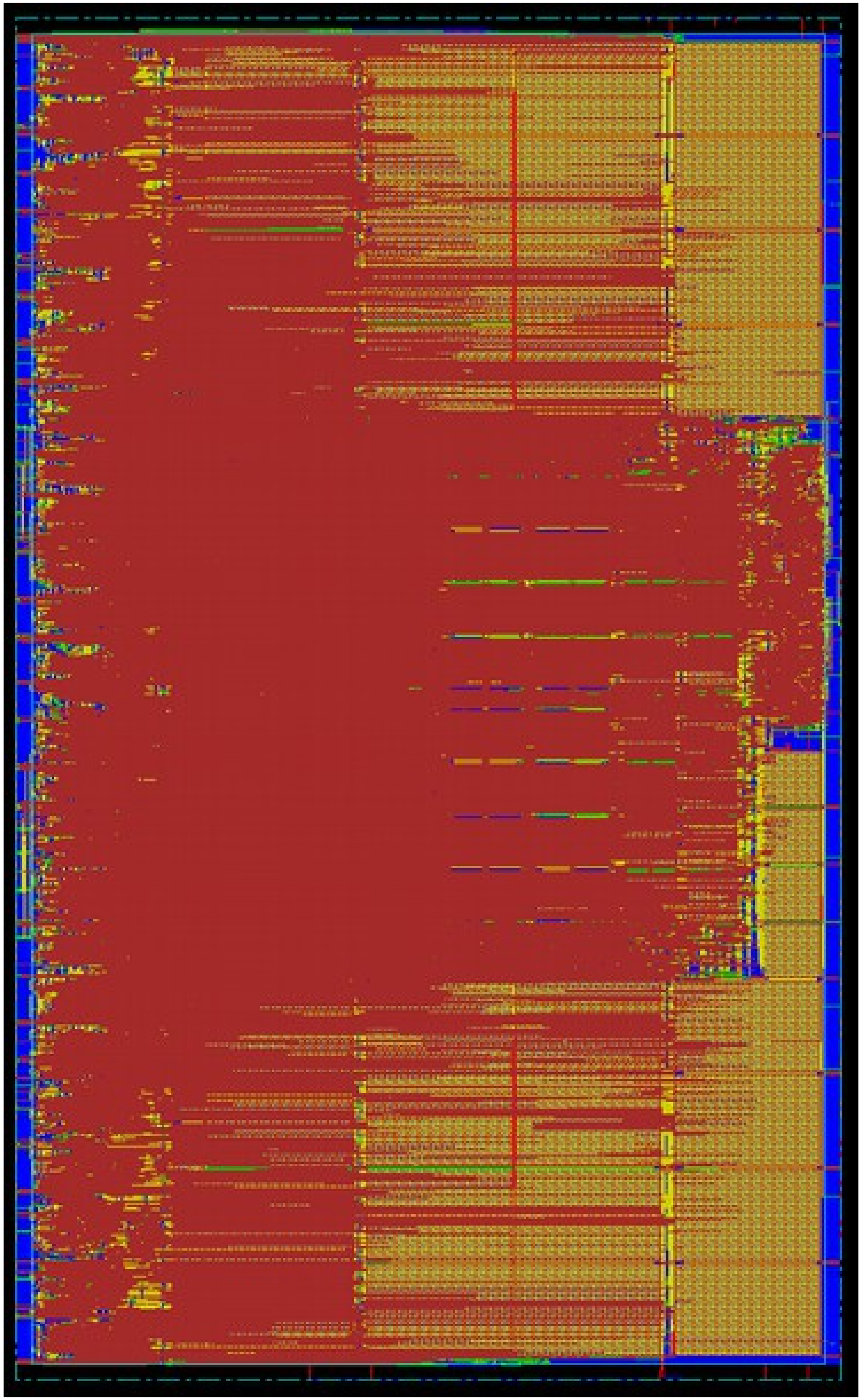
- New proposed Floorplan



SAMPA - DSP

- The Layout
  - Actual version of SAMPA
- At left:
  - 32 X 10b bus
    - ADC Connections
- Data flows to the center right of the chip
  - 4X serial outputs at 320Mbps
- Full layout made with
  - Last version of the code
    - Including TPC serial out reordering
    - MCH header suppression
    - Corrections on MCH Neighbor input



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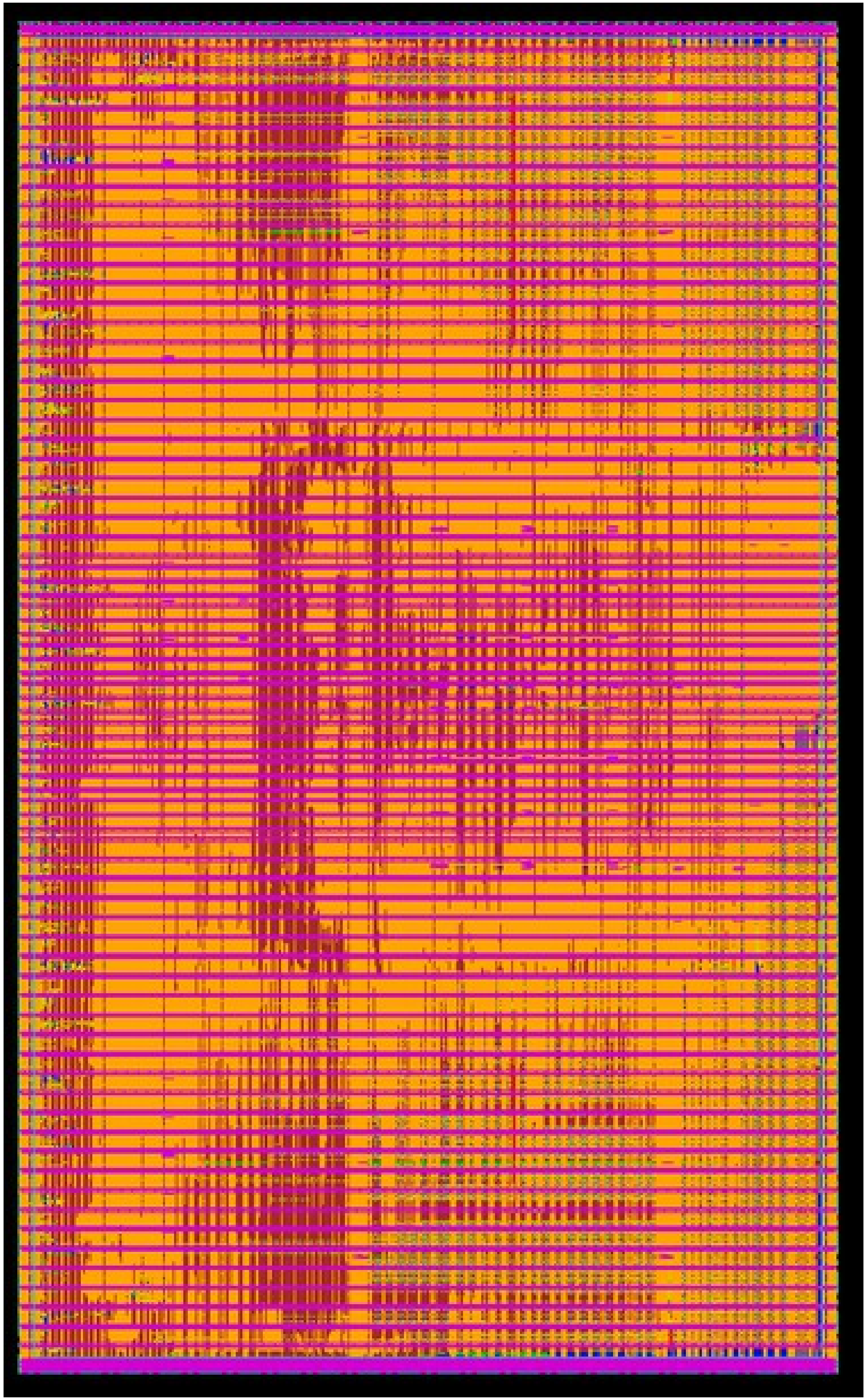
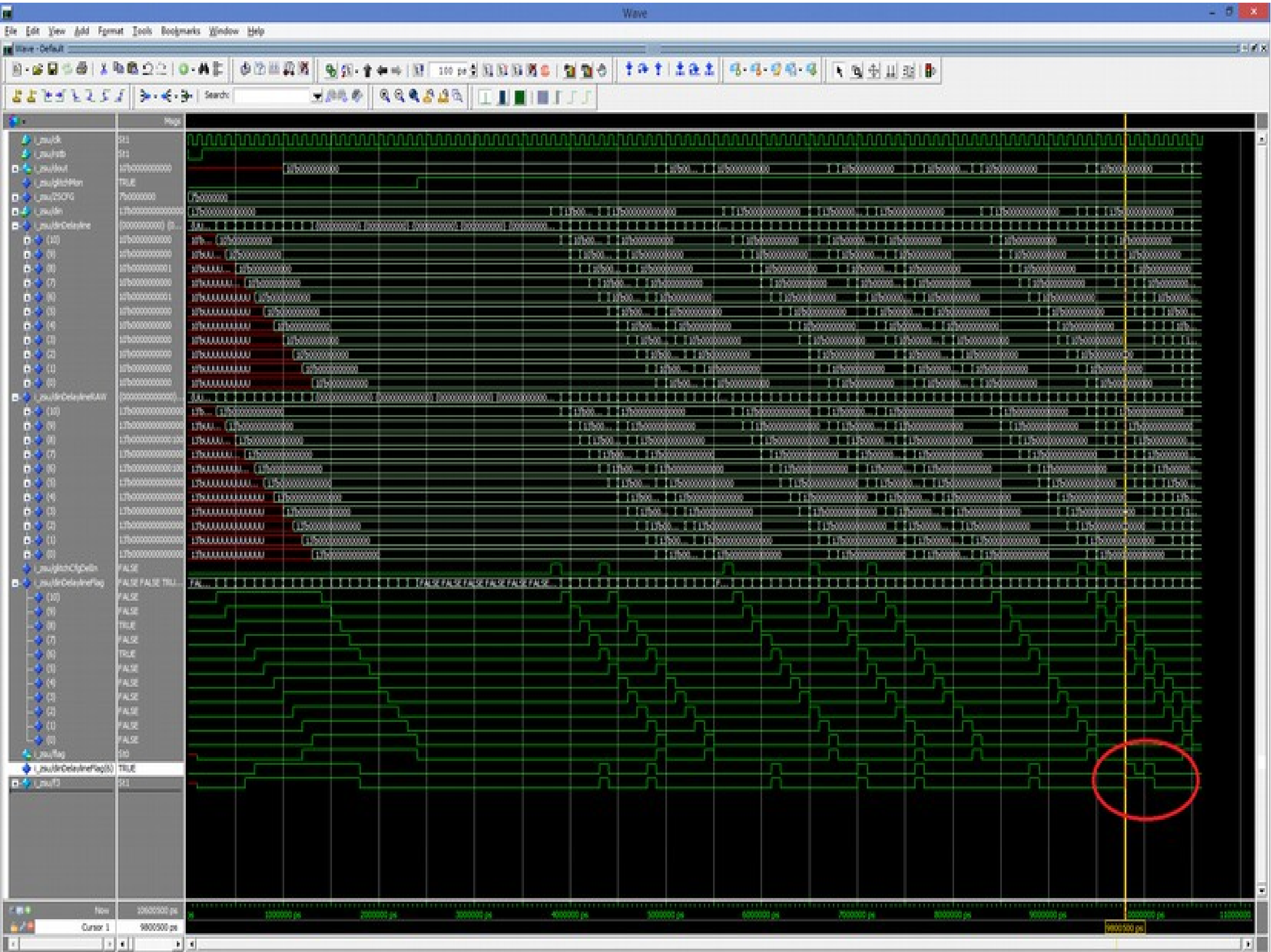


•Small Question about zero suppression to TPC / MCH:

Should we suppress two single samples spaced by one sample under the threshold?

By now you have a configurable zero suppression scheme that can filter glitches of:
a-) one sample above the threshold
b-) two
c-) the glitch filter can be disabled setting this number of samples to zero

*This point was found making a comparison with the filters on SALTRO, that implement this auto merging of one sample
→ this imply that two shots separated by one will be taken as a 3 sample cluster, generating more one Time count mark and one Cluster size mark, or even a two word cluster sum result.


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
100 ps
Search:
Msgs
i_zsu/clk St1
i_zsu/rstb St1
i_zsu/dout
i_zsu/glitchMon TRUE
i_zsu/ZSCFG
i_zsu/din
i_zsu/dinDelayline
(10)
(9)
(8)
(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
i_zsu/dinDelaylineRAW
(10)
(9)
(8)
(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
i_zsu/glitchCfgDelIn FALSE
i_zsu/dinDelaylineFlag FALSE FALSE TRU...
(10) FALSE
(9) FALSE
(8) TRUE
(7) FALSE
(6) TRUE
(5) FALSE
(4) FALSE
(3) FALSE
(2) FALSE
(1) FALSE
(0) FALSE
i_zsu/flag
i_zsu/dinDelaylineFlag(6) TRUE
i_zsu/f3 St1
FALSE FALSE FALSE FALSE FALSE FALSE...
Now
Cursor 1
1000000 ps
2000000 ps
3000000 ps
4000000 ps
5000000 ps
6000000 ps
7000000 ps
8000000 ps
9000000 ps
10000000 ps
11000000

Thanks