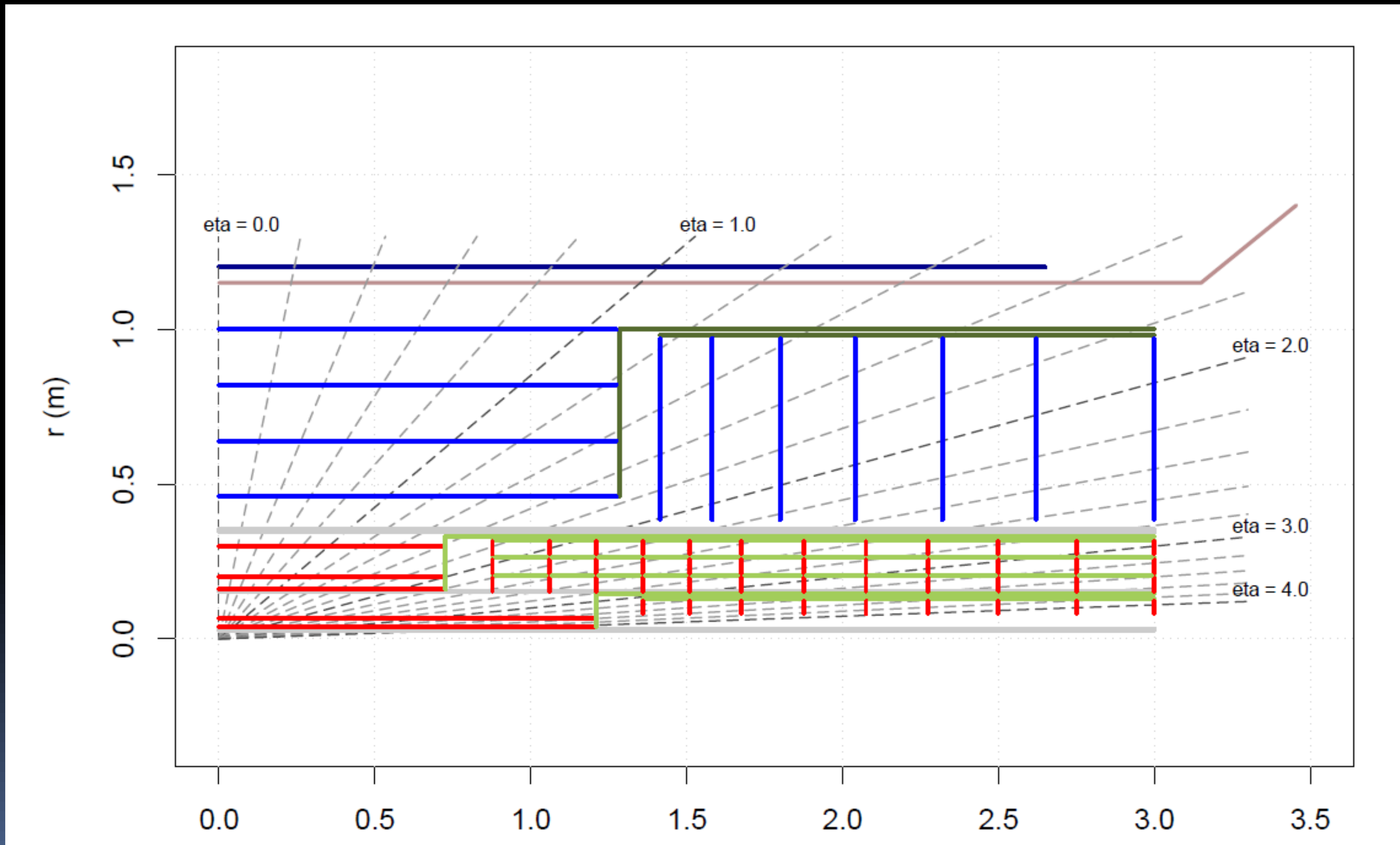
P. Morettini

Extension of the pixel volume

5 Pixel / 4 Strip layers

- The LTF is starting the simulation of layouts like this one. Still very preliminary…



5th / 6th Pixel Layers

Layer 6 is just an option, not costed for the moment.

- Barrel

	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6
Radius	4 cm	8 cm	14 cm	20 cm	30 cm	34 cm
Length in z	120 cm	120 cm	70 cm	70 cm	70 cm	70 cm
# of modules	960 D	960	980	1540	2100	2380

- Rings (just a guess, tracking requirements in the VF region not well defined)

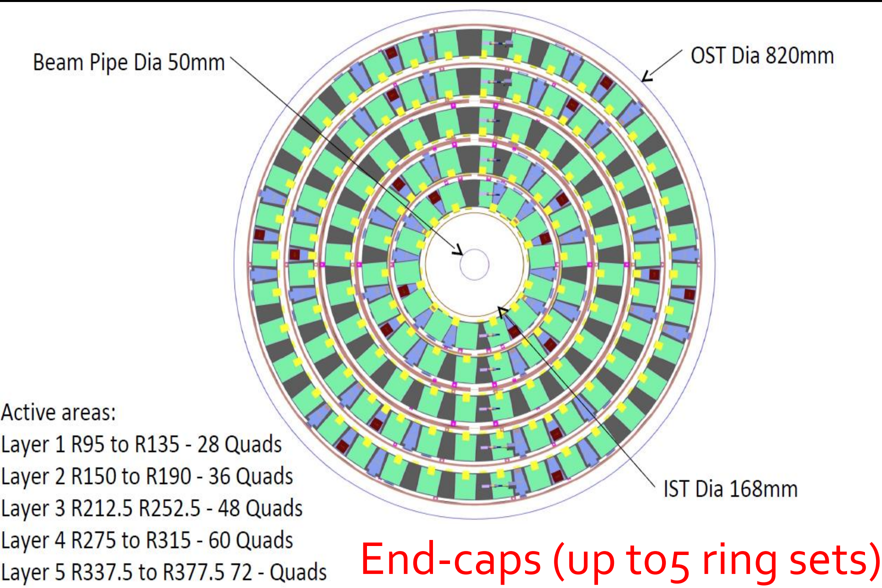
	Set 1	Set 2	Set 3	Set 4
Radius	15-19 cm	21-25 cm	27.5-31.5 cm	33.7-37.7 cm
# of rings	18	24	24	24
# of modules	648	1152	1440	1728

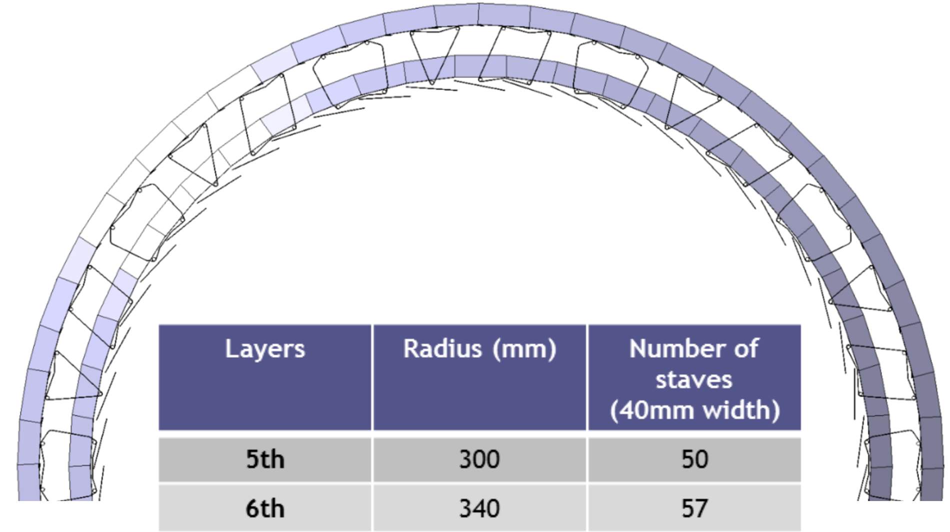
- Pixel envelope = 38 cm
- Layer 5: ~4000 more modules, extra cost in hybrid technology ~ 12 Mchf

First drawings

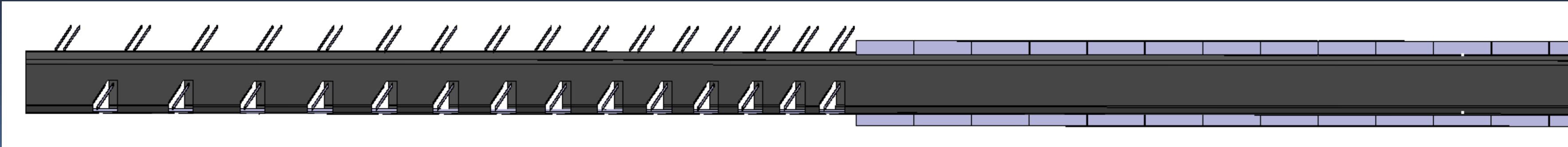
Some initial design of possible support structures is already in progress…

Several optimizations are possible in the barrel/ring transition.





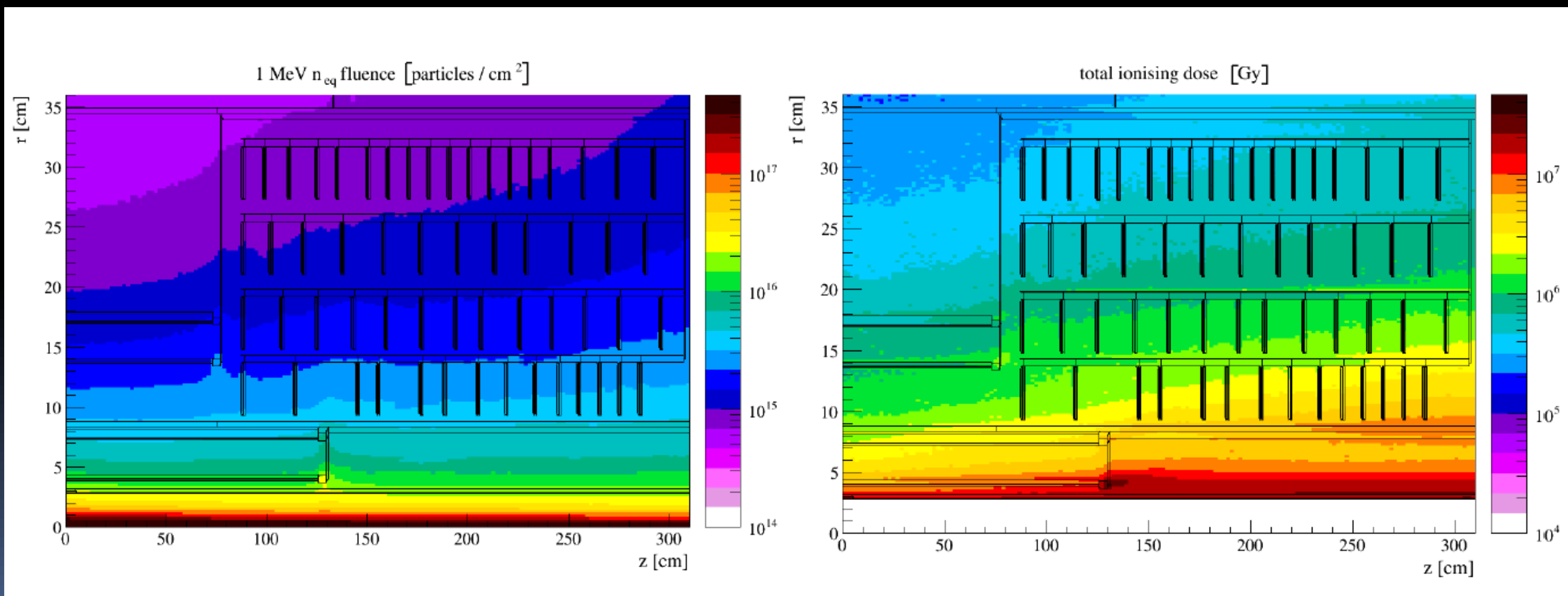
Layers	Radius (mm)	Number of staves (40mm width)
5th	300	50
6th	340	57



Expected doses

Layer 5/6 are in a relatively quiet environment:

- 5-7 10^{14} 1 MeV n_{eq}
- 30-50 Mrad



Thermal Run-Away Plots at T_{evap_max} = -30°C

PLANAR [0.46 W/cm² @ -25°C @ 2.6E16 n_{eq}/cm²]

3D [0.08 W/cm² @ -25°C @ 2.6E16 n_{eq}/cm²]

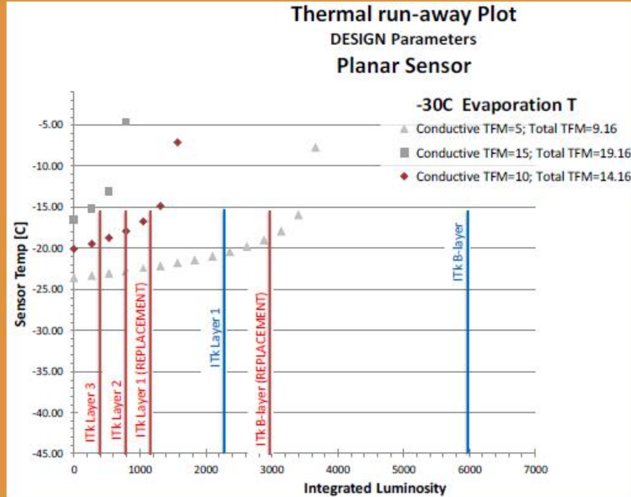
DESIGN

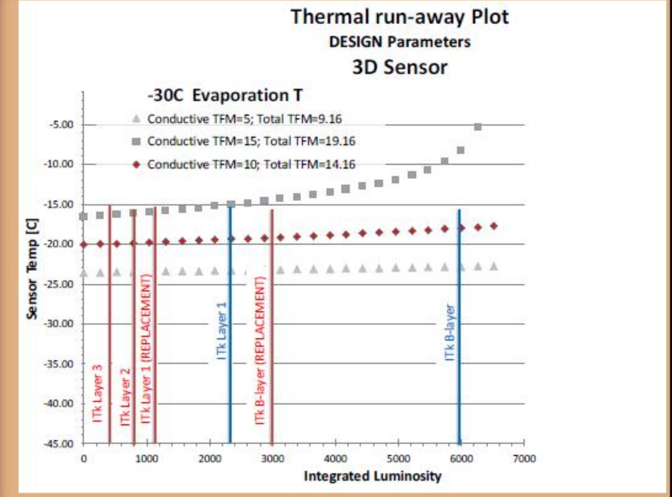
$\mathcal{L}$= 6000 fb^{-1}

FE_{power} = 0.7 W/cm²

T_{evap_max}= -30°C

HTC_{CO2}= 6000 $W.m^{-2}.K^{-1}$





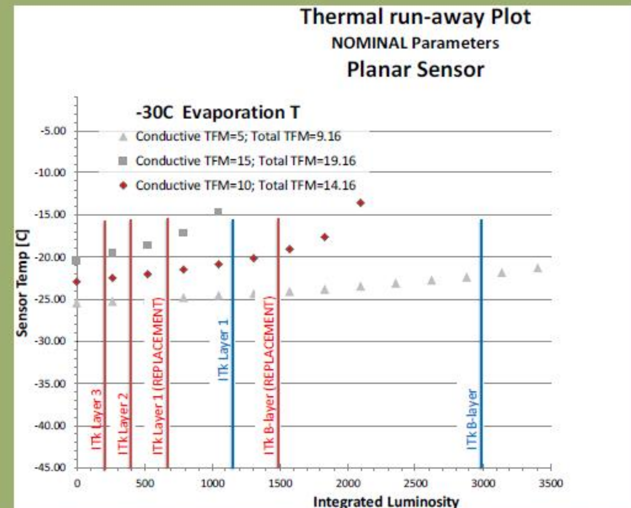
NOMINAL

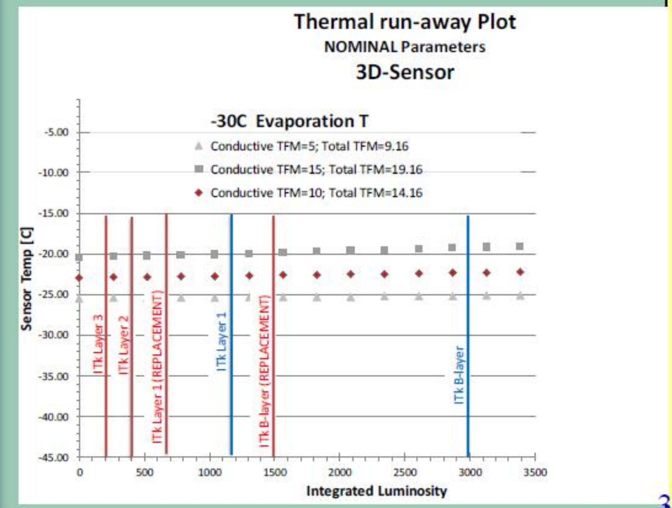
$\mathcal{L}$= 3000 fb^{-1}

FE_{power} = 0.5 W/cm²

T_{evap_max}= -30°C

HTC_{CO2}= 6000 $W.m^{-2}.K^{-1}$





D. Giugni

Readout requirements

Need to verify with new simulations. Present estimates, mainly LoI based, at 1 Mhz LVL0 readout are:

	R	Hit rate	Raw data rate	BW per FE chip
Layer 1	4 cm	2 Ghit/(s*cm²)	2.7 Gb/s	5 Gb/s
Layer 2	8 cm	820 Mhit/(s*cm²)	1.1 Gb/s	2 Gb/s
Layer 3	14 cm	400 Mhit/(s*cm²)	520 Mb/s	1 Gb/s
Layer 4	20 cm	250 Mhit/(s*cm²)	350 Mb/s	640 Mb/s
Layer 5	30 cm	150 Mhit/(s*cm²)	200 Mb/s	480 Mb/s
Layer 6	34 cm	120 Mhit/(s*cm²)	170 Mb/s	320 Mb/s

The difference between the raw data rate and the requested BW is to limit transmission latency for track trigger.

Problems to address

- Cost: removing one strip layer saves ~10 MCHF.
- Production: more work, but there are may groups interested in Pixel, and more than 12 labs are interested in being qualified as production sites.
- Bump-bonding: a possible bottleneck; ~5 vendors can be qualified, but the process is intrinsically slow and prone problems that may reduce the rate.

Possible solutions to explore:

- More BB vendors; possibility to do flip-chip in labs.
- CMOS passive sensors should be less expensive
- Active CMOS sensors could alleviate the BB problem, using different bonding technogy/vendor.
- MAPS : no BB at all and large cost reduction.

Timeline

- June 23 LTF Workshop – June 29 costing : first ideas on production plans (hybrid detector); consolidation of costing of non-module components.
- End of November : review of the Strip TDR preparation; Pixel should define the date of the TDR (move it to Q2 2018?), define milestones for TDR preparation, illustrate a solid production plan.
- Beginning of 2016 : definition of the layout; local support options still possible, but the position and the number of barrels and rings should be defined, as well as a baseline for service routing and integration strategy.
- End 2016: should have clear ideas about the technologies that could be available for the production, and start converging on a design for the TDR. Demonstrator programs should be ready by then.