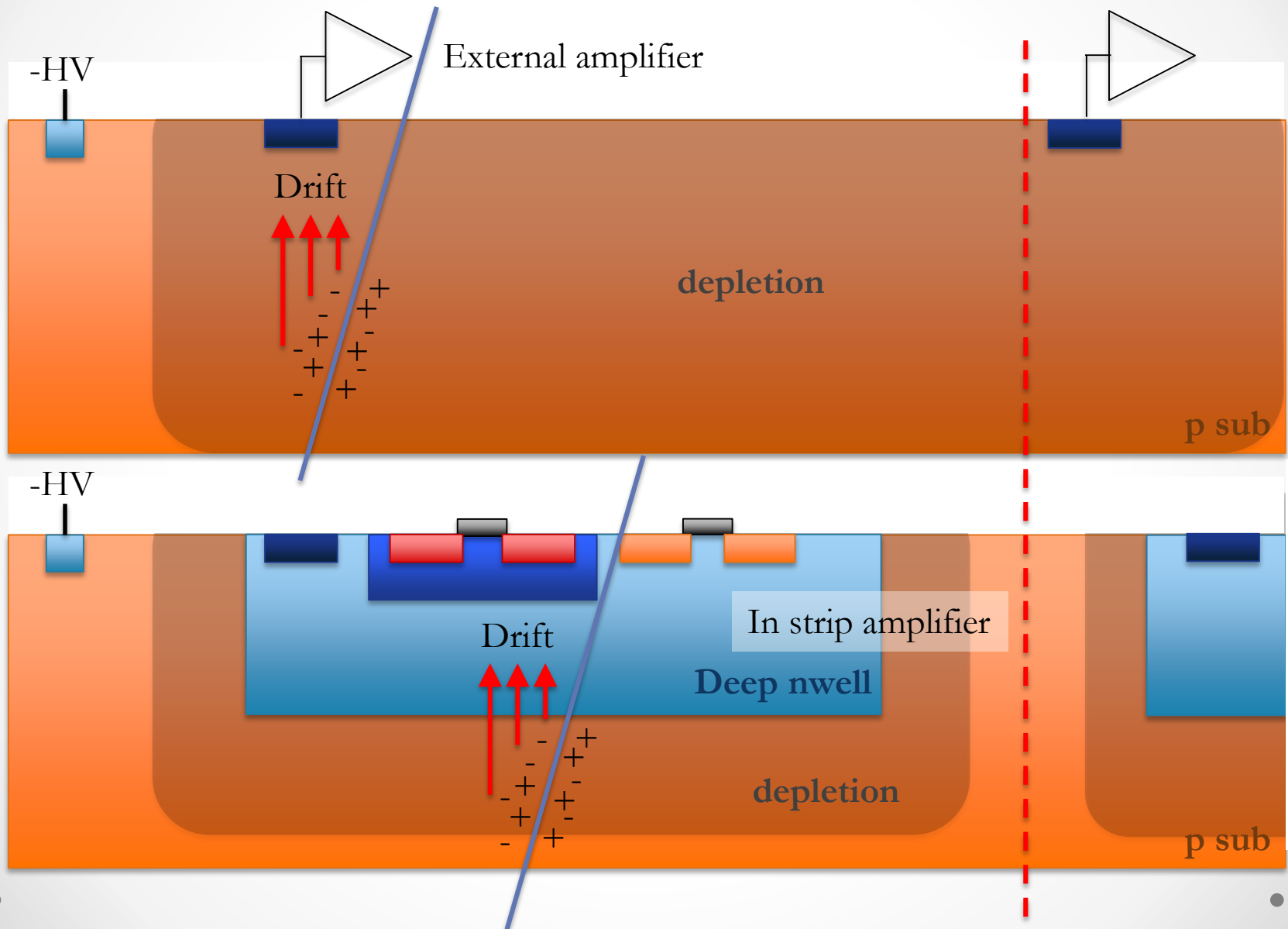


Developments in CMOS for strip detectors

H. Grabas for the CHESS collaboration

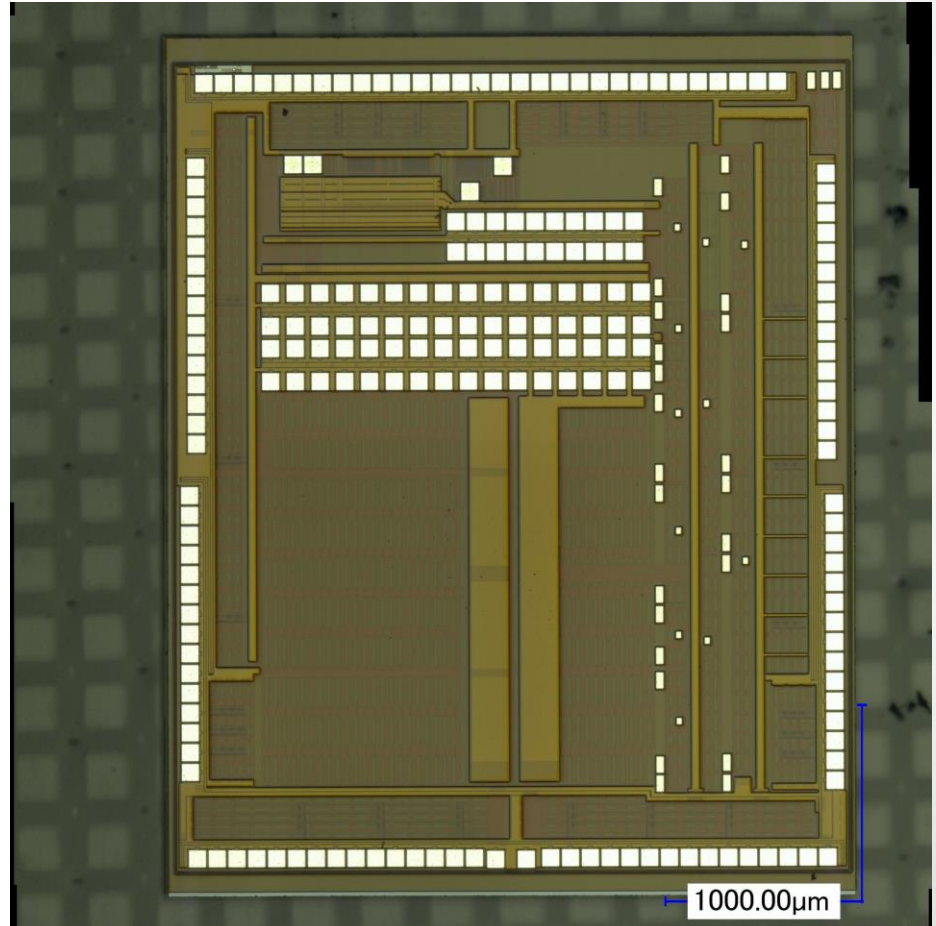
UCSC – SLAC – KIT

HV-CMOS for strips



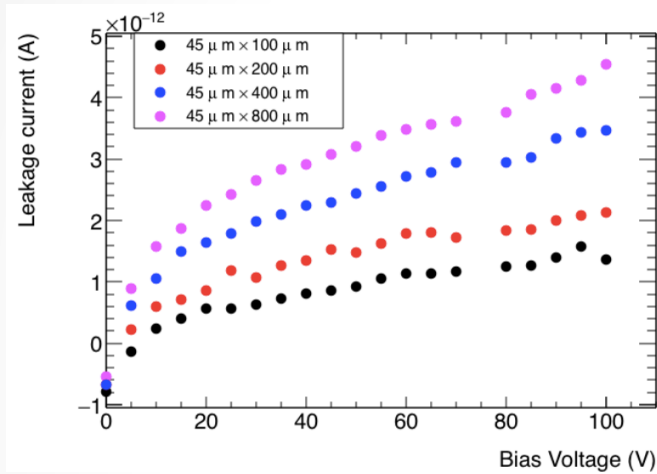
Demonstrator: CHES-1

- Multiple active and passive HVCMOS pixel matrices
 - Allows to measure capacitance/resistance
 - Response signal, even for low signals (i.e. real particles)
- Large array to allow for charge deposition measurement (depletion depth, 2x2[mm] in size)
- Small passive array to support edge-TCT (Laser)
- Component array to study radiation defects in transistors/caps/diodes

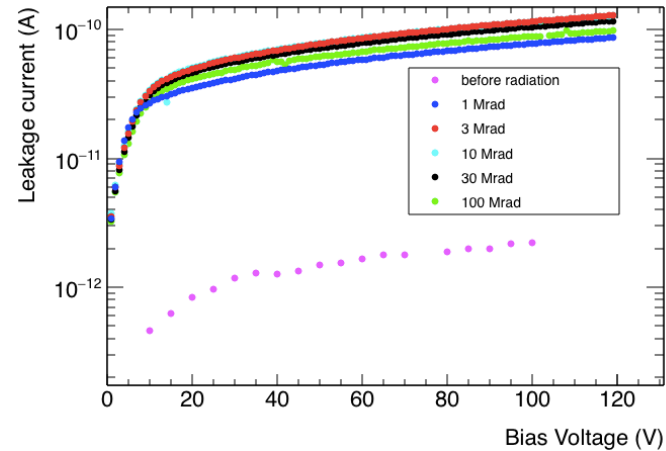


CHESS1 results

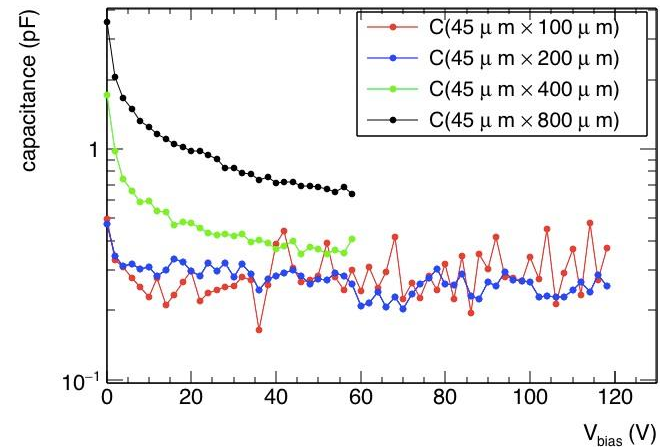
- Leakage at 100V is:
 - 0.15nA/strip before IR



6.4nA /strip after IR (100MRad gamma)



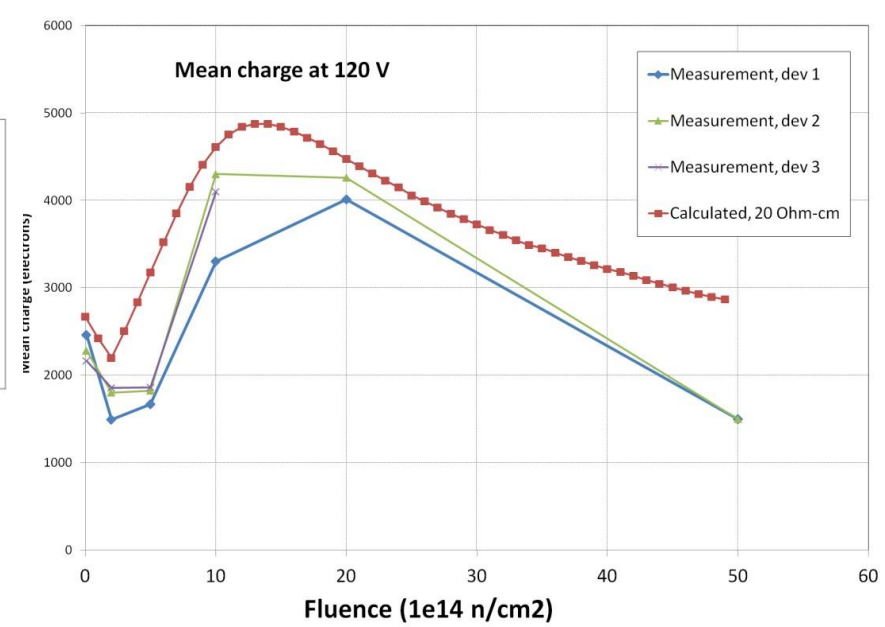
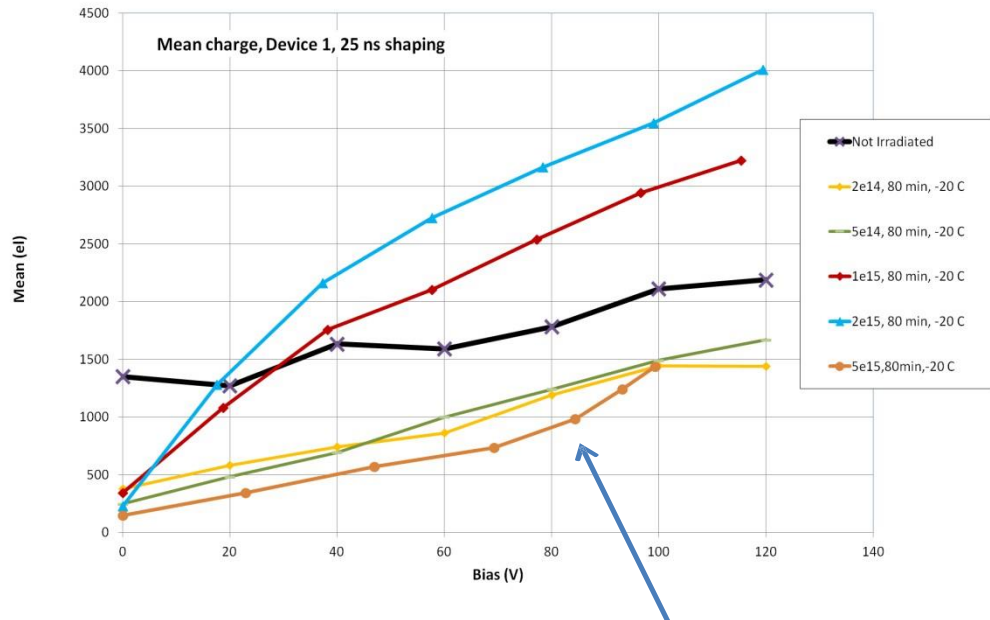
- 45 x 800 μm pixels capacitance:
 - 400fF at 100V



- Amplifier noise:
 - ~ 80 to $100 e^-$ of noise

CHES1 charge collection

Sr-90 electrons, mean charge, 25 ns shaping



□ Large drop of collected charge after $5 \times 10^{15} \text{ n/cm}^2$

- Initial acceptor removal finished
- Depleted region narrows because of radiation induced defects

Evolution of N_{eff} with fluence:

$$N_{eff} = N_{eff0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$$

Initial concentration

acceptor removal

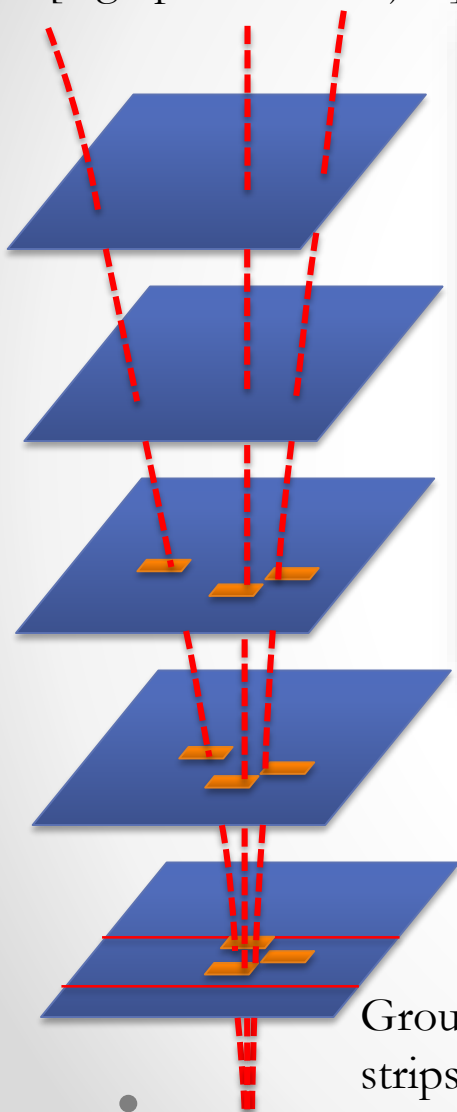
Radiation introduced deep acceptors (stable damage): $g \sim 0.02 \text{ cm}^{-1}$

Towards CHESS2

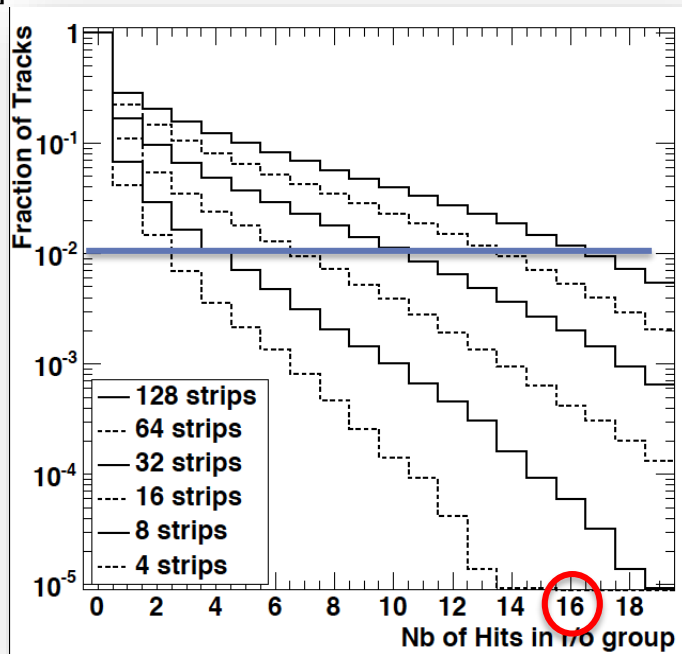
- CHESS-2 will be the second demonstrators for both HR & HV-CMOS for strip sensor R&D.
- CHESS1 and HV_Strip1 have proven that HV_CMOS can be used for Strip detector
- CHESS-2 is meant to demonstrate that HR & HV_CMOS can cope with the physics at HL-LHC.
- CHESS-2 will integrate full length strips + readout.
- Design done in collaboration with UCSC, SLAC and Ivan Peric.
- Slides are for HV-CMOS but a CHESS-2 equivalent will be submitted as well in the HR-CMOS process by Renato, following the same specifications.

Strip detector hit occupancy

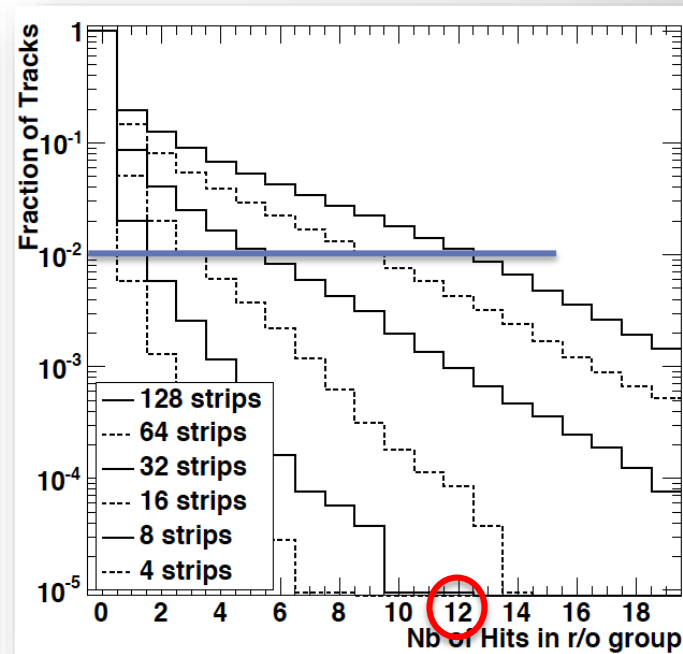
Sim. Marco Battaglia
[high p_T $H \rightarrow bb$ jets]



First strip layer



Fifth strip layer



Consistent with simulation by Nick Edwards:

| Layer | 68% Clusters | 95% Clusters | 99% Clusters | 68% Hits | 95% Hits | 99% Hits |
|---------|--------------|--------------|--------------|----------|----------|----------|
| Layer 0 | 1 | 2 | 4 | 3 | 8 | 17 |
| Layer 1 | 1 | 2 | 4 | 3 | 8 | 17 |
| Layer 2 | 1 | 2 | 4 | 3 | 8 | 16 |
| Layer 3 | 1 | 2 | 4 | 3 | 8 | 16 |
| Layer 4 | 1 | 2 | 4 | 3 | 9 | 19 |

Table 1: Number of hits/clusters corresponding to the 95% and 99% quantiles of the distribution of hits/clusters per SCT chip in $t\bar{t}$ events with $\mu = 140$. Chips with zero hits/clusters are not included in the calculation.

Strip detector hit encoding

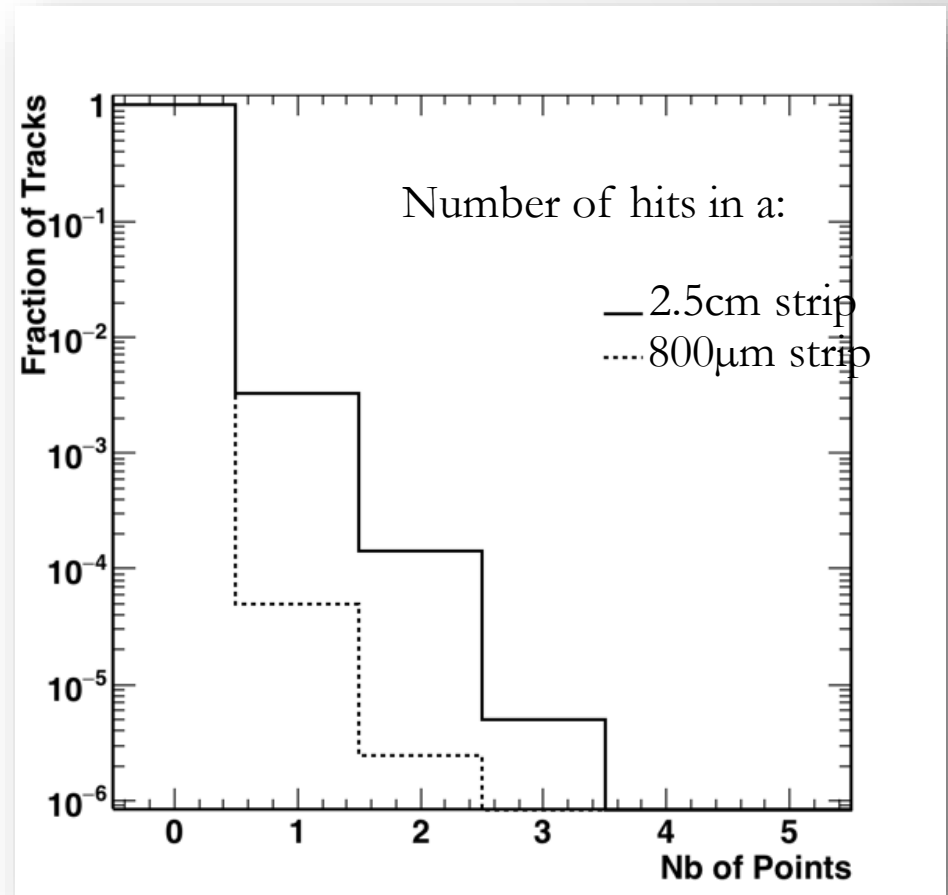
- 1% average occupancy of the detector is not an issue.
- **No de-randomizer in the sensor.**
- Need to be able to cope with bursts of ~ 20 hits in the detector.
- Contrary to the Baseline Sensor, we cannot retain all the hits in the CHESS detector.
- Need to encode strips hits.
- Need to minimize number of wirebonds.
- Can send 8 words at 320MHz per 25ns bunch crossing (no buffering in chip).

| Nb of strips in group | Wirebonds needed | Wirebonds per strip | Max. number of hits @320MHz |
|-----------------------|-----------------------------|---------------------|-----------------------------|
| 512 | $5 + 1 + 9 = 15$ | 0.03 | 8 |
| 256 | $(5 + 1 + 8) \times 2 = 24$ | 0.045 | 16 |
| 128 | $(5 + 1 + 7) \times 4 = 52$ | 0.1 | 32 |
| 64 | $(5 + 1 + 6) \times 8 = 96$ | 0.18 | 64 |

- We are going to 128 strips group retaining 8 hit for each group.

Single strip hit selection

- Simulation by Marco Battaglia shows that double hit in ζ direction is highly suppressed.
 - $\sim 2 \cdot 10^{-3}$ probability
- Will be investigated in the high pile-up environment (should be ok given the low occupancy).



Baseline to HV-CMOS

Baseline

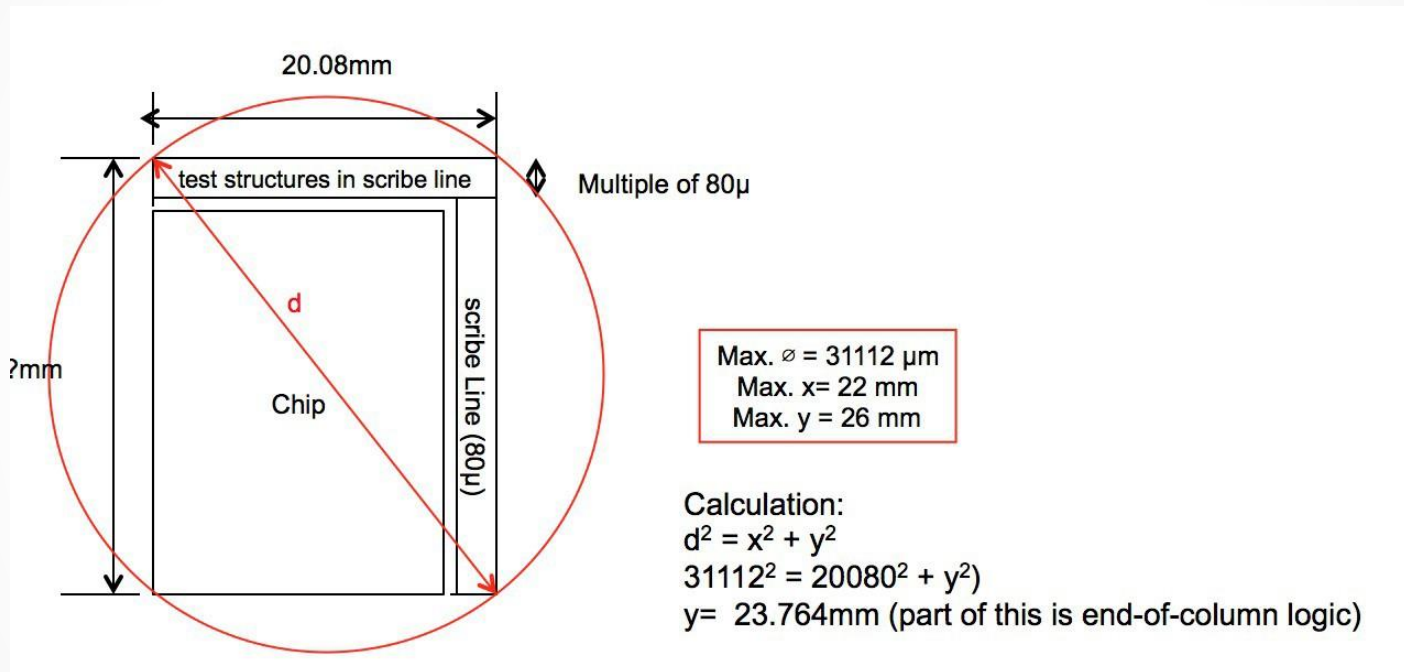
| | |
|--------------------|---------------------------|
| | |
| Number of strip | 256 (for comparable area) |
| Strip pitch | 75 μ m |
| Strip segmentation | None |
| | |
| Number of sensor | 2 (stereo) |
| Output signal | Analog |
| Max. nb. of hits | 256/ b. crossing |
| Nb. of wirebonds | 1/strip |

HV-CMOS

| | |
|--------------------|---------------------------|
| | |
| Number of strips | 512 |
| Strip pitch | 40 μ m |
| Strip segmentation | 32 |
| Segment length | 800 μ m |
| Number of sensor | 1 (can be thinned) |
| Output signal | Encoded Digital |
| Max. nb. Of hits | 32/ b. crossing |
| Nb. of wirebonds | 0.1/strip |

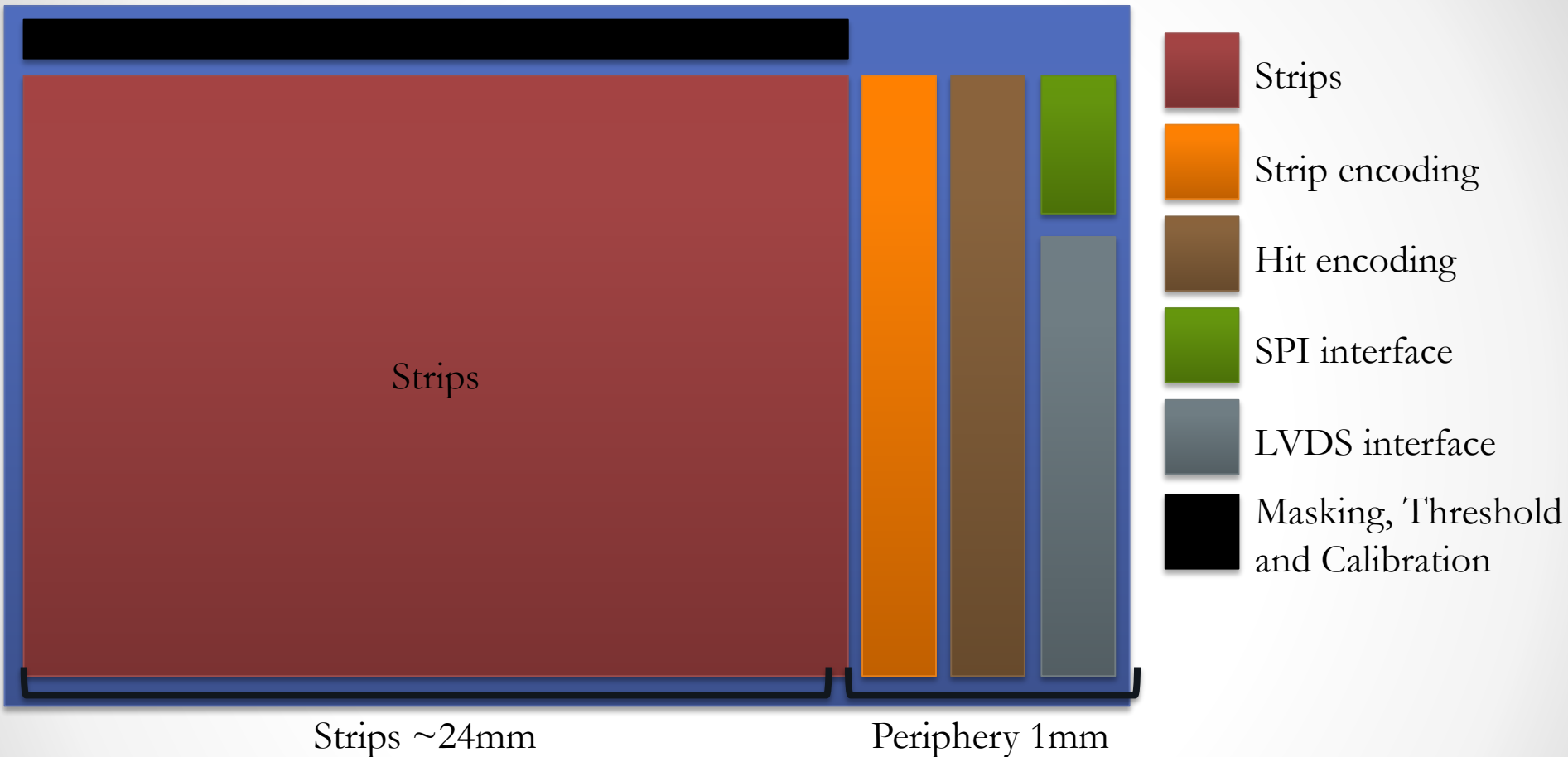
Sensor dimension

- Ideally we would like a 20mm x 25mm sensor (to be compatible with the baseline Strip sensor).



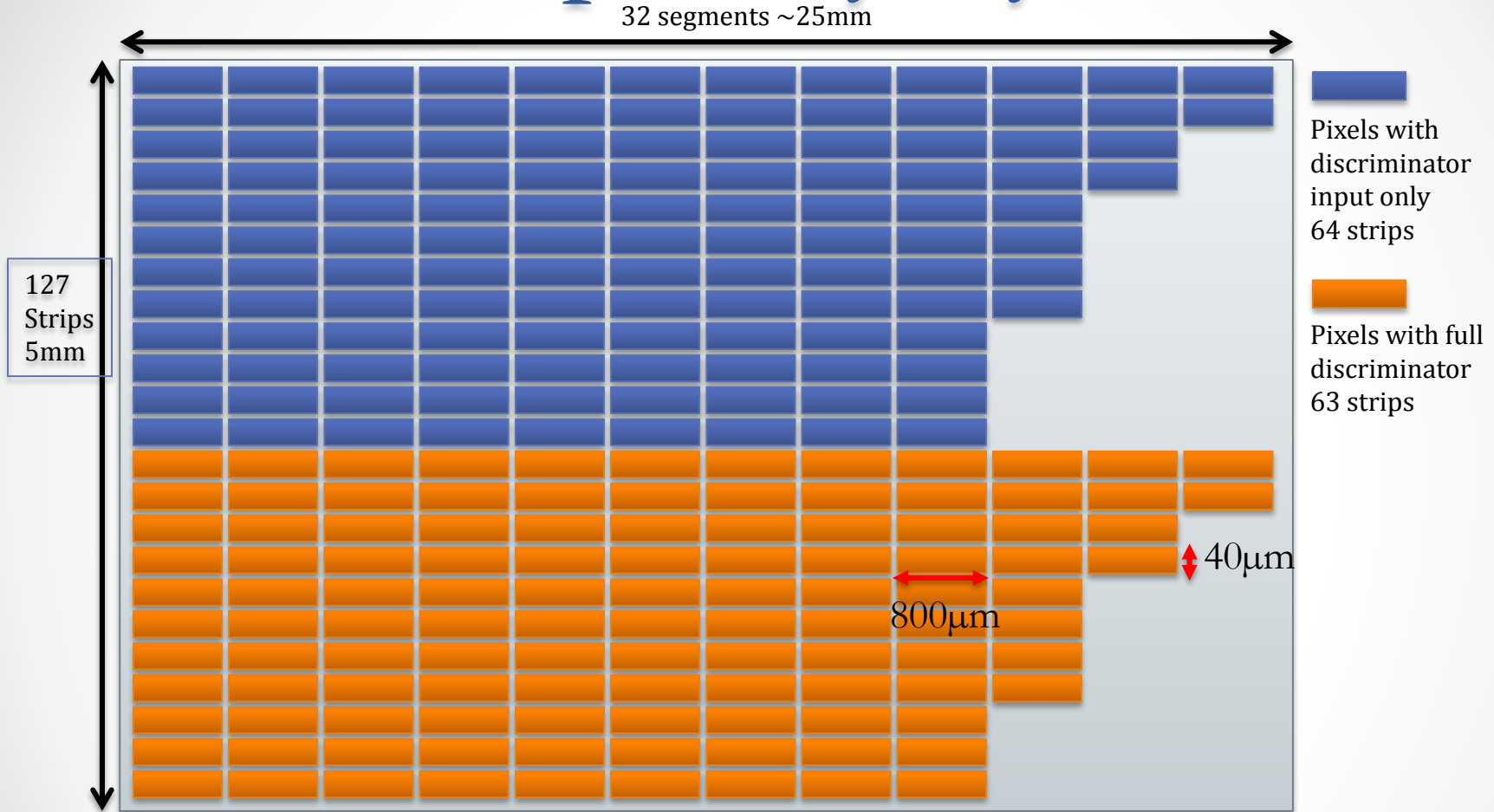
- Can't do a monolithic 20mm x 25mm due to reticle size
- 1mm of periphery

CHESS-2 main architecture



- Design done between UCSC, SLAC & with Ivan Perić.
- Engineering run 20, 80, 200 Ohm bulk resistivity

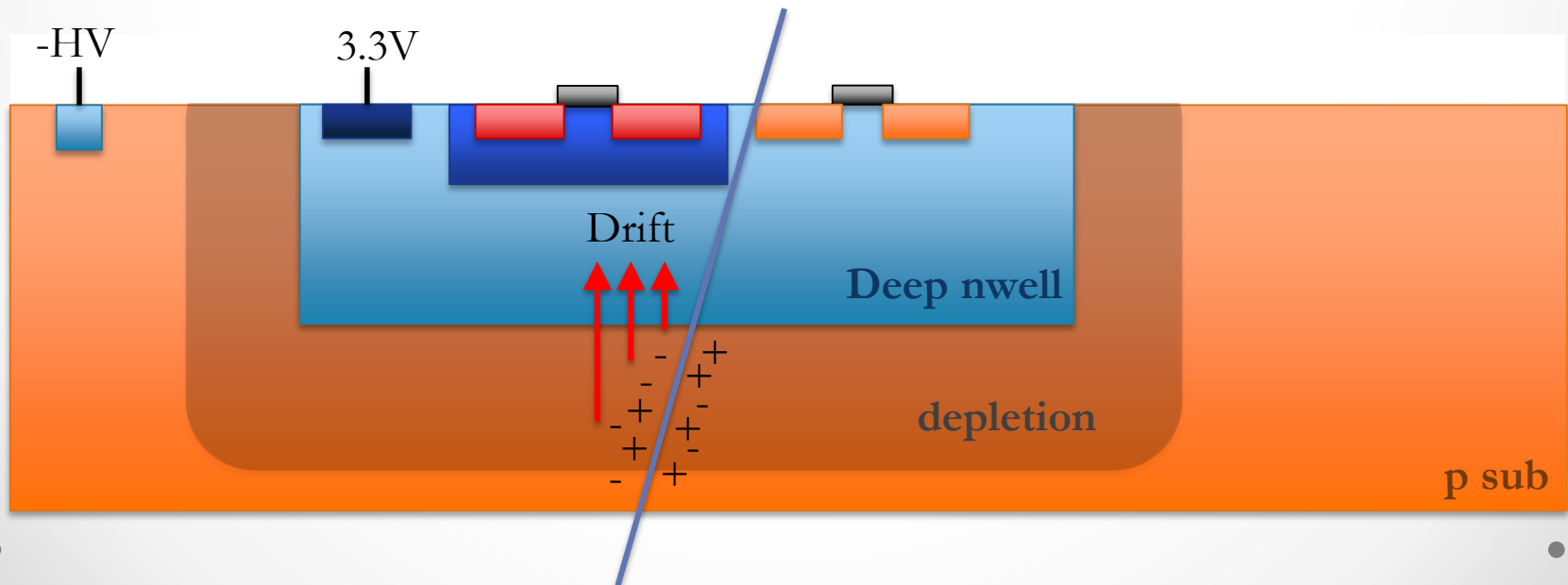
Strip array layout



- Pixels without discriminator have smaller detector capacitance. But there might be analog cross-talk going to the edge.
- 50 & 30% diode fraction

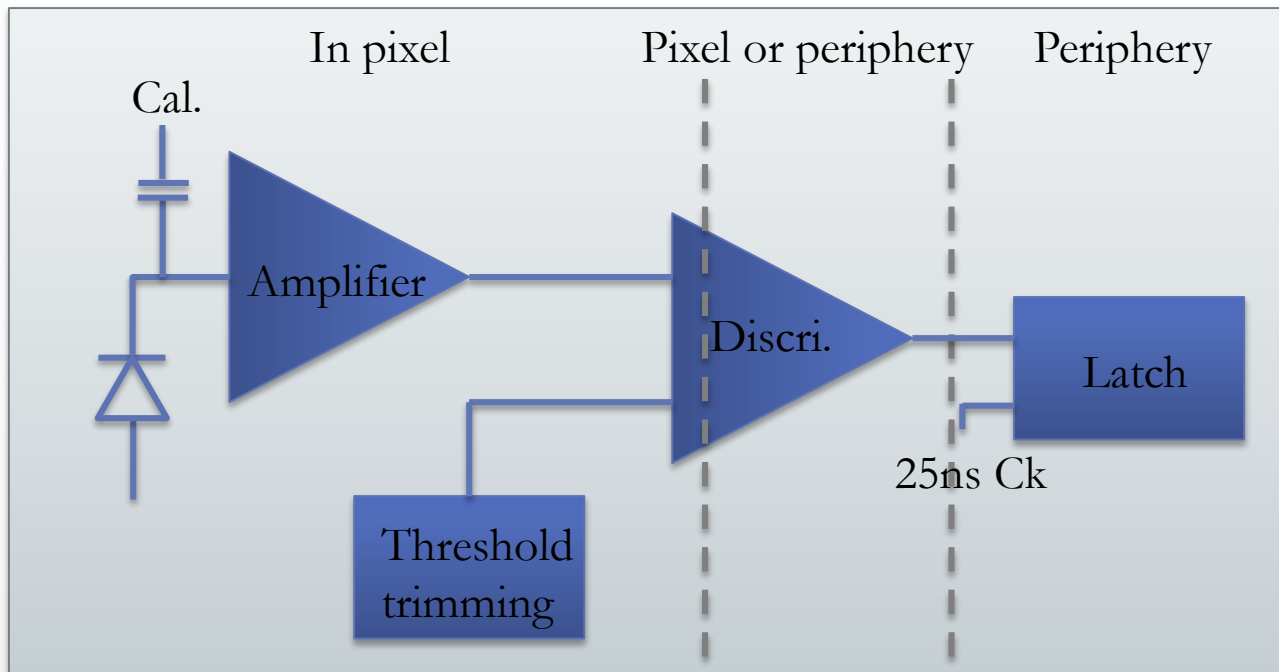
Pixel amplifier

- Most probable value for MIP is $\sim 1500e$ at 120V for a 20 Ohm substrate.
- Landau distribution significant values start $\sim 700e$ (20Ohms).
- For a 32 segment strip, we require threshold to noise of 5 to 1.
- Requires below 25ns peaking time (LHC bunch rate).
- Note: Signal to noise is improved for higher resistivity substrate.

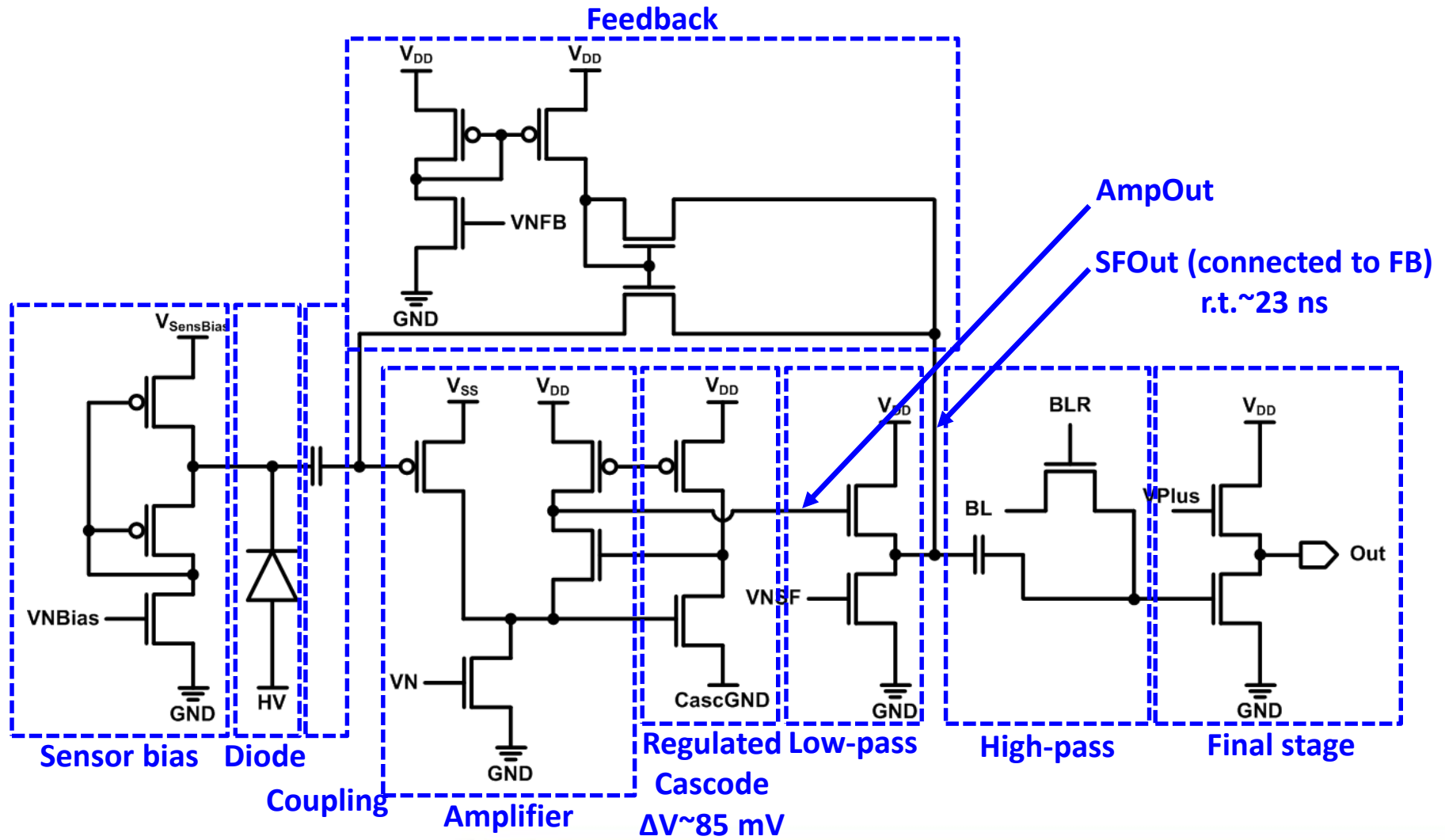


Details of the pixels

- Active amplifier and threshold trimming in each pixel.
- Discriminator front and trimming in pixel
- Full discriminator in pixel or periphery.
- Latches and encoding logic at the periphery.
- Capabilities:
 - Hot pixels masking.
 - Injection of calibration signal.
 - 4bit threshold trimming.



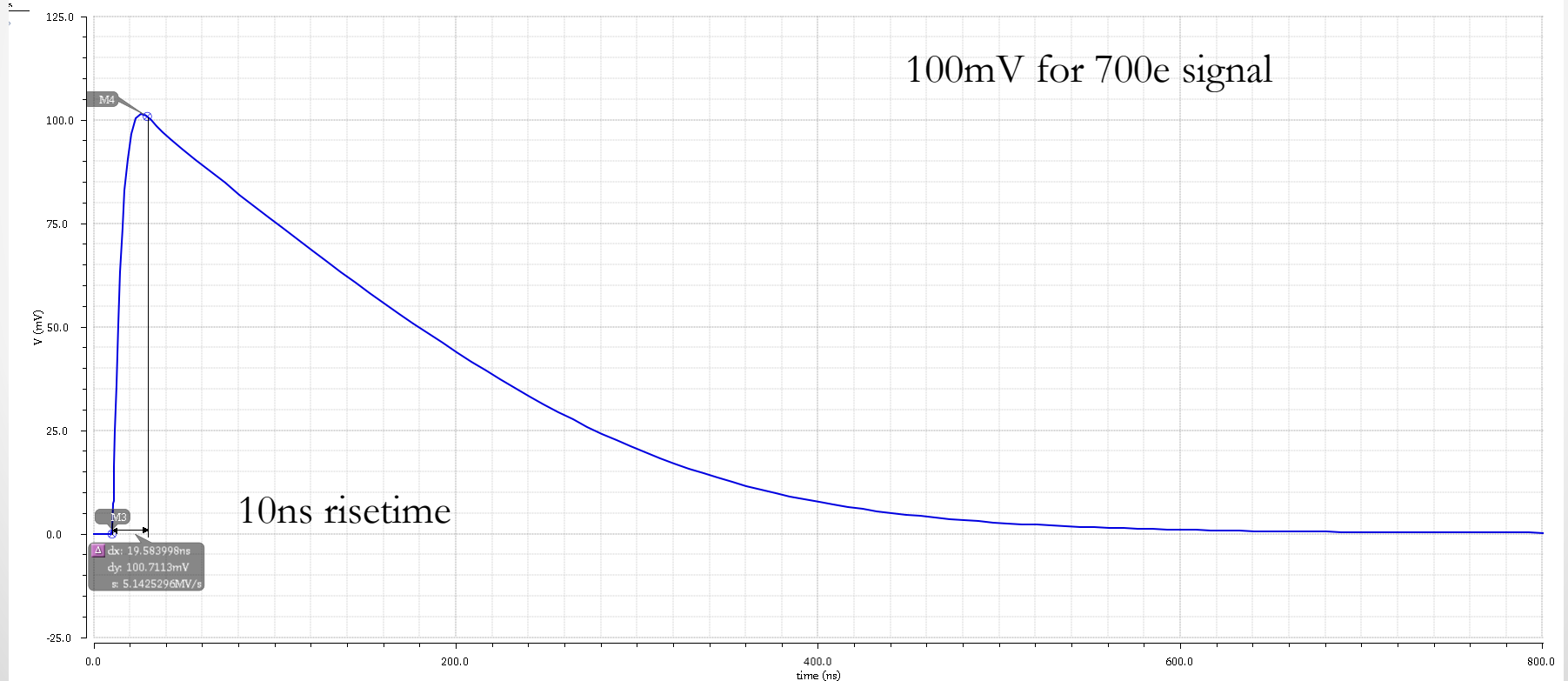
Pixel schematic from I. Peric and E. Vilella



Amplifier simulation

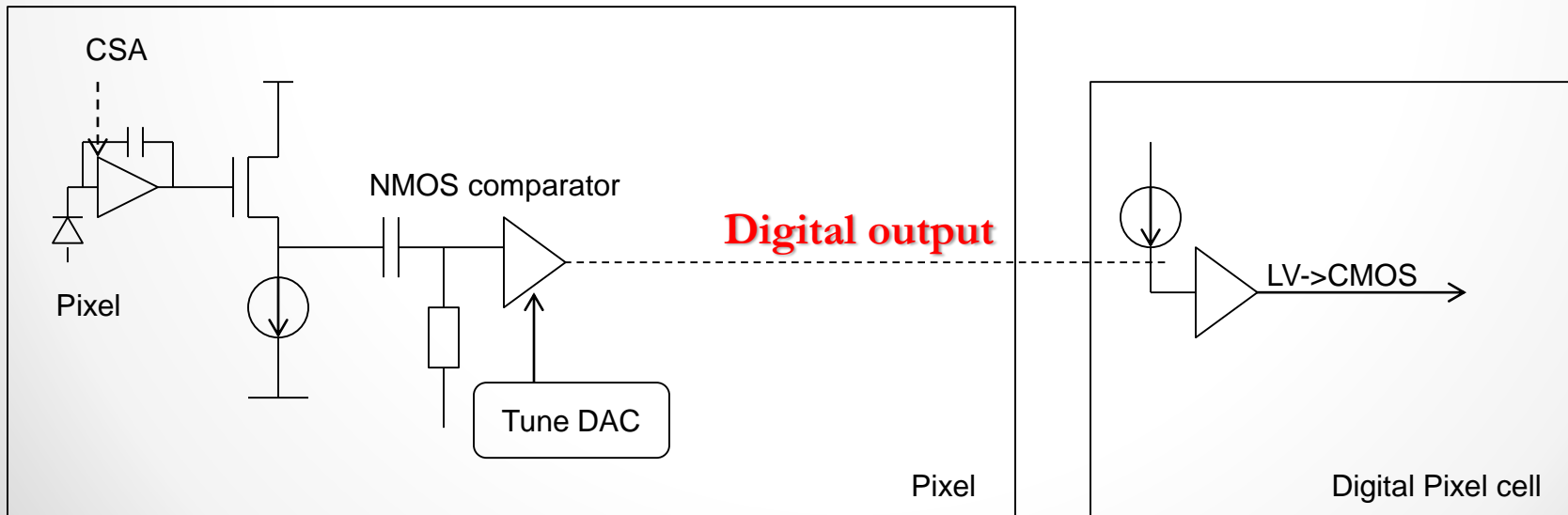
- New amplifier design by Eva Vilella and Ivan Peric
- Fast: $\sim 10\text{ns}$ risetime
- $\text{SNR} = 10$ for $700e$
- Power $30\mu\text{W}/\text{pixel}$, 0.5W per sensor.

Wed Apr 22 02:04:13 2015



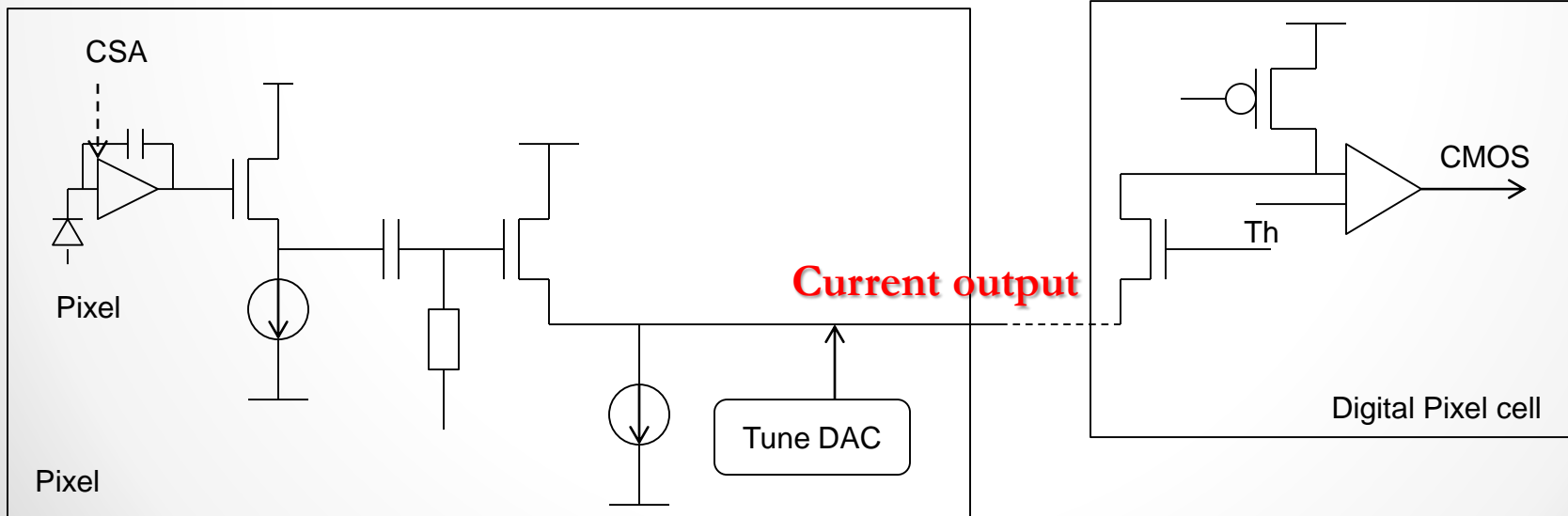
Comparator output [1]

- The sensor is 2.5cm long
- The lines are very coupled and very capacitive:
 - 32 lines 0.6 μ m spacing
 - 2.5cm long
 - Up to 1pF capacitance to other metals (gnd).
- Full in pixel comparator with digital output:
 - Digital output – no worries about crosstalk
 - Bigger layout – added detector capacitance



Comparator output [2]

- The lines are very coupled and very capacitive:
 - 32 lines 0.6 μm spacing
 - 2.5cm long
 - 1pF capacitance to other metal (gnd) maximum.
- Partial in pixel comparator (less added capacitance):
 - Current output – less cross-talk expected
 - Higher mismatch on the comparator.



Strip Hit Encoding

- Single hit in the strip



- Encoded position of the first hit



- Double or multiple hits in the strip

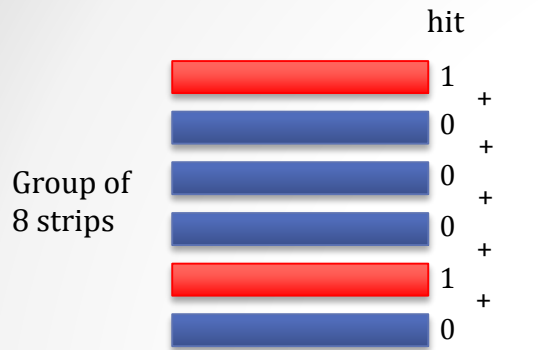


- Encoded position of the first hit + Flag

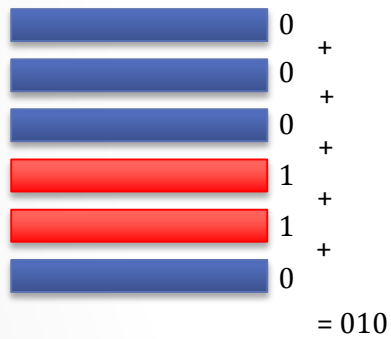


- The first hit in the strip is encoded on **5bits**
- Additional hit **Flag** is raised in case of multiple hits.
- **Flag** provides loose information on the position of the additional hits.
- During strip encoding an internal bit is also raised when the strip is hit.

Hit encoding



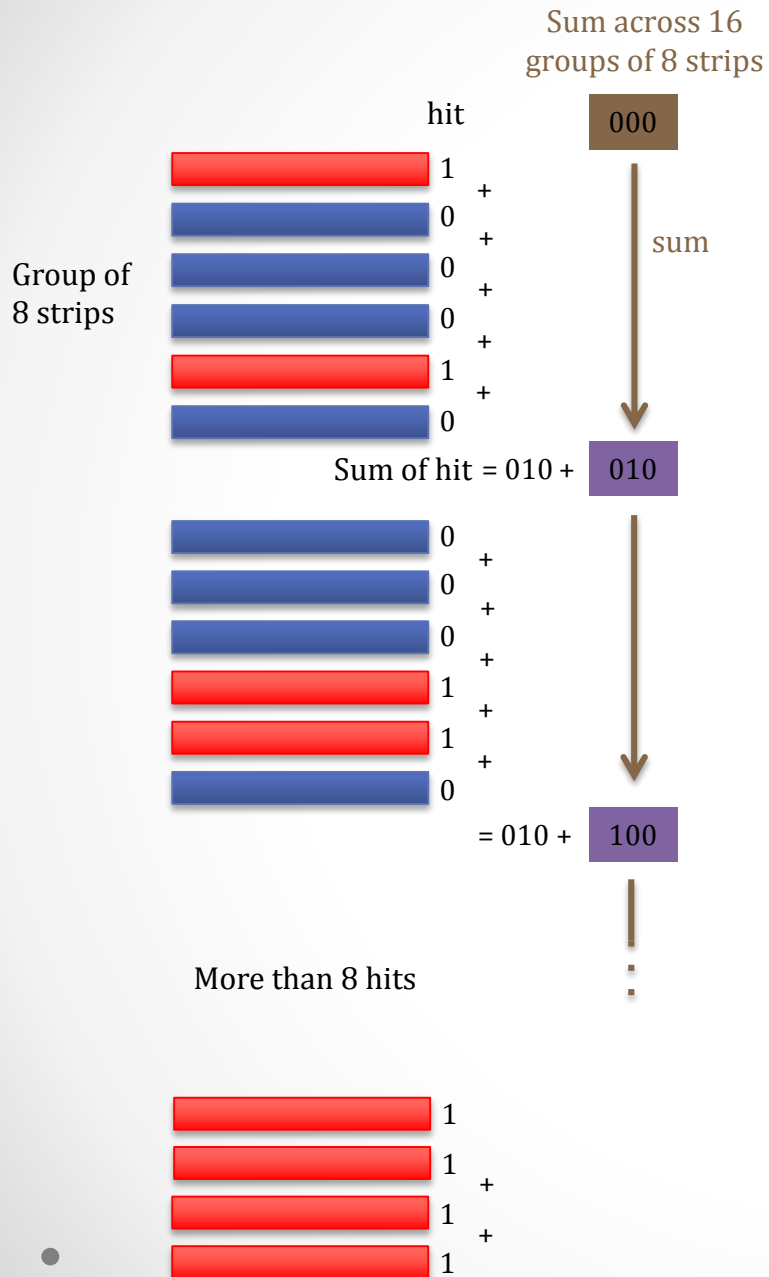
Sum of hit = 010



More than 8 hits

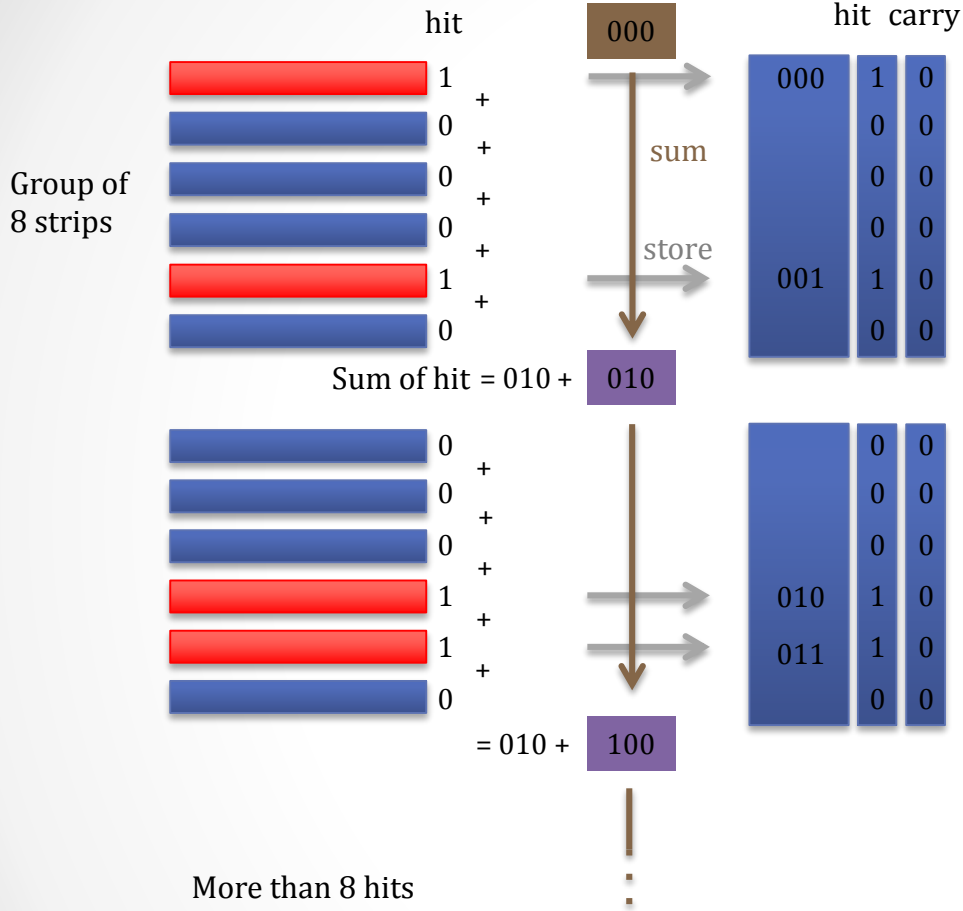


Hit encoding



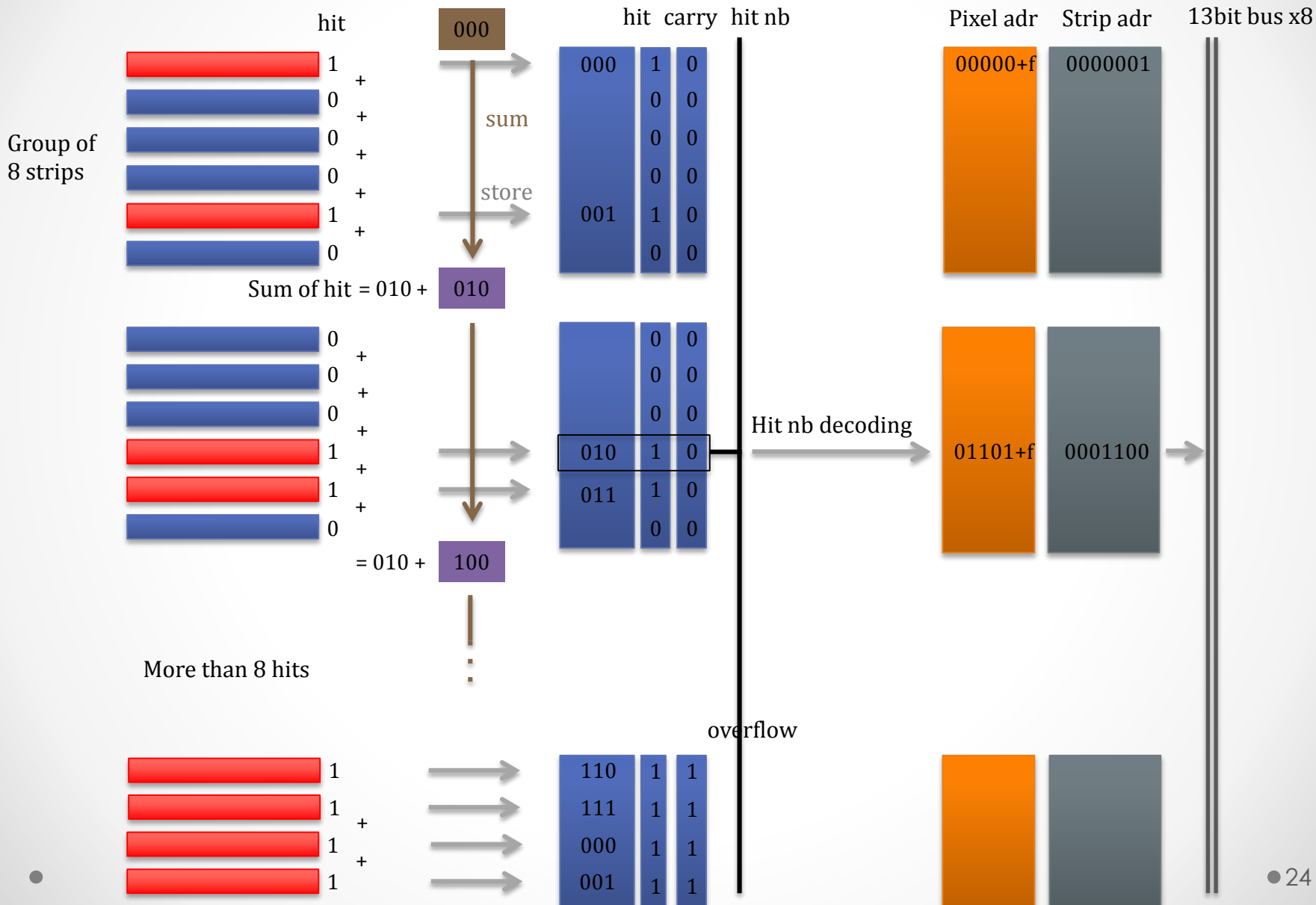
Hit encoding

Sum across 16 groups of 8 strips

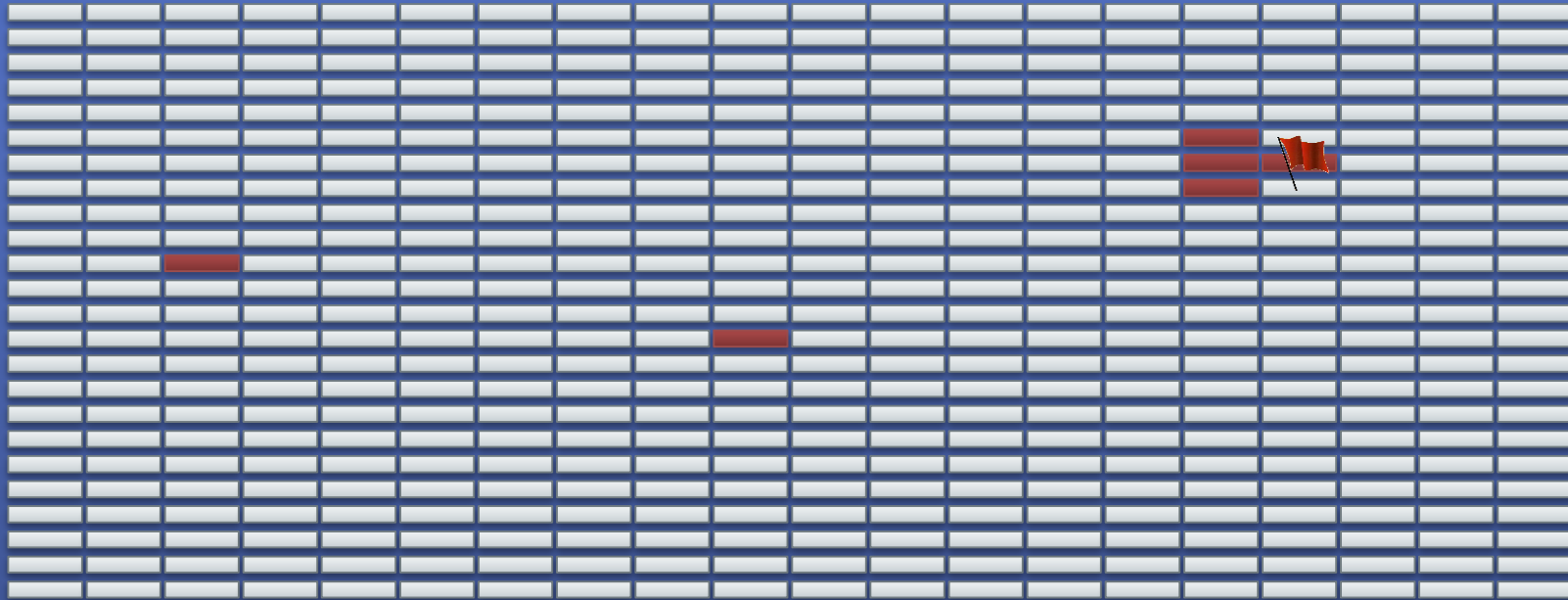


Hit encoding


Sum across 16 groups of 8 strips



Output data format



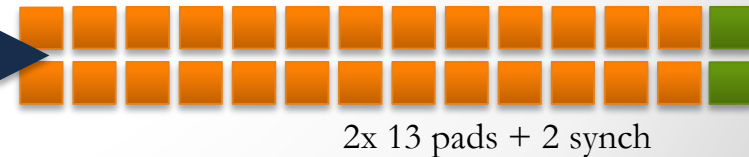
127 strip
= 7bits

32 segments = 5bits + 

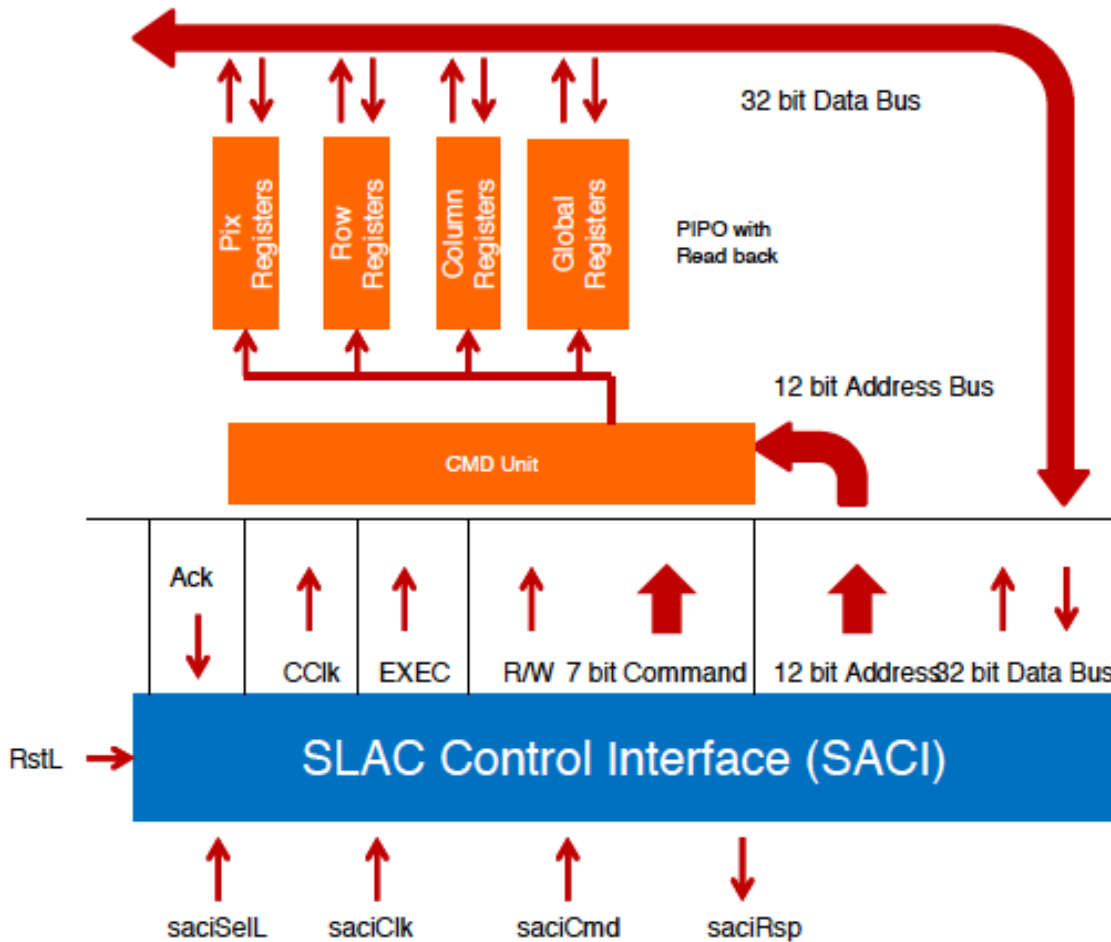
127 strips



Output Pads



SACI – SLAC ASIC Control Interface



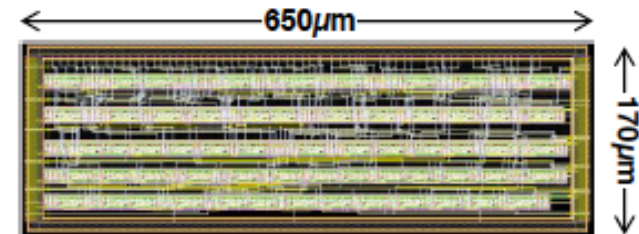
Serial Interface with handshake protocol

5 Signals

- 3 shared: *saciClk*, *saciCmd*, *saciRsp*.
- 1 dedicated select line per slave: *saciSelL*.
- 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.

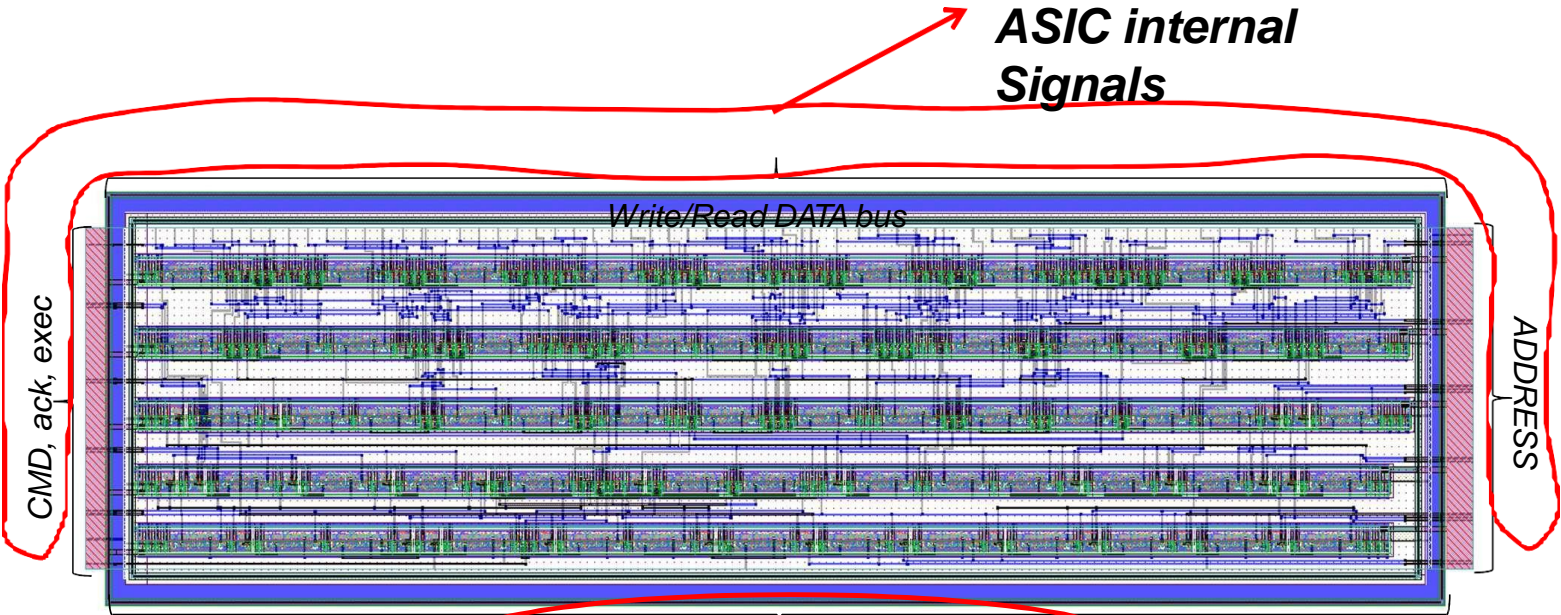
- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).

Layout



SLAC ASIC Control Interface (SACI)

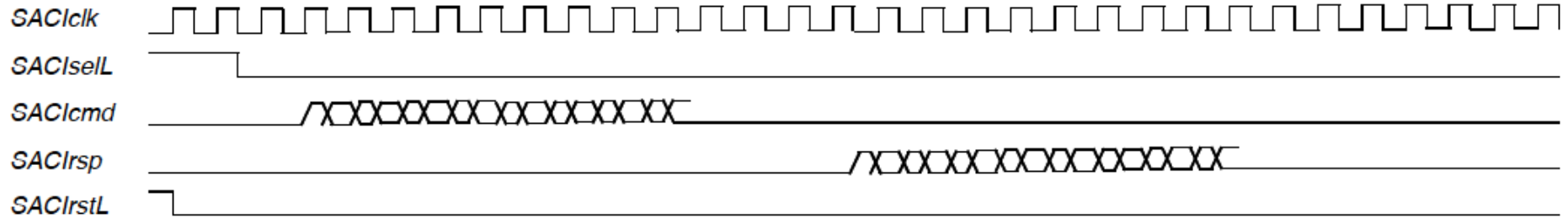
SACIcmd (serial signal):



SACIclk, SACIcmd, SACIrsp, SACI sel, rst

Signals from PADS

SACI - Signals



SACIcmd (serial signal):



SACIrsp (serial signal):



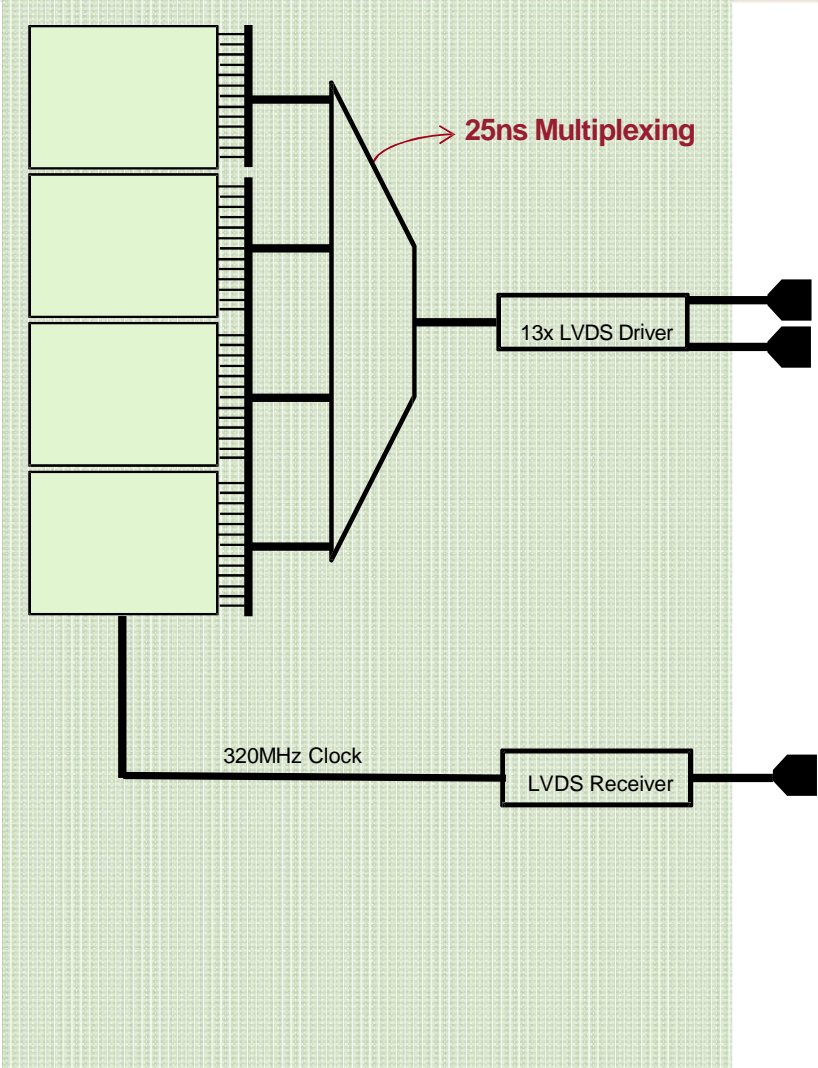
SACI - Commands



| RW | CMD | Function |
|-------------|-----|----------------------------|
| Clock Cycle | | |
| 0/1 | tbd | Read/Write Global Register |
| 1 | tbd | Write Matrix |
| 0/1 | tbd | Read/Write Pixel |

- The ASIC decoded the command last 4 bits. Any given command longer than 4 bits will be interpreted as a 4 bit command.

Encoding Read-Out scheme – Overview



LVDS Driver – Simulated Performance

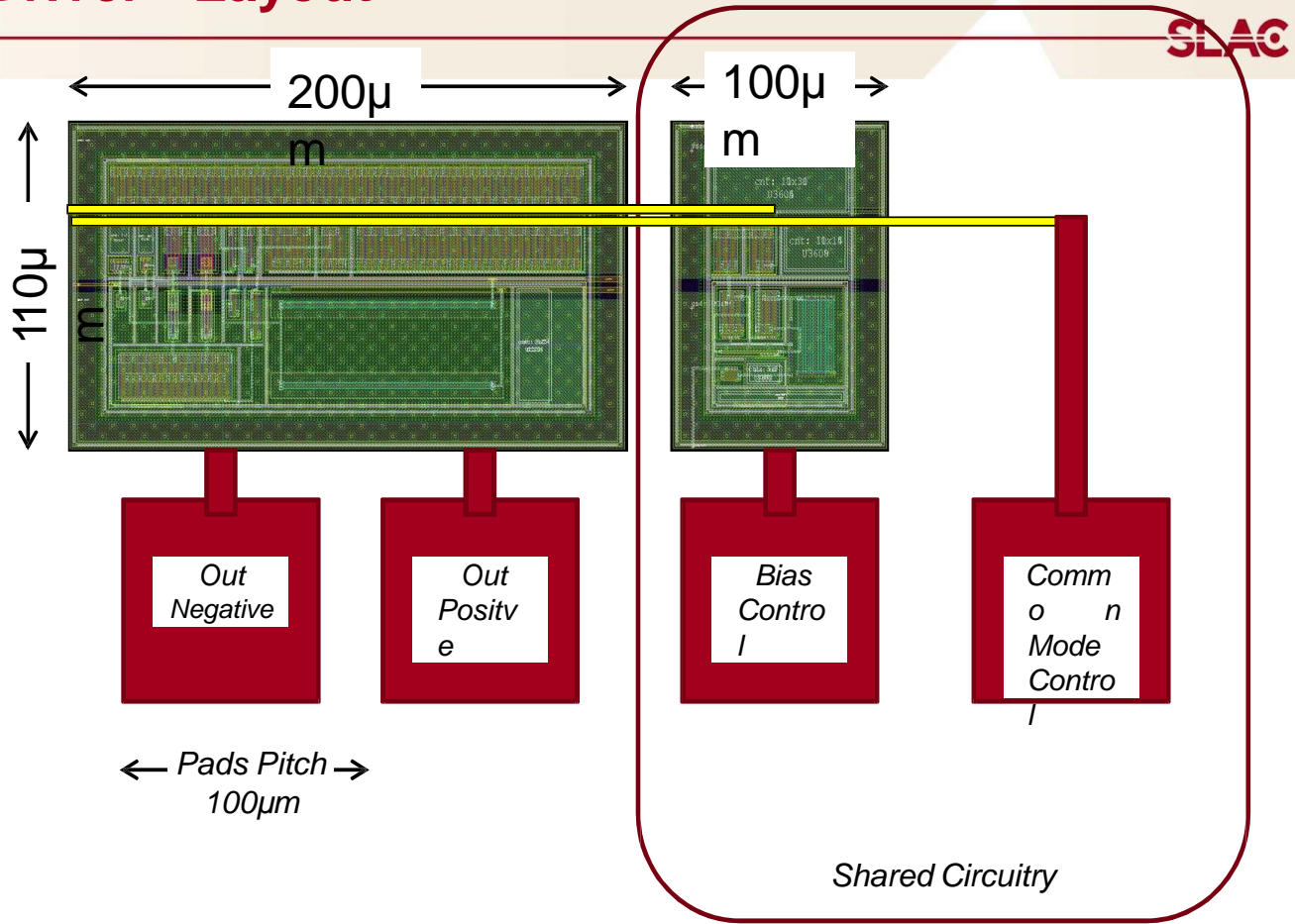


Schematic simulated at all condition (wo,wz,ws,wp) at room

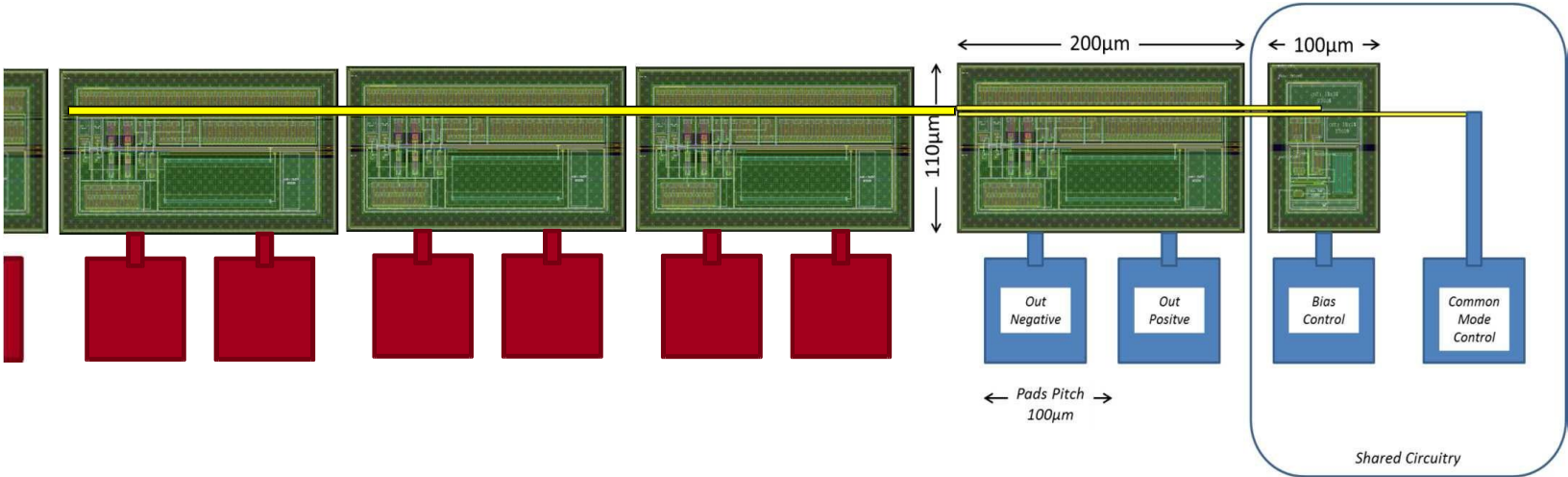
| Specs | Typical | Min | Max |
|---|---------|-------|--------|
| Differential Output Voltage (@ $R_{LOAD}=100\Omega$) | 600mV | | |
| Output Common Mode | 1.2V | 0.5 | 2.8 |
| Current | 3mA | 0.2mA | 3.5mA* |
| Speed | 320MHz | | 500MHz |
| Supply | 3.3V | | |

** Can meet standard LVDS requirements.*

LVDS Driver - Layout



LVDS Driver - Layout



LVDS Receiver – Simulated Performance



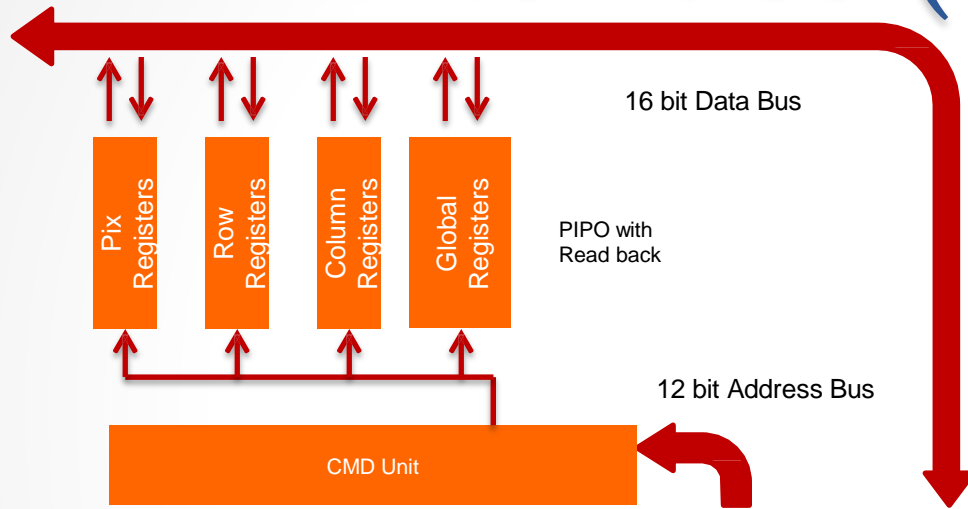
Schematic simulated at all condition (wo,wz,ws,wp) at room temperature.

| Specs | Typical | Min | Max |
|--|---------|-----|---------|
| Differential Input Voltage (@ $R_{LOAD}=100\Omega$) | 600mV | | |
| Output Common Mode | 1.2V | | |
| Input Current | 3mA* | | |
| Speed | 320MHz | | 500M Hz |
| Supply | 3.3V | | |

** Can meet standard LVDS requirements.*



SLAC ASIC Control Interface (SACI)

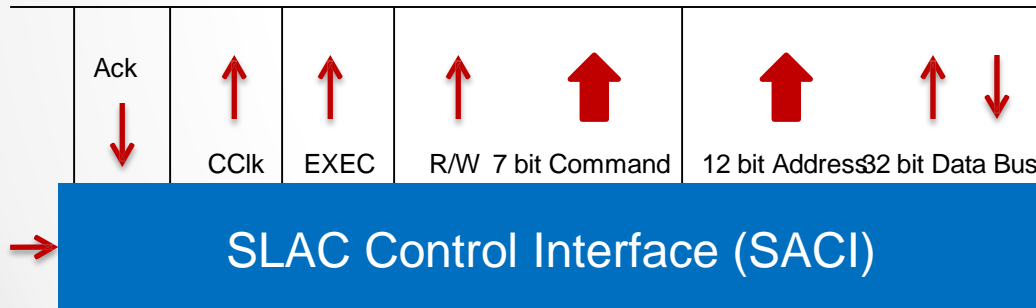
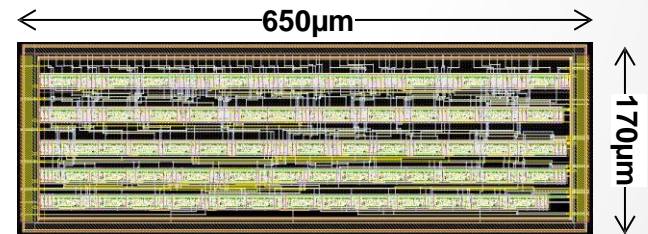


Serial Interface with handshake protocol

5 Signals

- 3 shared: *saciClk*, *saciCmd*, *saciRsp*.
 - 1 dedicated select line per slave: *saciSelL*.
 - 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.
- Operated between 0V and 3.3V
 - Allows multiple SACI on same bus (parallel mode).

Layout



CHESS-2 specification

| | Specifications |
|---------------------------------------|------------------------------------|
| Size of the chip | 0.6cm x 2.5cm |
| Pixel size | 40 μ m x ~800 μ m |
| Number of strips | 127 |
| Number of pixels per strip | 32 |
| Readout speed | 320MHz |
| Output buffers | LVDS with tunable signal amplitude |
| Maximum number of hit per strip | 1 + overflow flag |
| Maximum number of hits in strip array | 8 |
| Size of data output | 13 bits |
| Format of data output | 5 + 1+ 7 bits |
| Latency | Fixed latency |

Summary

- A huge amount of knowledge has been accumulated from CHESS-1 & HV_Strip1
- Physics simulation seems to indicate that 128 strip grouping retaining 8 hits should meet occupancy requirements.
- More simulation would still need to be done including pile-up and harsh conditions in layer 1 and endcaps.
- Design in progress for submission end of June.
- HV & HR are collaborating for this new submission following the specs
(<https://twiki.cern.ch/twiki/bin/viewauth/Atlas/CHESSStripTestChip>).
- Engineering run scheduled with res. from 20 to 200ohms.