

COOL: MAPS for the ATLAS outer pixel layers

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- Motivations

- HR CMOS
 - Why?
 - LFoundry process
 - What can we get out of them?

- COOL1 monolithic architecture
 - Baseline approach
 - Some preliminary pixel simulation
 - Plans for submission

- Conclusions

Motivations from a Science perspective

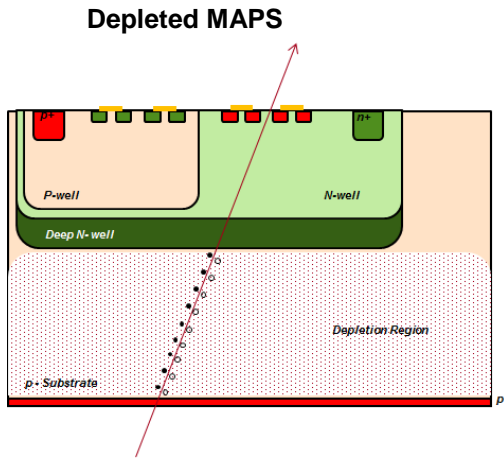
Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost:

- **Significantly lower material budget**
 - eliminate the need for bump bonding or other challenging interconnect methods
 - can be thinned to less than 100um
- **Smaller pixel size**
 - not limited by bump bonding
- **Lower costs**
 - can be implemented in standard commercial technologies

SLAC has an interest in monolithic technologies for applications in:

- **Particle Physics**
 - ILC SiD Tracker and Ecal (kPixM), - ATLAS Strips (with UCSC), -ATLAS Outer Pixels
- **Photon Science**
 - LCLS, LCLSII
- **Neuroscience**
 - Brain studies

Can we build a complete read-out system using a monolithic approach?



The possibility to use **depleted** MAPS for our kind application has been demonstrated by the results that many of you have shown (I. Peric, Bonn group, J. Segal) in the last years and in the past.

Can we build a full read-out system that meets the ATLAS pixels requirements (at least for the outer layers)?

	Hybrid	Depleted MAPS		
		HVCMOS	HRCMOS	SOI
collection speed	fast (drift)	fast (partial/drift)	fast (drift)	fast (drift)
cost	high	low	low	low
material	high	low	low	low
pixel size	medium	small	small	small
signal	high	low	high	high
In pix processing	high	Medium/high	high	medium

that:

- is In-time efficient (95%) within 25ns
- has a sufficient S/N ratio
- has 50x250 μm^2 pixel
- can cope with the expected hit rate
- is low power $\sim 20\mu\text{A}/\text{pixel}$
- can sustain 50 Mrads TID and 10^{15} neq/cm² NIEL

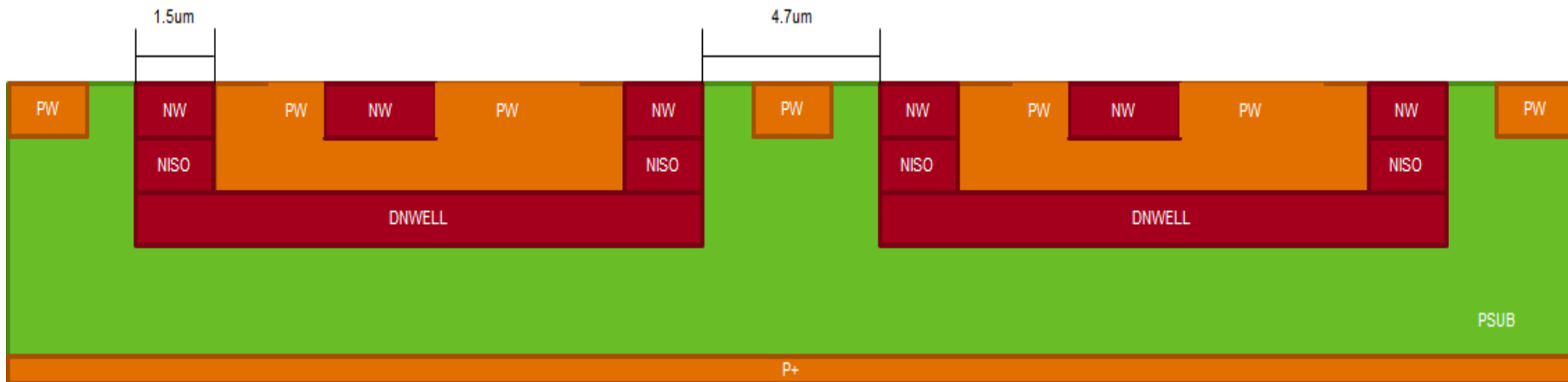
HR CMOS in LFoundry 0.15 μm technology

LF15A is a modular 0.15 μm RF CMOS process, offering up to 6 levels of Al plus thick metal (2 - 6 μm), optionally a MIM capacitor, a polyimide passivation and I/O voltages of 1.8 V, 3.3V and 5.0 V.

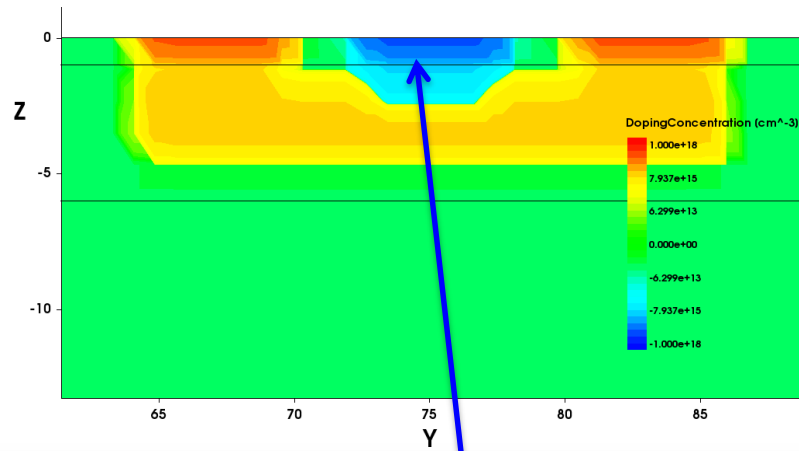
- Substrate resistivity 1-2k Ωcm
- Allow isolated NWELL within a DNWELL (Full CMOS)
- Large fill factor $\sim 85\%$ for 50x250 μm^2 pixel
- Break down voltage $\sim 120\text{V}$

Thinned to 125 μm :

- full depletion from the back side should be feasible (80V at 2k Ωcm)
- $Q_{\text{MIP}} \sim 10000e^-$
- $C_{\text{in}} \sim 400\text{fF}$ (70fF DNW to SUB, 330fF DNW to PW) for 50x250 μm^2 pixel (worst case)
- Considering sharing a threshold around 1000 e^- should give us reasonable efficiency. Required Noise $\sim 100e^-$



Pixel simulations



- Nominal cell: 250um X 50um
- P-well contains both NMOS transistors *and* an embedded n-well with PMOS (not shown)
- Nominal n-well width = 30um

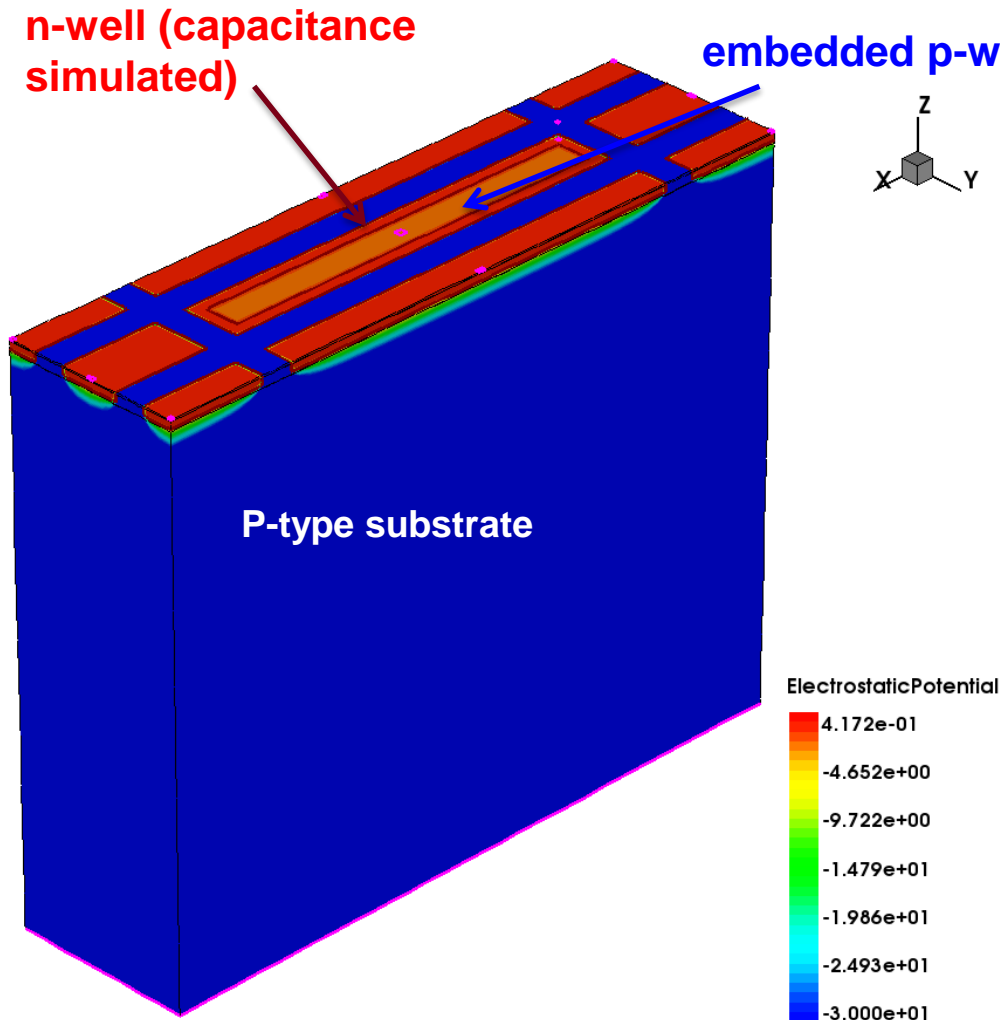
n-well
embedded p-well

Nominal Cell: 30um n-well width

Narrow diffusion:
20um n-well width

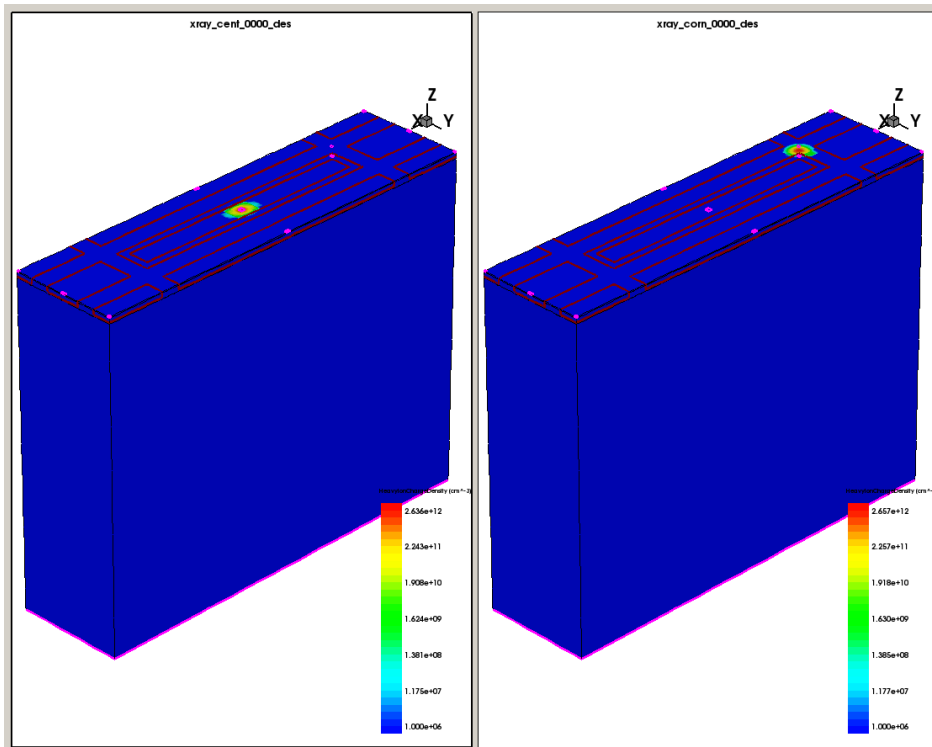
Disclaimer: All simulations based on “educated guesses” about junction profiles, implant mask sizing

Capacitance simulations



Baseline Pixel 250x50, nwell 230x30	n-well to internal p-well capacitance	330fF
Baseline Pixel 250x50, nwell 230x30	total n-well capacitance with internal p-well	400fF
Baseline Pixel 250x50, nwell 230x30	total n-well capacitance without internal p-well	70fF
Narrow diffusion: 250x50, nwell 220x20	total n-well capacitance without internal p-well	51fF

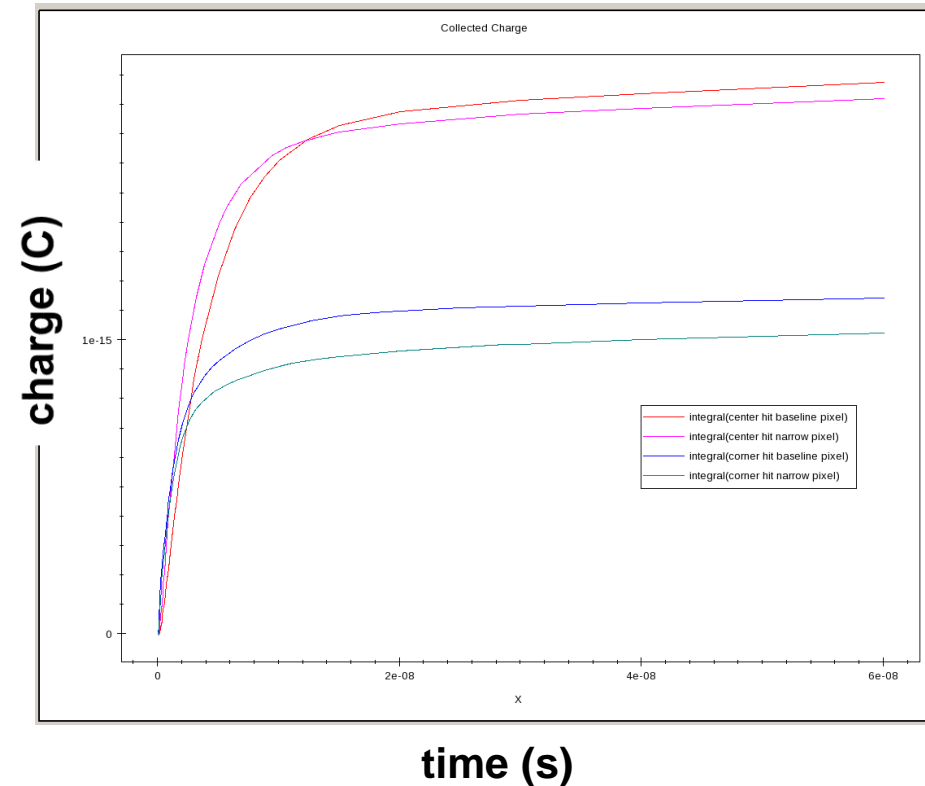
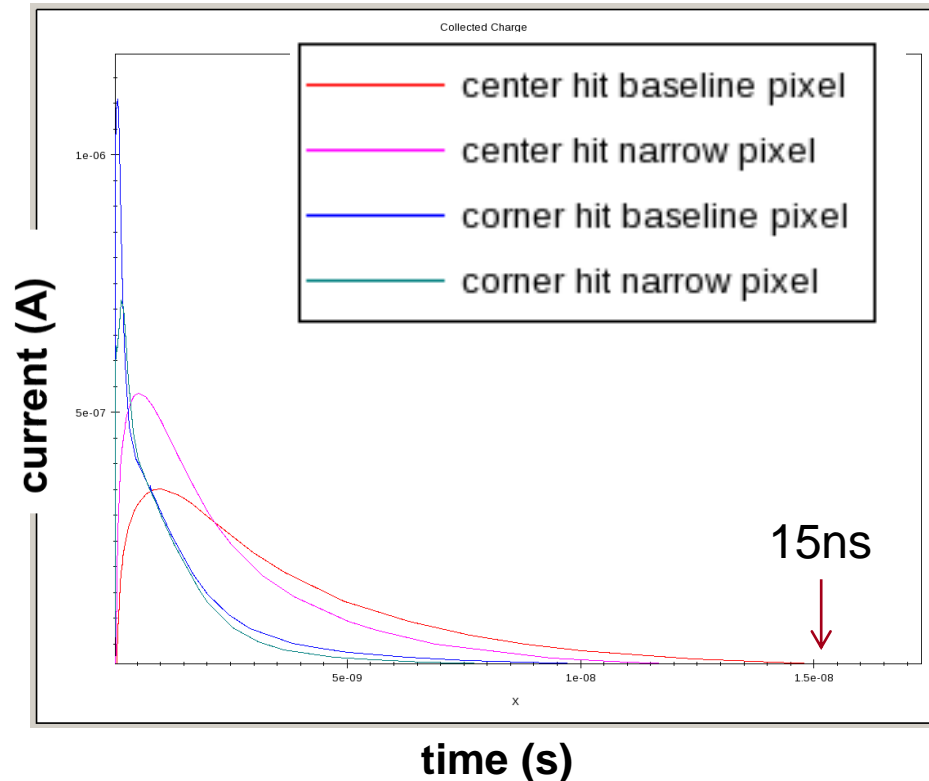
Charge collection for a MIP



**Charge collection @120V bias
Nominal n-well vs. narrow
simulated**

Center Hit vs. Corner Hit

Charge collection for a MIP



- **Corner hit initially faster charge collection due to fields between pixels**
- **Corner hit has significant charge sharing (substrate resistivity = 1000ohm-cm)**

COOL-1: CMOS for Outer Layers ASIC

Given the requirements of the detector at the 5th and 6th layer of pixels an FEI-3 like architecture would be satisfactory. Thus we will assume this as a baseline for the design of COOL.

General characteristics

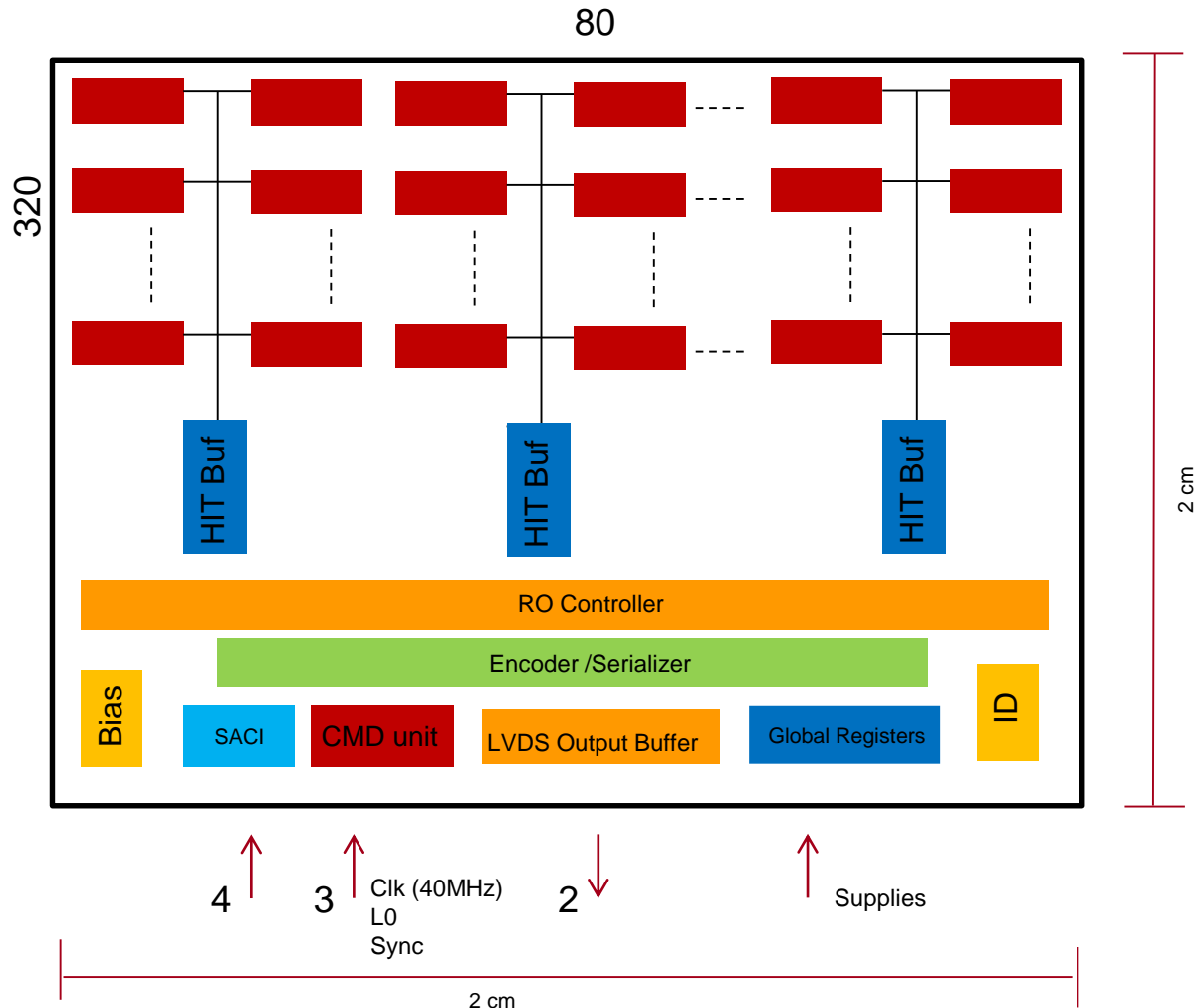
- Bunch timing and amplitude (ToT) extraction
- Column digital readout
- End-of Column hit buffers controlled by the L0 trigger (1MHz, 6 μ m latency)
- System-on-chip approach (limited IO required)
- Serial LVDS readout
- SACL configuration protocol
- Calibration per pixel
- Auxiliary Monitoring

Tentative goals

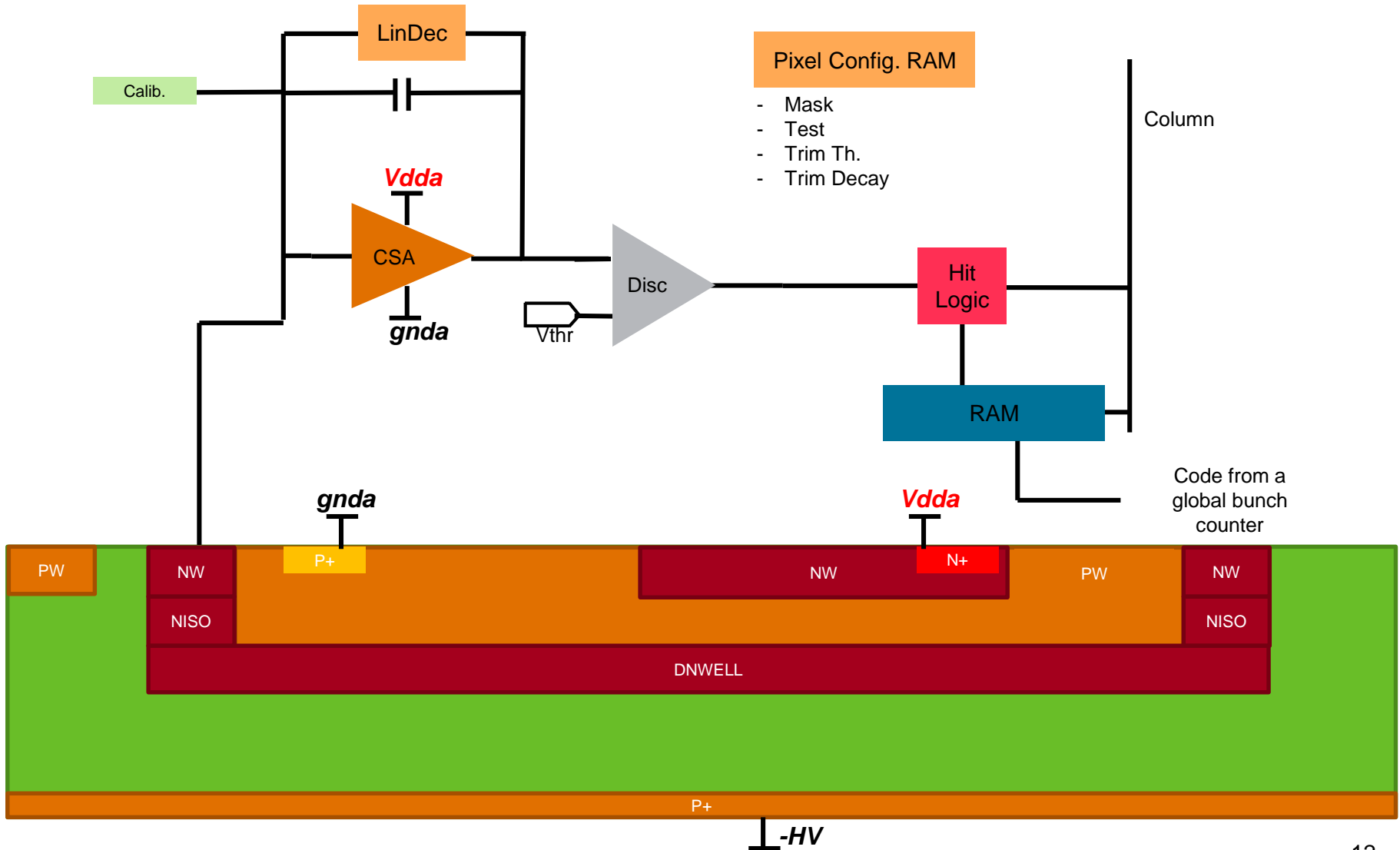
Pixel size	250x50 μ m ²
Array	320x80
Full Size	reticles
Max. Signal	~10ke ⁻
Effective ENC	<120e ⁻
DC Current cons.	~ 20 μ A/pix

COOL-1

COOL-1 general architecture (preliminary):

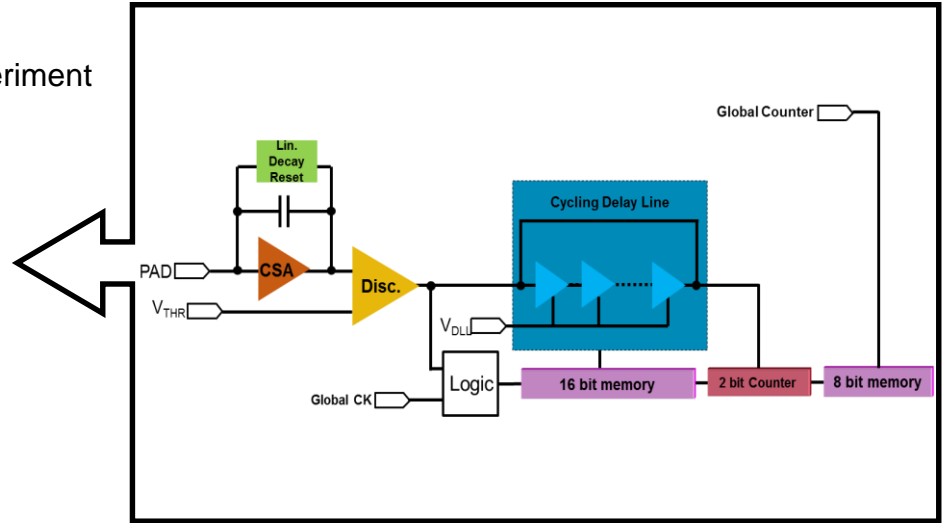
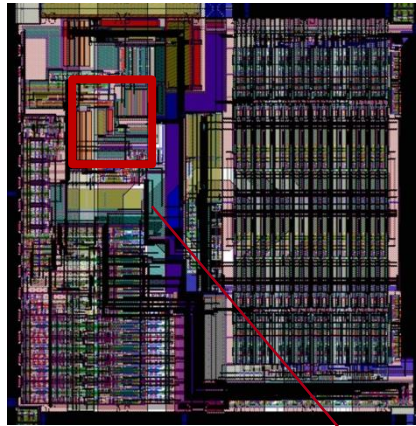
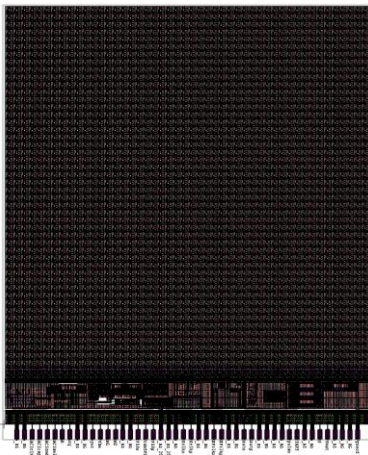


COOL pixel architecture (under study)



COOL Preamp – Ported from tPix ASIC for Tixel 0.13 μm

Tixel a spatial and time resolving pixel detector with full multi-hit capability for a multi-coincidence momentum spectroscopy experiment

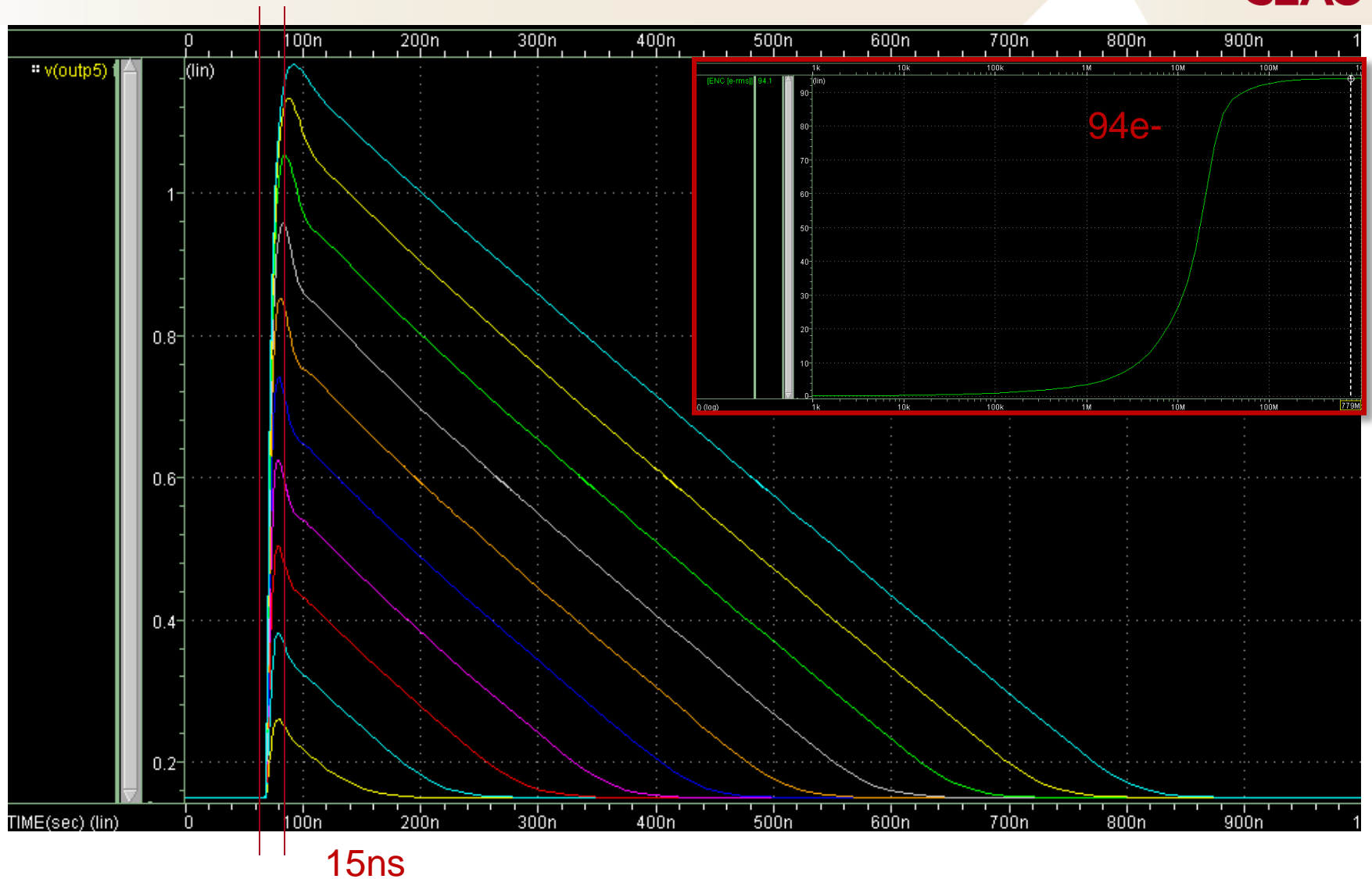


Preamp characteristics

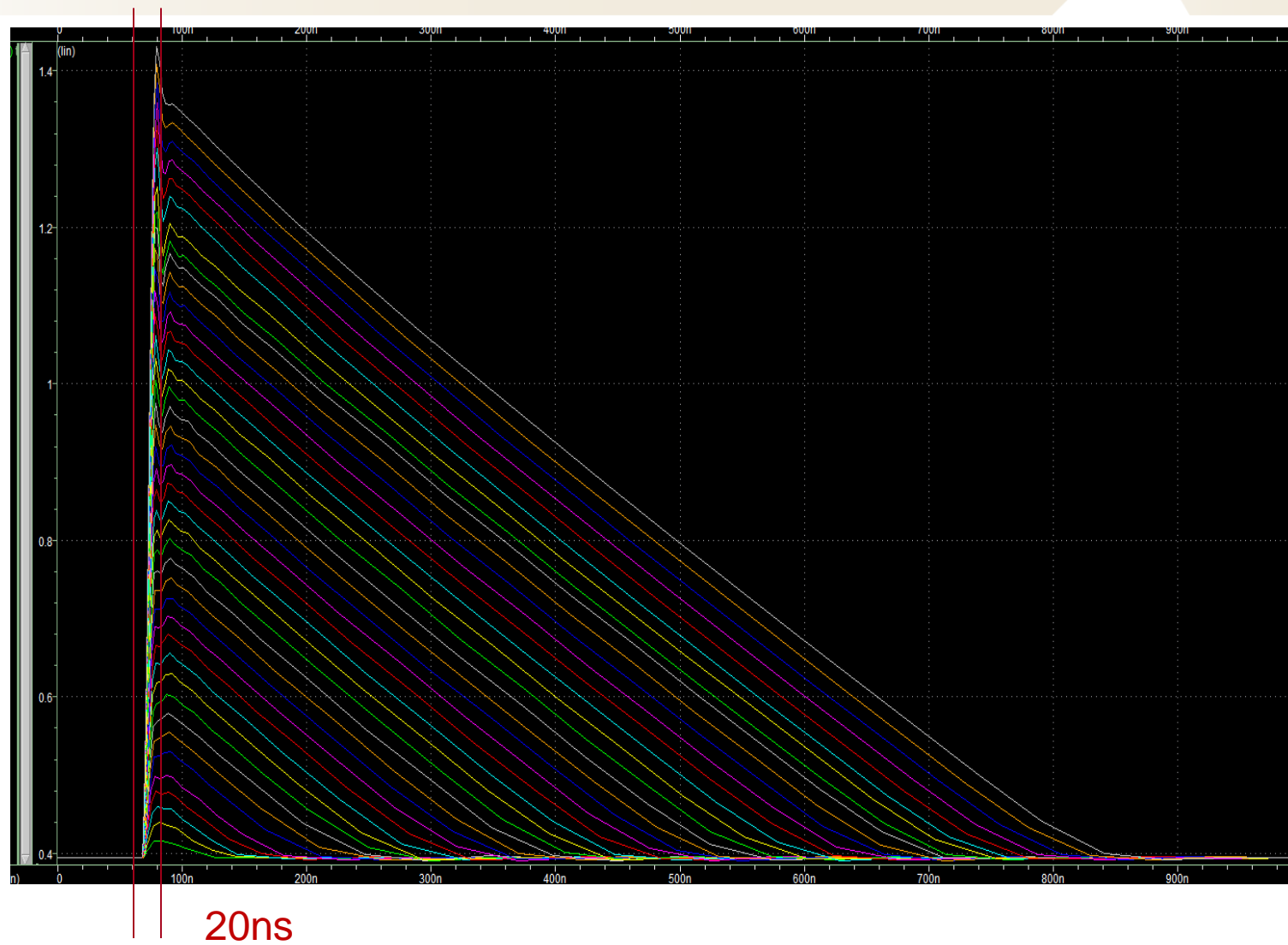
- Consumption 16uA
- Size 25 μm x 25 μm
- Rise time 15ns
- Linear decay (programmable)
- ENC 94e- r.m.s.

	Tixel
Mode of Operation	Time of Arrival + ToT
Pixel Size (μm)	100 x 100
Tile size (pixels)	352 x 384 (2x2 ASICs)
Timing resolution	~ 100ps / 1ns
Time depth	1 μs / 10 μs
Min. threshold	2 keV
Frame Rate	120Hz -1kHz

Tixel preamp for COOL

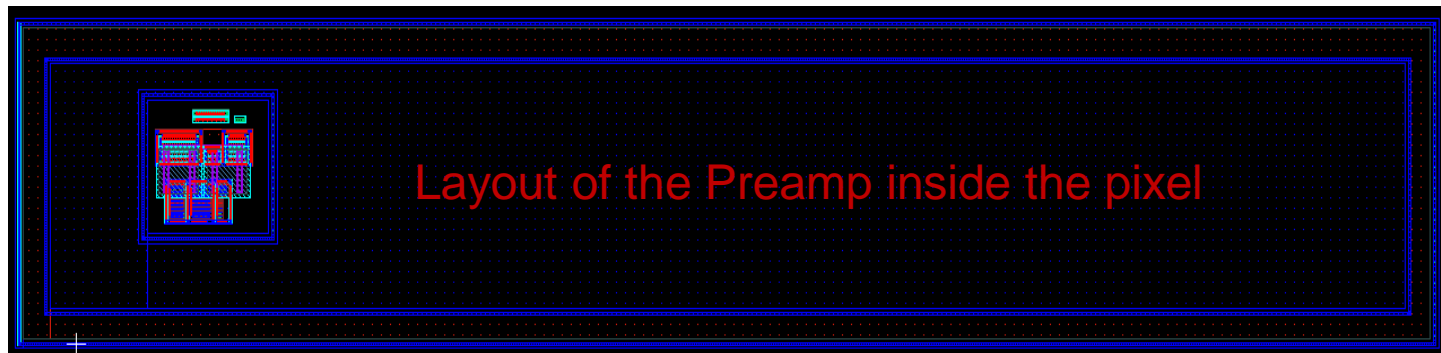
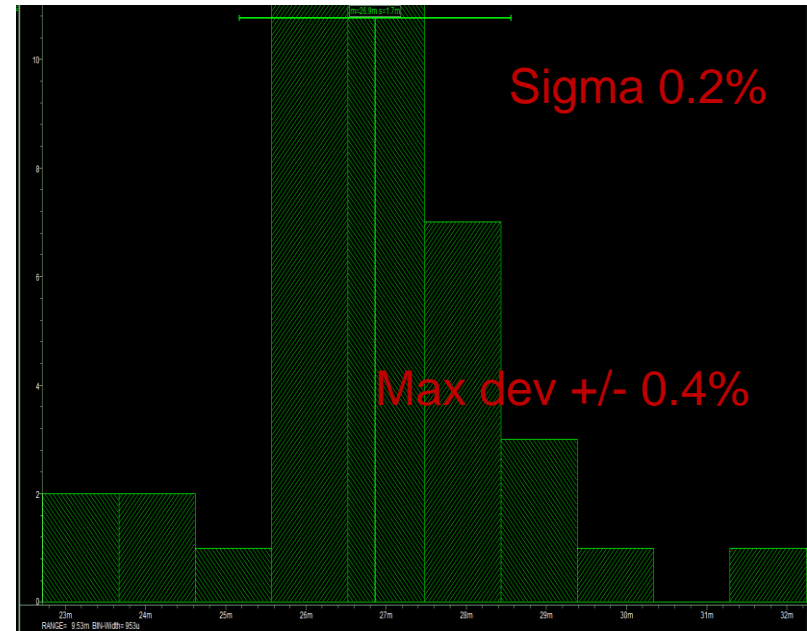
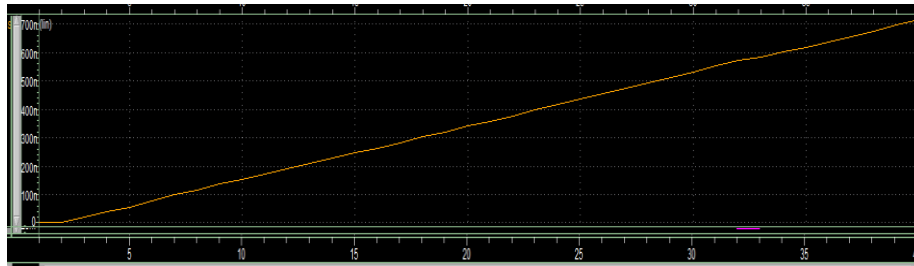


COOL Preamp – Lfoundry 0.15um

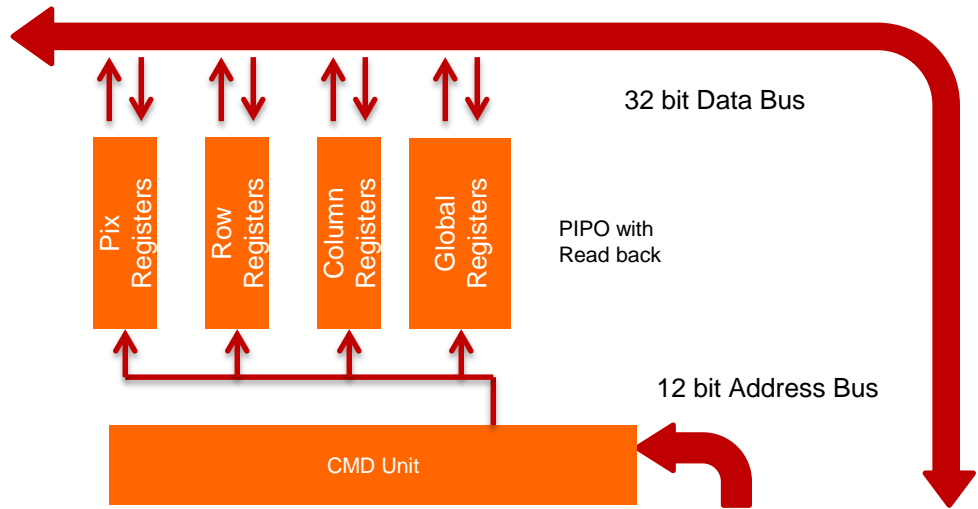


COOL Preamp – Lfoundry 0.15um

ToT Linearity



SACI – SLAC ASIC Control Interface

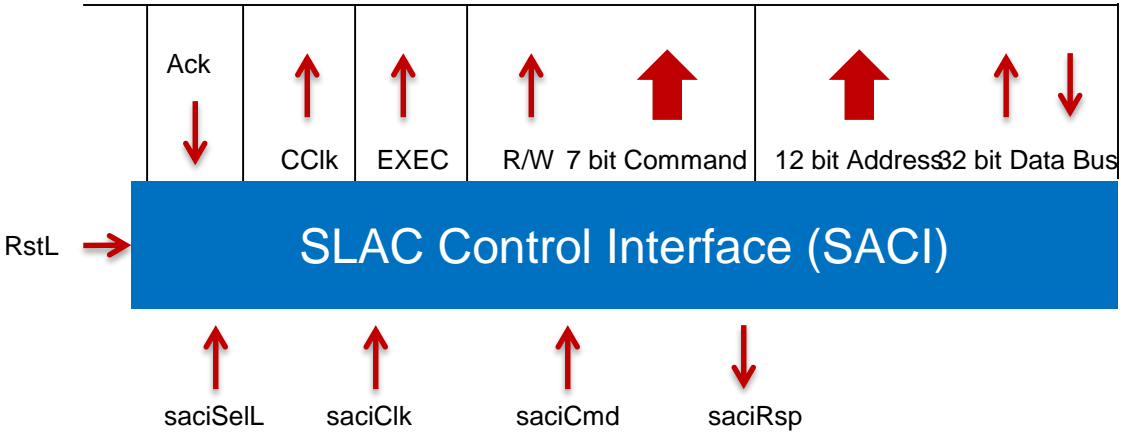
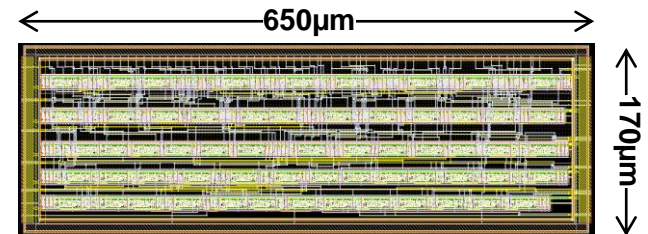


Serial Interface with handshake protocol

5 Signals

- 3 shared: *saciClk*, *saciCmd*, *saciRsp*.
 - 1 dedicated select line per slave: *saciSelL*.
 - 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.
- Operated between 0V and 3.3V
 - Allows multiple SACI on same bus (parallel mode).

Layout (implementation for CHESSII)



Shared LFoundry run with Bonn University on high resistivity substrate ($2\text{k}\Omega\text{cm}$) in the beginning of summer 2015.

Run will include

- Variants of passive arrays of pixel for collection studies
- Variants of active pixel arrays (analog section)
- Simple digital column readout for evaluation purposes
- SACI configuration blocks
- Test blocks for the digital readout
- MOSFET arrays for technology evaluation

Summary and Conclusions

- Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost. There is an opportunity for ATLAS to enhance the Inner Tracker performance adding 2 additional outer layers if we prove this technology effective.
- SLAC is interested in monolithic technology for several fields of applications
- Given the encouraging results presented by other groups in using depleted MAPS for tracking applications we want to investigate the feasibility of a full read-out integrated system for the outer layers using an HRCMOS technology
- Using as a baseline the FEI-3 architecture COOL1 will feature a full column parallel readout for the extraction of hit timing and amplitude (ToT).
 - Architecture details and implementation under study
 - Pixel device simulation in progress
 - Design of the analog pixel in progress (preamplifier architecture under optimization)
 - Porting of digital blocks in progress
 - Technology test structures design in progress