COOL: MAPS for the ATLAS outer pixel layers

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Outline

• Motivations

• HR CMOS
  - Why?
  - LFoundry process
  - What can we get out of them?

• COOL1 monolithic architecture
  - Baseline approach
  - Some preliminary pixel simulation
  - Plans for submission

• Conclusions
Motivations from a Science perspective

Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost:

- Significantly lower material budget
  - eliminate the need for bump bonding or other challenging interconnect methods
  - can be thinned to less than 100um
- Smaller pixel size
  - not limited by bump bonding
- Lower costs
  - can be implemented in standard commercial technologies

SLAC has an interest in monolithic technologies for applications in:

- Particle Physics
  - ILC SiD Tracker and Ecal (kPixM), - ATLAS Strips (with UCSC), -ATLAS Outer Pixels
- Photon Science
  - LCLS, LCLSII
- Neuroscience
  - Brain studies
Can we build a complete read-out system using a monolithic approach?

The possibility to use depleted MAPS for our kind application has been demonstrated by the results that many of you have shown (I. Peric, Bonn group, J. Segal) in the last years and in the past.

Can we build a full read-out system that meets the ATLAS pixels requirements (at least for the outer layers)?

<table>
<thead>
<tr>
<th>Hybrid</th>
<th>Depleted MAPS</th>
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<tbody>
<tr>
<td></td>
<td>HVCMOS</td>
</tr>
<tr>
<td>collection speed</td>
<td>fast (drift)</td>
</tr>
<tr>
<td>cost</td>
<td>high</td>
</tr>
<tr>
<td>material</td>
<td>high</td>
</tr>
<tr>
<td>pixel size</td>
<td>medium</td>
</tr>
<tr>
<td>signal</td>
<td>high</td>
</tr>
<tr>
<td>In pix processing</td>
<td>high</td>
</tr>
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</table>

that:
- is In-time efficient (95%) within 25ns
- has a sufficient S/N ratio
- has 50x250 μm^2 pixel
- can cope with the expected hit rate
- is low power ~20μA/pixel
- can sustain 50 Mrads TID and 10^15 neq/cm2 NIEL
LF15A is a modular 0.15 μm RF CMOS process, offering up to 6 levels of Al plus thick metal (2 - 6 μm), optionally a MIM capacitor, a polyimide passivation and I/O voltages of 1.8 V, 3.3V and 5.0 V.

- Substrate resistivity 1-2kΩcm
- Allow isolated NWELL within a DNWELL (Full CMOS)
- Large fill factor ~85% for 50x250 μm^2 pixel
- Break down voltage ~120V

Thinned to 125μm:
- full depletion from the back side should be feasible (80V at 2kΩcm)
- \( Q_{MIP} \sim 10000e^- \)
- \( C_{in} \sim 400fF \) (70fF DNW to SUB, 330fF DNW to PW) for 50x250 μm^2 pixel (worst case)
- Considering sharing a threshold around 1000e^- should give us reasonable efficiency. Required Noise ~100e^-
Pixel simulations

- Nominal cell: 250um X 50um
- P-well contains both NMOS transistors and an embedded n-well with PMOS (not shown)
- Nominal n-well width = 30um

Disclaimer: All simulations based on “educated guesses” about junction profiles, implant mask sizing
Capacitance simulations

- n-well (capacitance simulated)
- embedded p-well

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Description</th>
<th>Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline Pixel</td>
<td>250x50, nwell 230x30</td>
<td>n-well to internal p-well capacitance</td>
</tr>
<tr>
<td>Baseline Pixel</td>
<td>250x50, nwell 230x30</td>
<td>total n-well capacitance with internal p-well</td>
</tr>
<tr>
<td>Baseline Pixel</td>
<td>250x50, nwell 230x30</td>
<td>total n-well capacitance without internal p-well</td>
</tr>
<tr>
<td>Narrow diffusion</td>
<td>250x50, nwell 220x20</td>
<td>total n-well capacitance without internal p-well</td>
</tr>
</tbody>
</table>

P-type substrate
Charge collection for a MIP

Charge collection @120V bias
Nominal n-well vs. narrow simulated

Center Hit vs. Corner Hit
Charge collection for a MIP

- Corner hit initially faster charge collection due to fields between pixels
- Corner hit has significant charge sharing (substrate resistivity = 1000ohm-cm)
COOL-1: CMOS fOr Outer Layers ASIC

Given the requirements of the detector at the 5th and 6th layer of pixels an FEI-3 like architecture would be satisfactory. Thus we will assume this as a baseline for the design of COOL.

General characteristics

- Bunch timing and amplitude (ToT) extraction
- Column digital readout
- End-of Column hit buffers controlled by the L0 trigger (1MHz, 6µm latency)
- System-on-chip approach (limited IO required)
- Serial LVDS readout
- SACI configuration protocol
- Calibration per pixel
- Auxiliary Monitoring

<table>
<thead>
<tr>
<th>Tentative goals</th>
<th>COOL-1</th>
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<tbody>
<tr>
<td><strong>Pixel size</strong></td>
<td>250x50 µm²</td>
</tr>
<tr>
<td><strong>Array</strong></td>
<td>320x80 reticles</td>
</tr>
<tr>
<td><strong>Full Size</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Max. Signal</strong></td>
<td>~10ke⁻</td>
</tr>
<tr>
<td><strong>Effective ENC</strong></td>
<td>&lt;120e⁻</td>
</tr>
<tr>
<td><strong>DC Current cons.</strong></td>
<td>~ 20µA/pix</td>
</tr>
</tbody>
</table>
COOL-1 general architecture (preliminary):
COOL pixel architecture (under study)

- Mask
- Test
- Trim Th.
- Trim Decay
COOL Preamp – Ported from tPix ASIC for Tixel 0.13µm

Tixel a spatial and time resolving pixel detector with full multi-hit capability for a multi-coincidence momentum spectroscopy experiment

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>Time of Arrival + ToT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size (µm)</td>
<td>100 x 100</td>
</tr>
<tr>
<td>Tile size (pixels)</td>
<td>352 x 384 (2x2 ASICs)</td>
</tr>
<tr>
<td>Timing resolution</td>
<td>~ 100ps / 1ns</td>
</tr>
<tr>
<td>Time depth</td>
<td>1µs / 10µs</td>
</tr>
<tr>
<td>Min. threshold</td>
<td>2 keV</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>120Hz -1kHz</td>
</tr>
</tbody>
</table>

Preamp characteristics

- Consumption 16uA
- Size 25µm x 25 µm
- Rise time 15ns
- Linear decay (programmable)
- ENC 94e- r.m.s.
Tixel preamp for COOL
COOL Preamp – Lfoundry 0.15um
COOL Preamp – Lfoundry 0.15um

ToT Linearity

Sigma 0.2%
Max dev +/- 0.4%

Layout of the Preamp inside the pixel
Serial Interface with handshake protocol

- 5 Signals
  - 3 shared: saciClk, saciCmd, saciRsp.
  - 1 dedicated select line per slave: saciSelL.
  - 1 Reset Line (RstL) can be shared with the ASIC Global Reset.

- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).

Layout (implementation for CHESSII)

SLAC Control Interface (SACI)
Shared LFoundry run with Bonn University on high resistivity substrate (2kΩcm) in the beginning of summer 2015.

**Run will include**

- Variants of passive arrays of pixel for collection studies
- Variants of active pixel arrays (analog section)
- Simple digital column readout for evaluation purposes
- SACI configuration blocks
- Test blocks for the digital readout
- MOSFET arrays for technology evaluation
Summary and Conclusions

• Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost. There is an opportunity for ATLAS to enhance the Inner Tracker performance adding 2 additional outer layers if we prove this technology effective.

• SLAC is interested in monolithic technology for several fields of applications

• Given the encouraging results presented by other groups in using depleted MAPS for tracking applications we want to investigate the feasibility of a full read-out integrated system for the outer layers using an HRCMOS technology

• Using as a baseline the FEI-3 architecture COOL1 will feature a full column parallel readout for the extraction of hit timing and amplitude (ToT).
  - Architecture details and implementation under study
  - Pixel device simulation in progress
  - Design of the analog pixel in progress (preamplifier architecture under optimization)
  - Porting of digital blocks in progress
  - Technology test structures design in progress