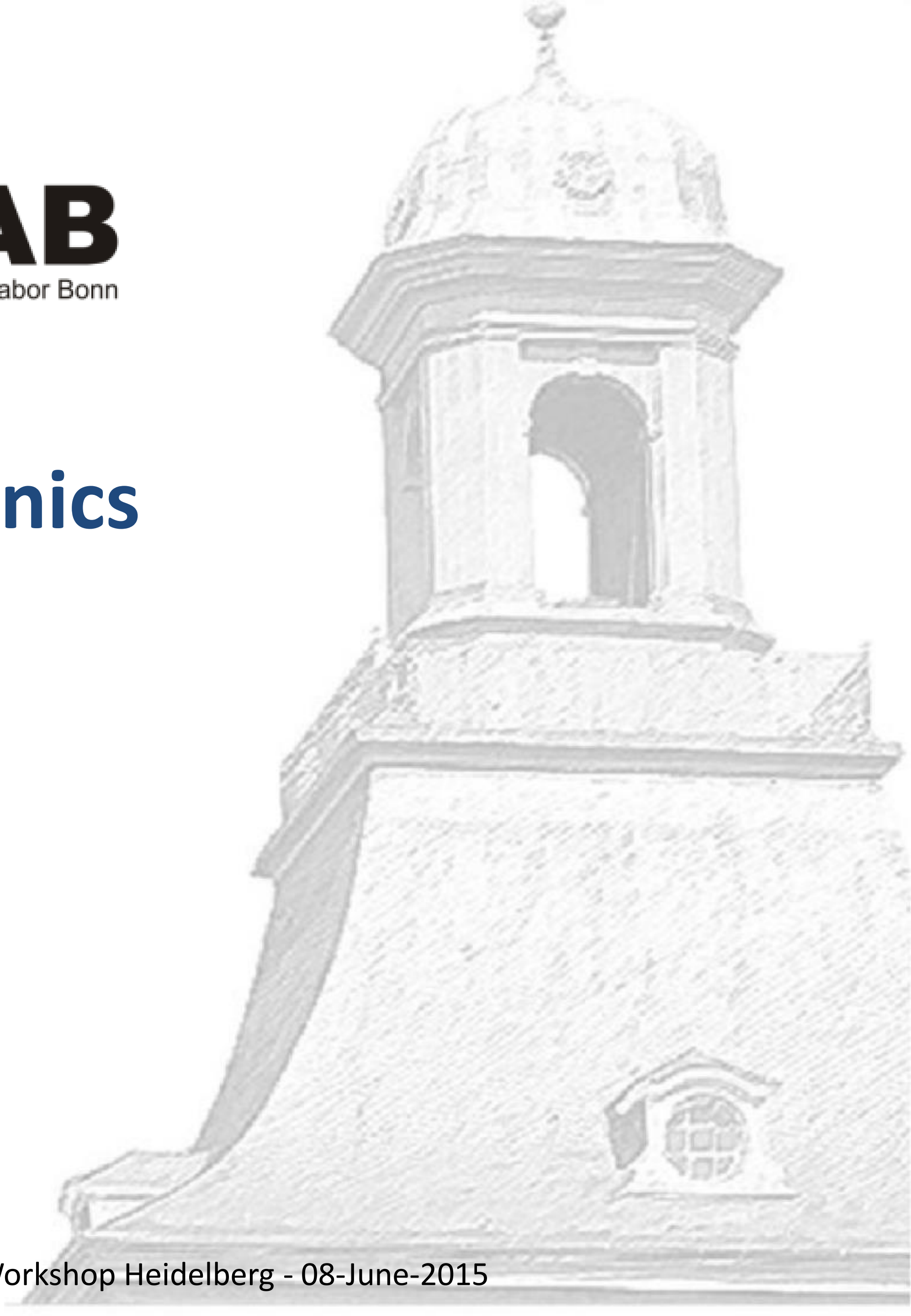

Modules and Mechanics

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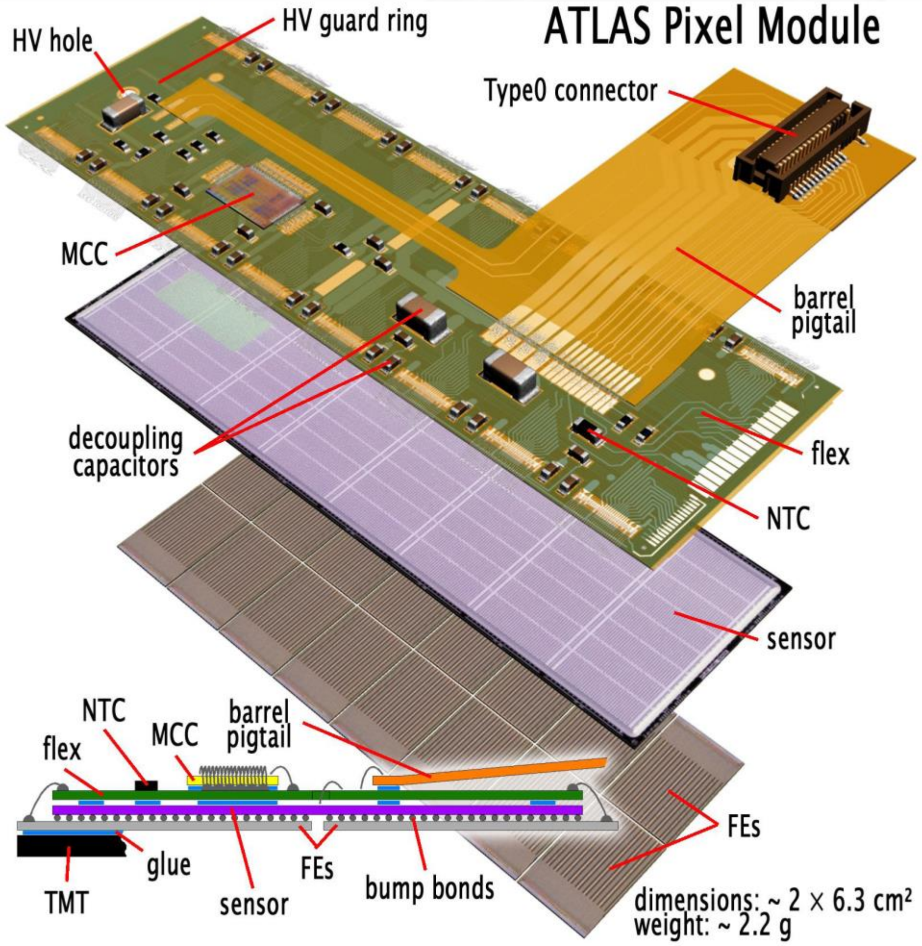
Hybrid Pixel Modules

- Basic building block of the pixel detector:
  - smallest detector unit which can be operated
- Hybrid pixel modules consist of:
  - sensor
  - FE-chip(s)
  - printed circuit board with components and interface to outer world
- Chip and sensor match on pixel basis:
  - chip covers full sensor area
  - FE and sensor pixel have the same size and are connected via bumps



Requirements of ITk pixel modules: Rates and radiation

Radiation levels:

- 10 Mgy and $2*10^{16}$ n_{eq}/cm^2 for the innermost layer

Readout:

- Trigger requirement
  - BC : 40 MHz
  - <L0 accept rate> : 1 MHz
  - Latency : 6 µs
- Readout pixel detector fully at L0
- Simulation say for inner barrel layer :
  Hit rate = 2 GHz/cm^2
- 1 MHz trigger rate
  ➔ 50 MHz/cm^2 hit rate
  ➔ 168 MHz/chip (FEI4 size)
- Data size : 16 bits/hit
  ➔ 2.7 Gbps/chip
- But need low latency
  - need to account for hit rate and trigger rate fluctuations

  ➔ **5 Gbps/chip**
  for inner barrel layer

Pixel structure	Dose (MGy)	Fluence (1MeV neq 10^{14} cm^{-2})
Inner Barrel	7.8	134.6
4th Barrel	0.43	9.4
1st Inner ring	0.95	17.0
Last inner ring	1.13	16.1
1st Outer ring	0.44	8.2

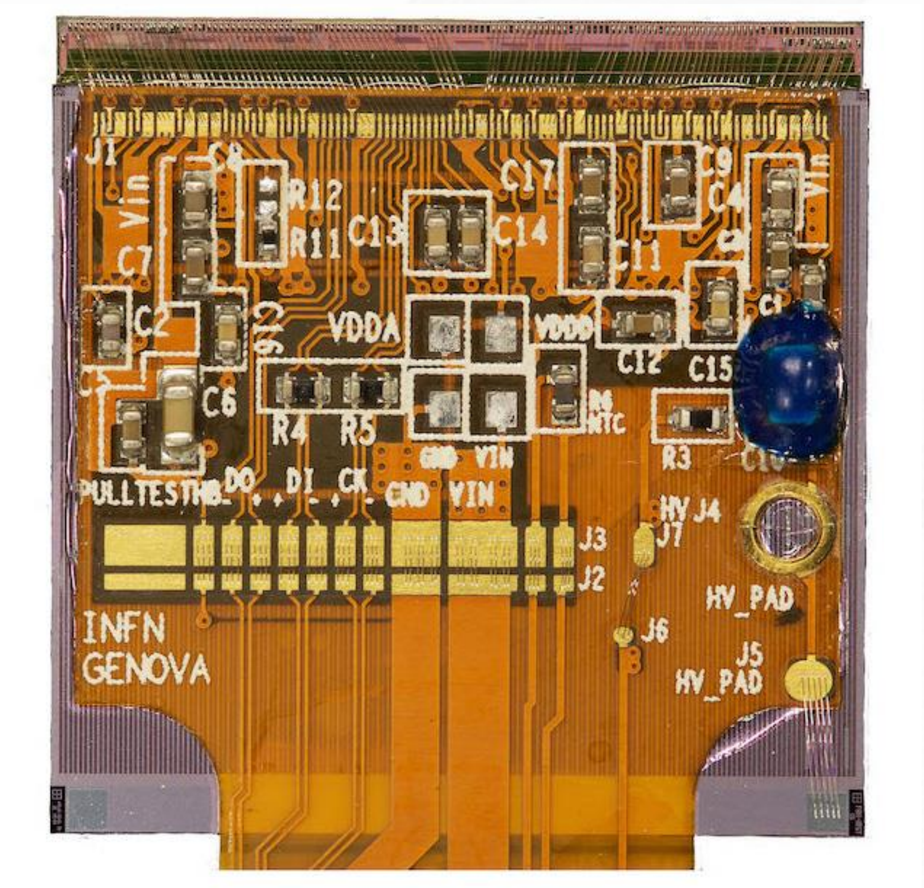
Pixel Detector	Module type	Rate/module (Mbps)
Barrel L1	2 chip	5120
Barrel L2	Quad	2 x 4000
Barrel L3	Quad	5120
Barrel L4	Quad	2560
Inner Ring	Quad	2560

from R. Bates, Vertex 2015

Assumes data on a quad multiplexed together

Requirements of ITk pixel modules: Power and Material

- Power budget for ITk modules:
  - inner layers: 0.7 W/cm^2 for chip and ~0.3W/cm^2 for sensor
  - outer layers: 0.5 W/cm^2 for chip and ~0.2W/cm^2 for sensor
- Material budget for ITk modules:
  - for IBL we achieved: ~0.6% X/X_0
  - for inner ITk layers: 0.5% X/X_0
  - outer layers, esp. 5th or 6th pixel layer could be relaxed: ~0.6 – 0.7% X/X_0



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Scale of the extended ATLAS pixel system

	Yield (%)
Sensor wafers	90
FE wafer	60
Bump-bond	90
Assemblies	95

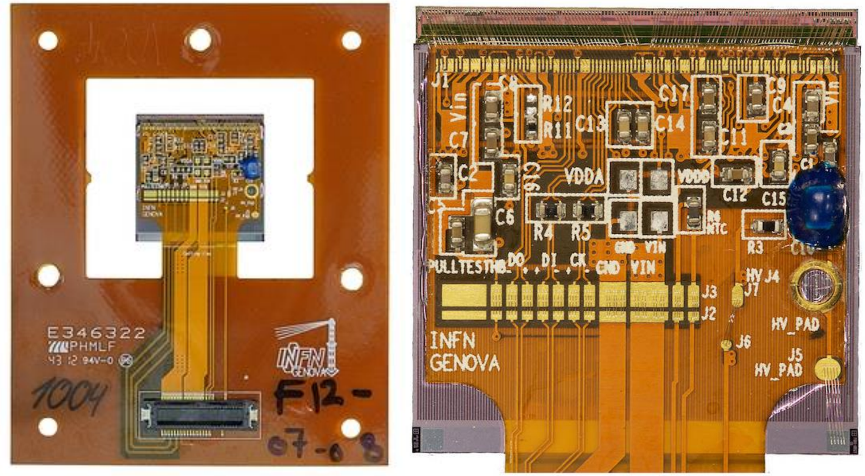
- An extended pixel system requires low cost pixel modules
- Assumed here a 6th pixel layer
  - 5 pixel layers area = 14 m^2

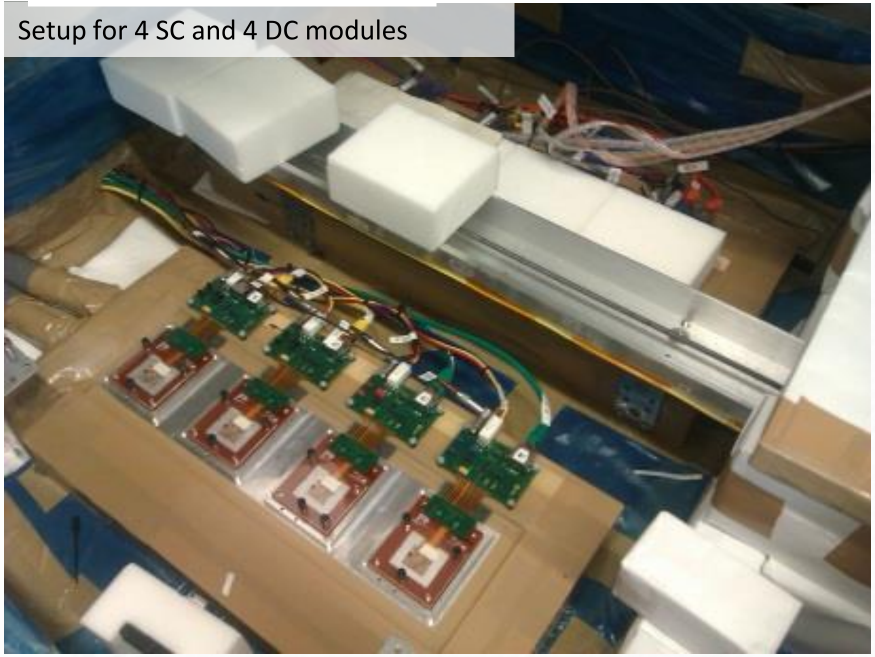
Item	Baseline (area = 8.76m^2)	Maximum Pixel system extension (area = 18m^2)
Number of good 2&4 chip modules	6436	13033
Number of 2&4 chip module flip-chip starts	7528	15244
Number of FE wafer bump deposition starts	333	684
Number of sensor wafer starts	1356	2785

from R. Bates, Vertex 2015

Module testing and qualification

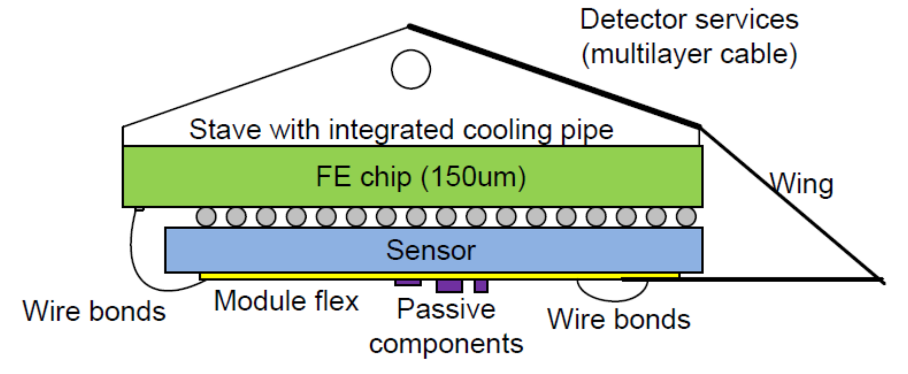
- Scale of the extended pixel system requires high production and testing throughput:
  - testability of the modules is an important requirement for the design!
  - modules must be robust and easy to handle before loading
  - need well defined interface for testing → need a test connector
  - handling and protection frame
  - robust shipping frame
  - integration of automated test and tuning routines in the electronics/chips

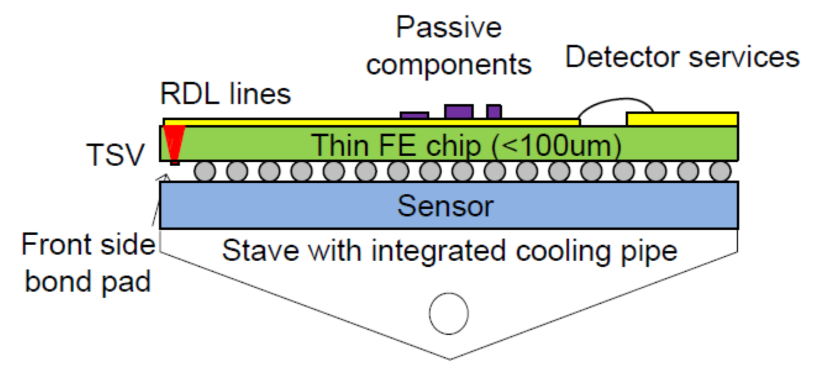



Setup for 4 SC and 4 DC modules

Module concepts

- module concepts don't differ so much for hybrid, monolithic or CCPD approach:
  - all need a kind of a flex hybrid for the passive components and the interface to the outer world
  - monolithic and hybrid are basically the same
- a TSV technology could help to make the module more robust, e.g. no wire bonds
- for CCPD other configurations are necessary:
  - chip size could be much smaller than sensor sizes
  - connection of both chips to the flex difficult due to face to face orientation





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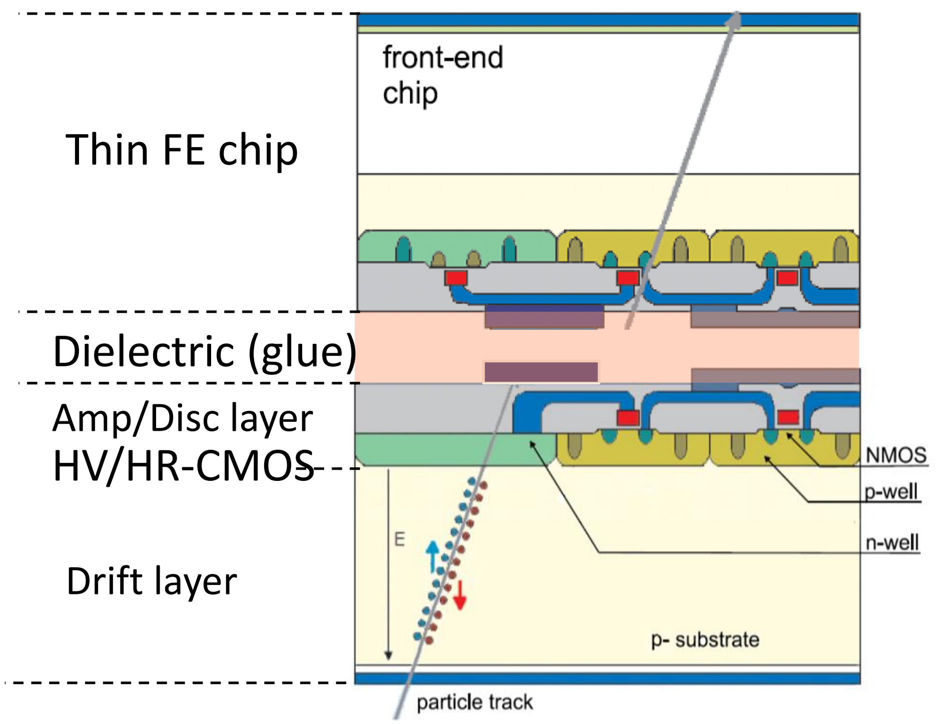
Gluing vs. bump bonding

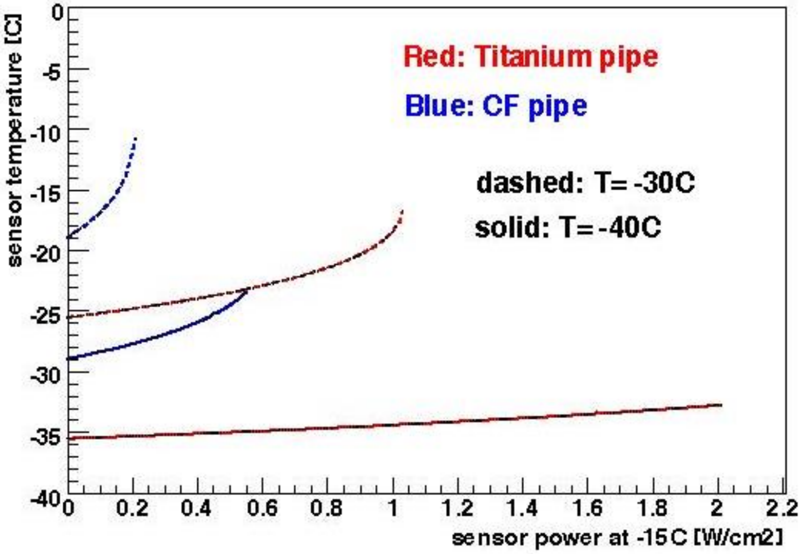
Gluing is a potentially cheaper hybridization technique for charge coupled devices (CCPD):

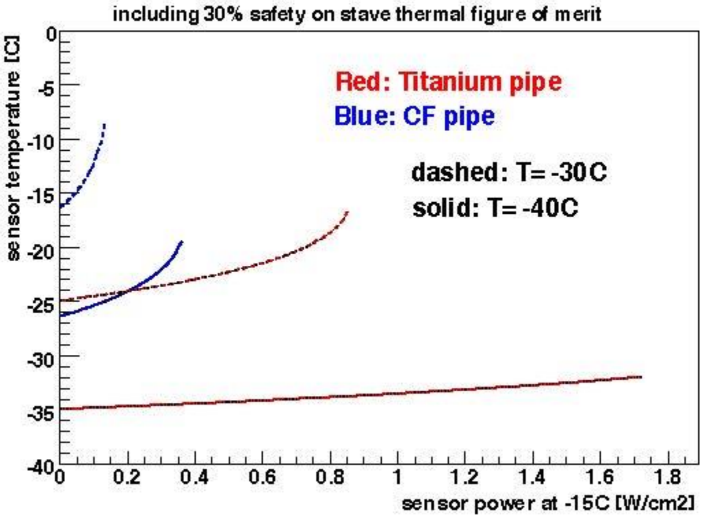
- But there are things to be considered:
  - procedure for a mass production must be developed and tested
  - cost reduction is probably not so big because only bump deposition and UBM can be omitted → assembly effort is roughly the same
  - still some conductive connections for power and data transmission are needed → not easy for same sized chip and sensor assemblies.
  - HV voltage connection maybe needed on sensor backside
- pure monolithic devices are obviously the best option!



Cooling issues

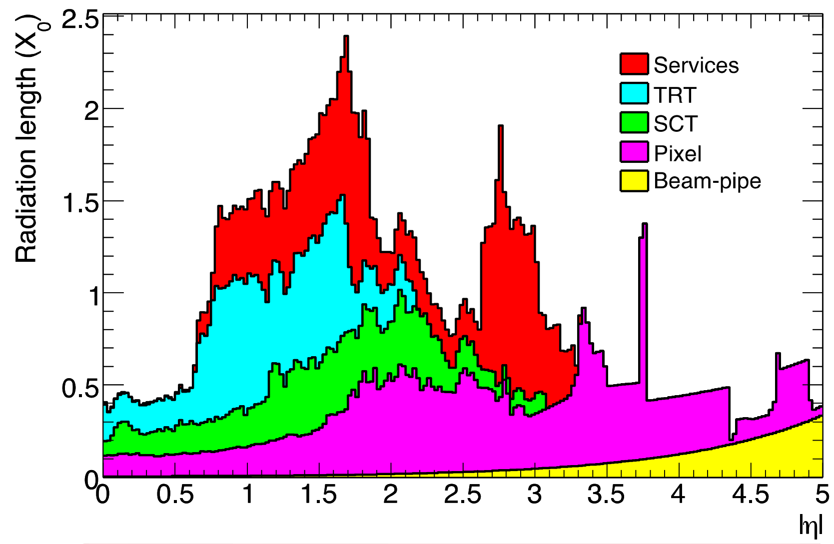
- Static cooling requirements are clear but there is still an uncertainty:
  - thermal runaway effects are a potential risk → we need the sensor power dissipation with fluence as input for the TFoM requirement of the cooling system
  - I expect that HR CMOS behaves similar as standard planar sensor silicon in terms of leakage current generation
  - A bit more unclear for LR or EPI materials and how the electronics affects all this?
  - This must be addressed for the CMOS sensors basically now!





Powering issues

- It is clear that for HL-LHC inner tracking detectors a usual direct powering scheme will not work!
  - service material budget in the active volume will be too high
  - we need a reduction of about a factor 5 to 10 which can only be achieved by DC-DC power conversion of SP concepts
- Both concepts have severe impact on the module design:
  - integration of regulators on chip and/or on module level
  - bypass and control schemes needed esp. for SP
  - data readout requirements (AC coupling etc,)
- Need to be addressed for CMOS now as well!



ATLAS Inner Det. Material Distribution

ATLAS Inner Det. Cables

ATLAS pixel detector services

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Conclusions

- Module design for the ITk pixel detector is constraints by many external factors beyond radiation levels, data rates and readout speed:
  - magnitude of module production requires a good testability, robustness and disfavors a large variation of module types
  - cooling, powering and loading requirements are important to understand inside the whole system
- For monolithic CMOS detectors many things are similar as for hybrid pixel modules:
  - benefit from solutions being developed now for hybrid by just copying them
  - but in the end all these issues must be addressed as well in time!
- For charge coupled CMOS detectors things could be quite different depending on the chosen option:
  - this may complicate life because one have to develop own solutions

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BACKUP

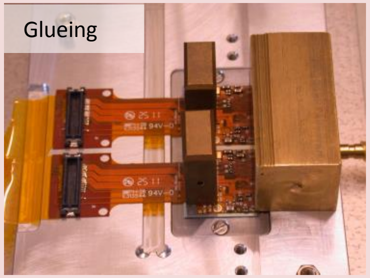
Modules of the IBL

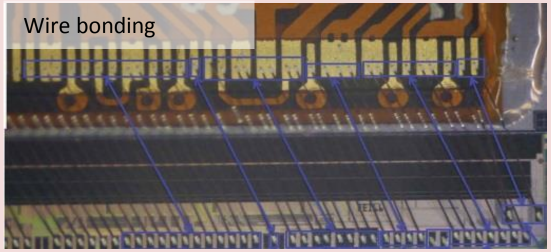
IZM (Berlin):

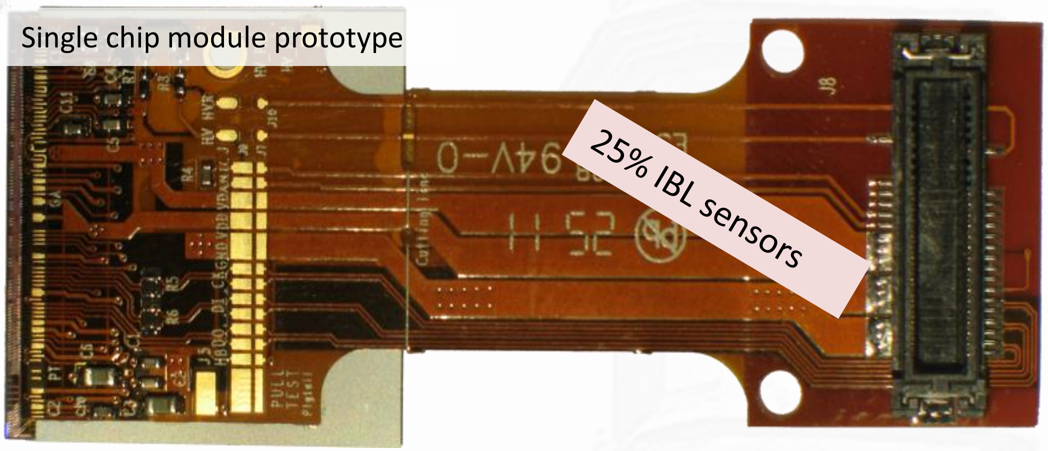
- bump-bonding of FE and sensor
- thinning of the FE-I4 wafer to 150 µm with glass handling wafer and dicing

At Bonn/Genova:

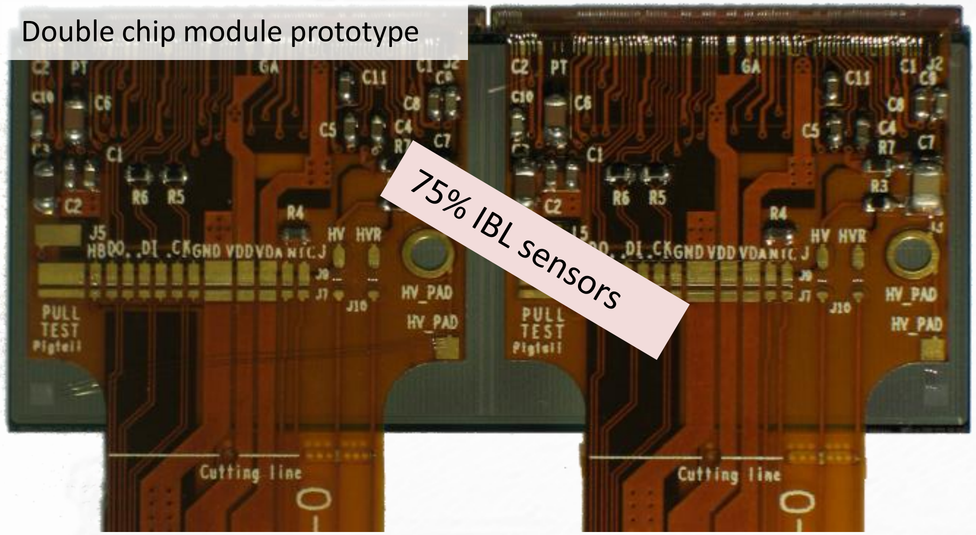
- Module assembly and QA


Glueing


Wire bonding


Single chip module prototype

25% IBL sensors


Double chip module prototype

75% IBL sensors

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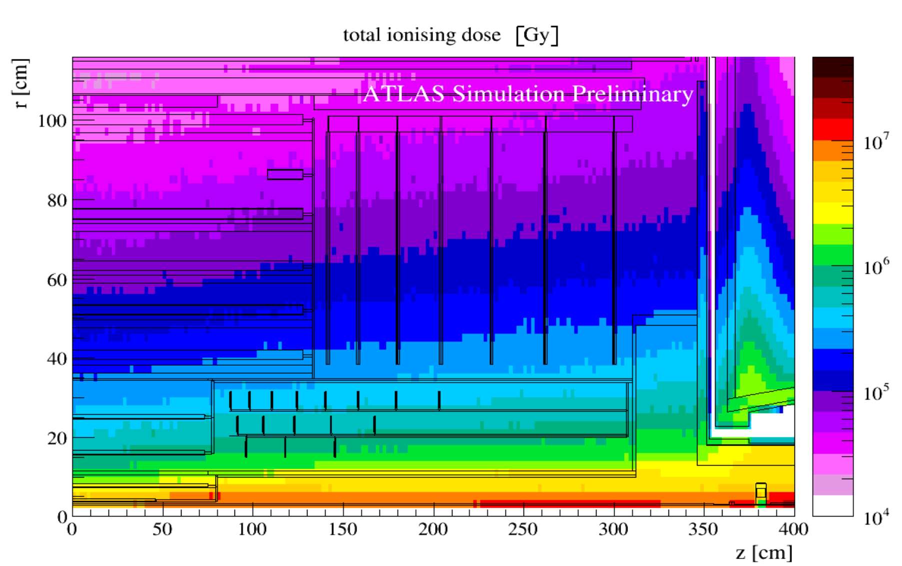
Basic Requirements of ITk pixel modules

- **Silicon damage (1 MeV) fluences** used to model Pixel and SCT leakage currents and depletion voltages, which allow us to anticipate detector performance over its lifetime, including S/N estimates, and required cooling performance
- **Ionizing dose** measurements important for predicting front-end chip performance
- **Charged particle fluences** allow us to estimate occupancies
- **Radio-activation** estimates can dictate procedures for cavern access and detector installation and maintenance



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