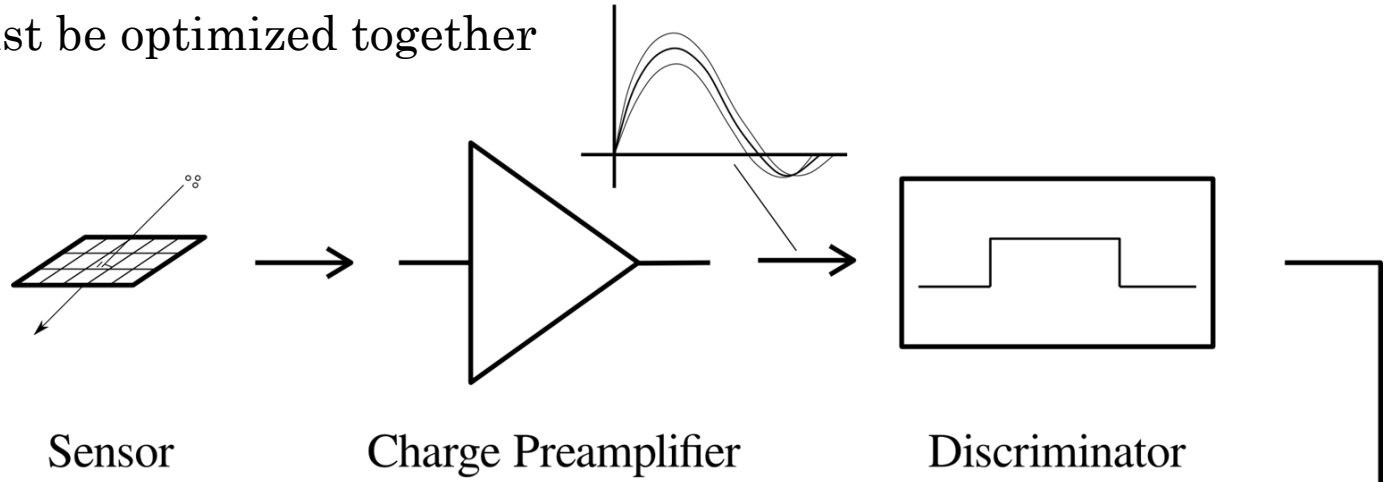
Pico-second TDC for HEP (and other applications)

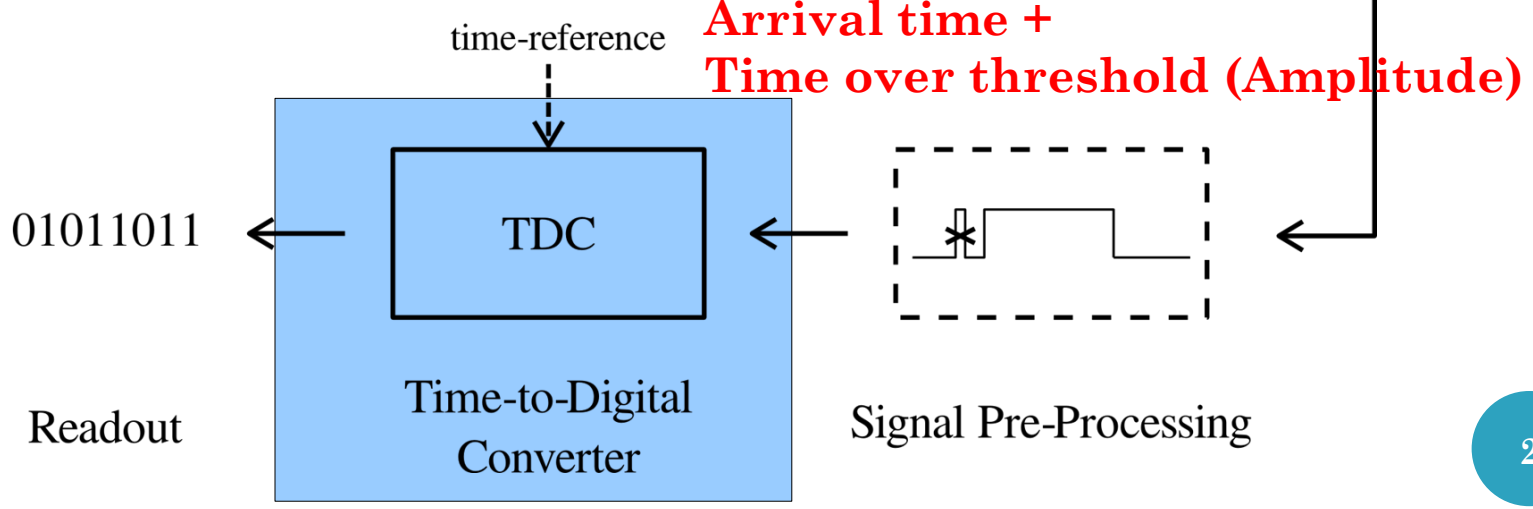
Jorgen Christiansen, Moritz Horstmann, Lukas Perktold (Now AMS), Jeffrey Prinzie (Leuven)

CERN/PH-ESE

Time Measurement Chain

Detector and discriminator critical
and must be optimized together





TDC APPLICATIONS IN HEP

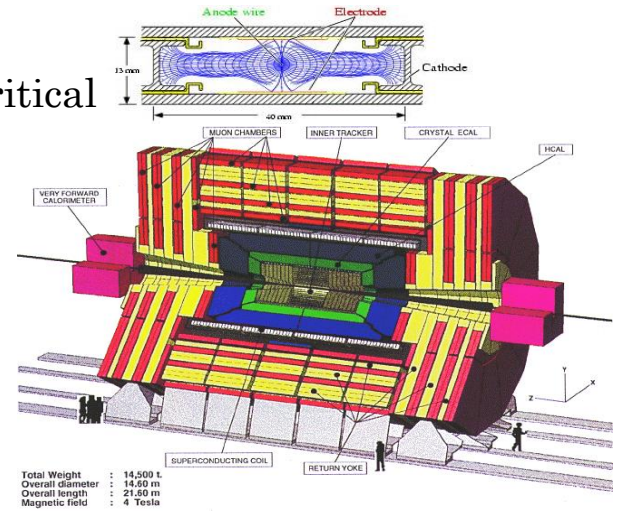
Large systems with many channels: 10k-100k

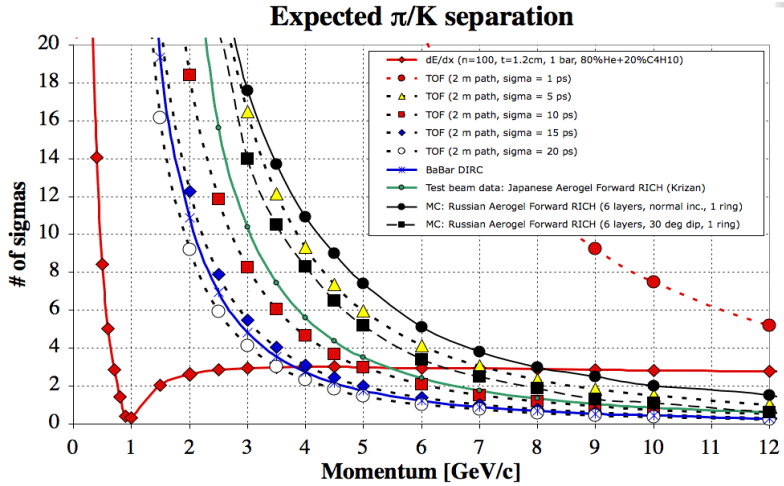
Single shot time resolution/stability across large system critical

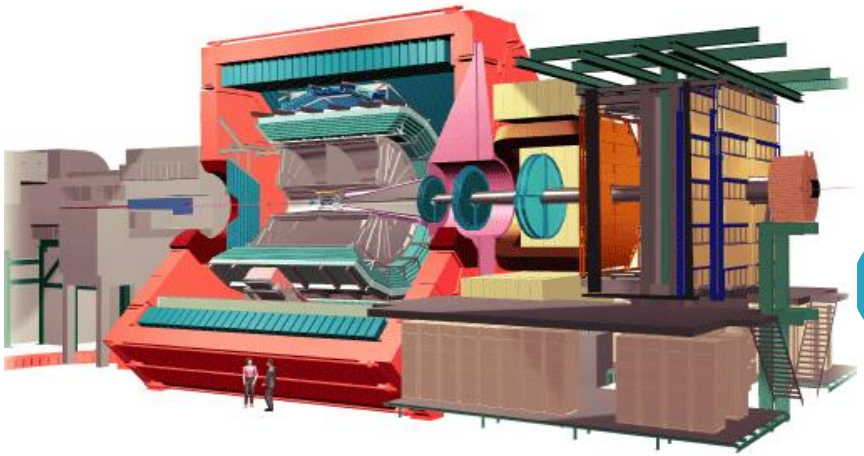
- Drift time in gas based tracking detectors
  - **Low resolution: ~1ns**
  - Examples: CMS, ATLAS, LHCb, , , drift tubes
- TOF, RICH
  - **High resolution: 1 – 100ps**
  - Example: ALICE TOF
- Background reduction: **1 – 10ps**
- Vertex identification from timing: **1 - 10ps**
- Signal amplitude and time walk compensation: Time Over Threshold (TOT)
  - Or Constant Fraction Discriminator (CDF) in analog FE
- Triggered or non triggered

New TDC with programmable resolution: 3ps, 12ps,

- Power consumption highly resolution dependent

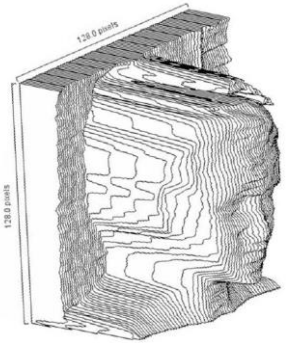


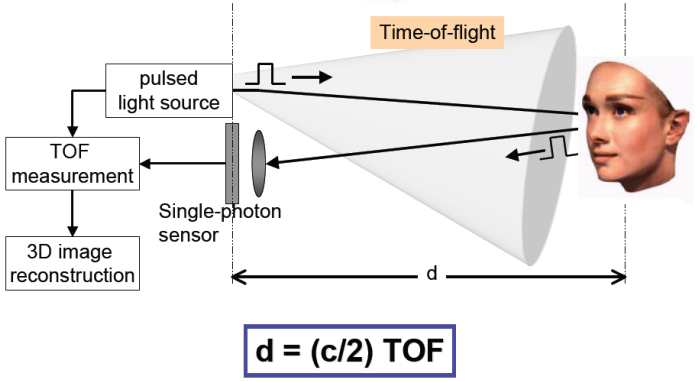




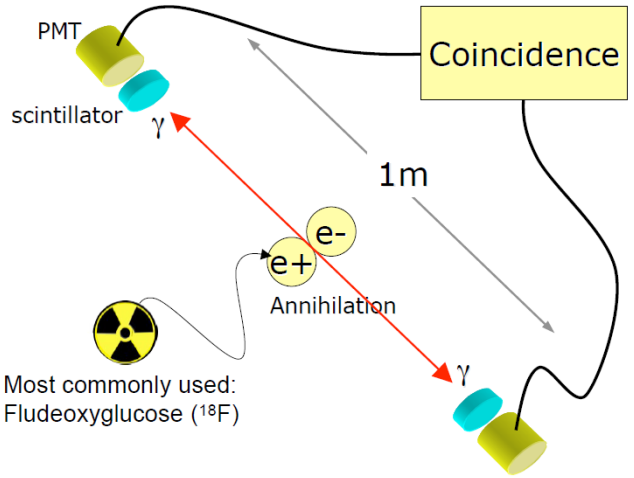
Other TDC applications

- Laser ranging
- 3D imaging
- Medical imaging: TOF PET
  - Improve signal/noise, lower radiation
- Fluorescence lifetime imaging
- General instrumentation.
- Differences to HEP systems
  - Small systems - Few channels
    - Time resolution/stability between few channels on same chip
  - Averaging can in many cases be used to get improved time resolution

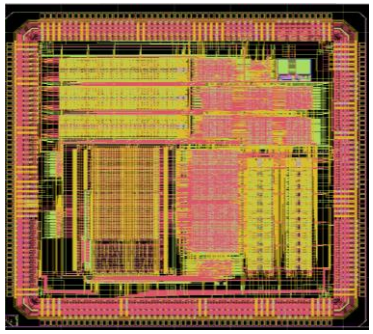




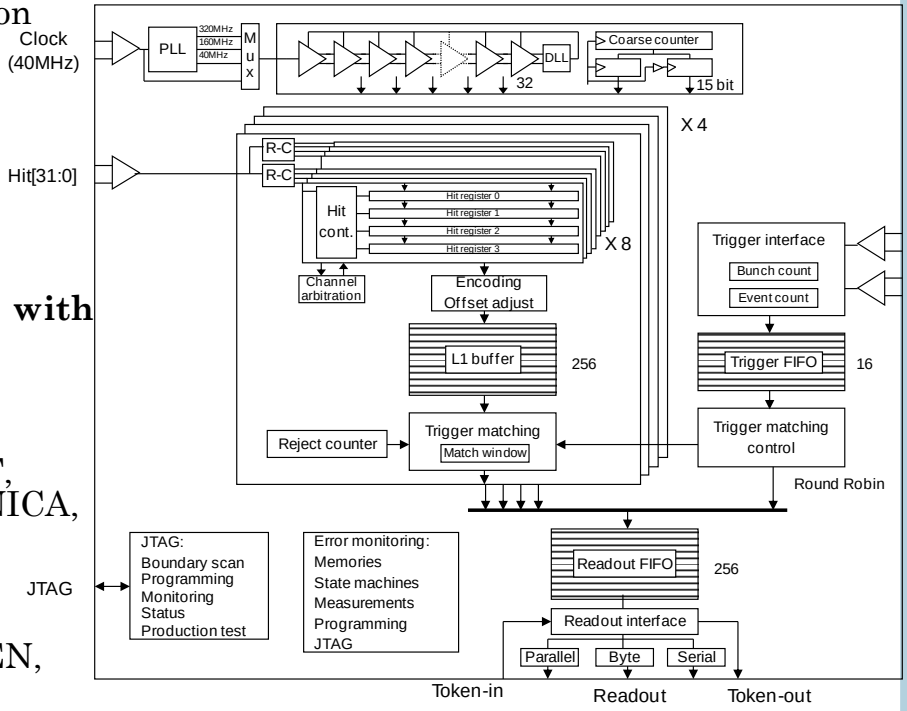
d = (c/2) TOF



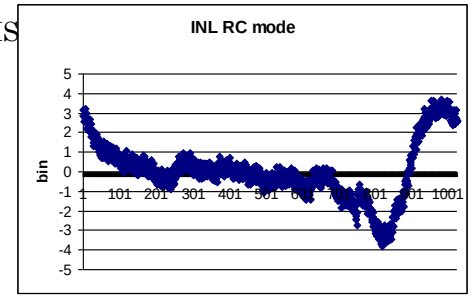
HPTDC



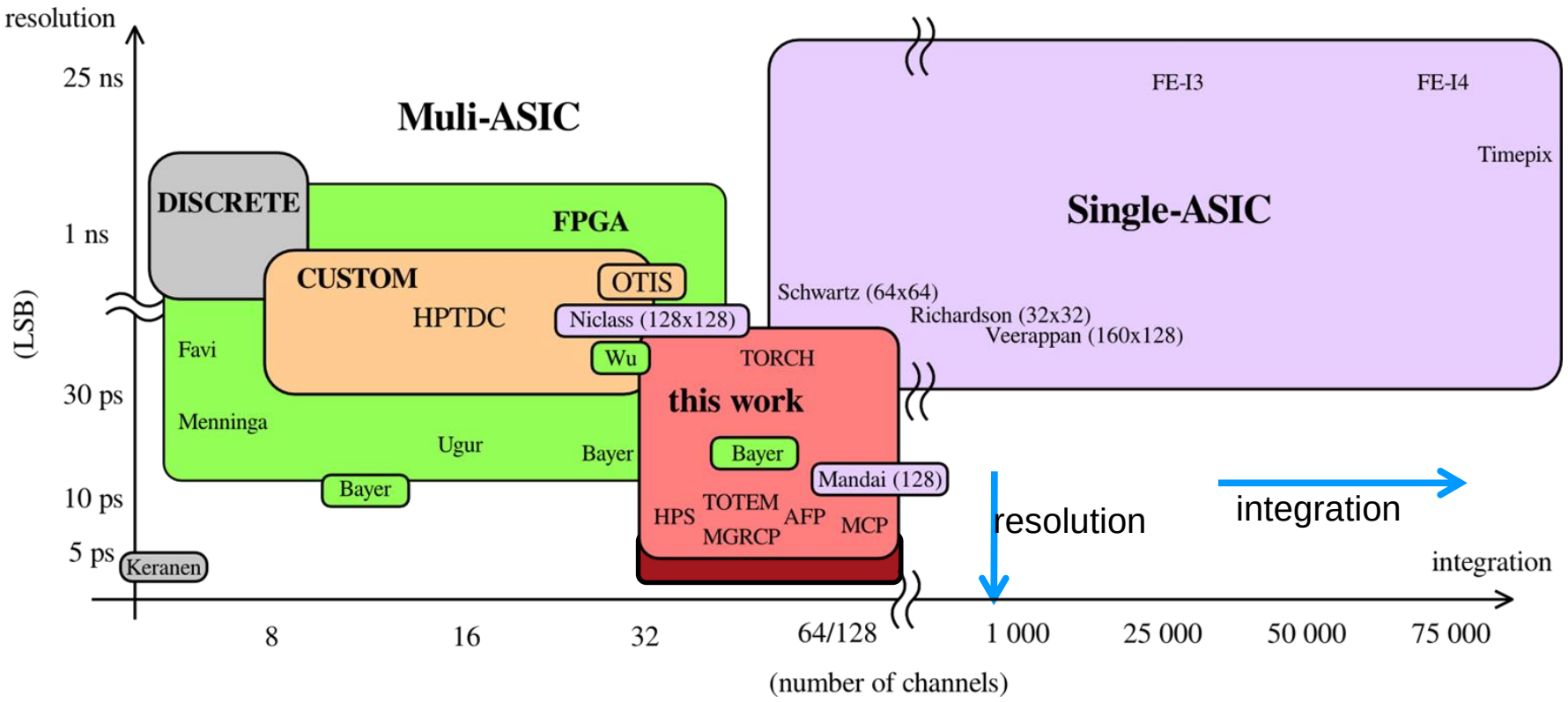
- History
  - Architecture initially developed at CERN for ATLAS MDT (design transferred to KEK)
  - CMS Muon and ALICE TOF needed similar TDC with additional features / increased resolution
- Features
  - 32 channels(100ps binning), 8 channels (25ps binning)
  - 40MHz time reference (LHC clock)
  - Leading, trailing edge and TOT
  - Triggered or non triggered
  - **Highly flexible data driven architecture with extensive data buffering and different readout interfaces**
- Used in large number of applications:
  - More than 20 HEP applications: ALICE TOF, CMS muon, STAR, BES, KABES, HADES, NICA, NA62, AMS, Belle, BES, , ,
    - We still supply chips from current stock.
  - Other research domains: Medical imaging,
  - Commercial modules from 3 companies: CAEN, Cronologic, Bluesky
  - ~50k chips produced
- 250nm technology (~10 years ago for LHC)
  - Development: ~5 man-years + 500kCHF.
  - Can not be produced any more
- http://tdc.web.cern.ch/TDC/hptdc/docs/hptdc_manual_ver2.2.pdf



17ps RMS



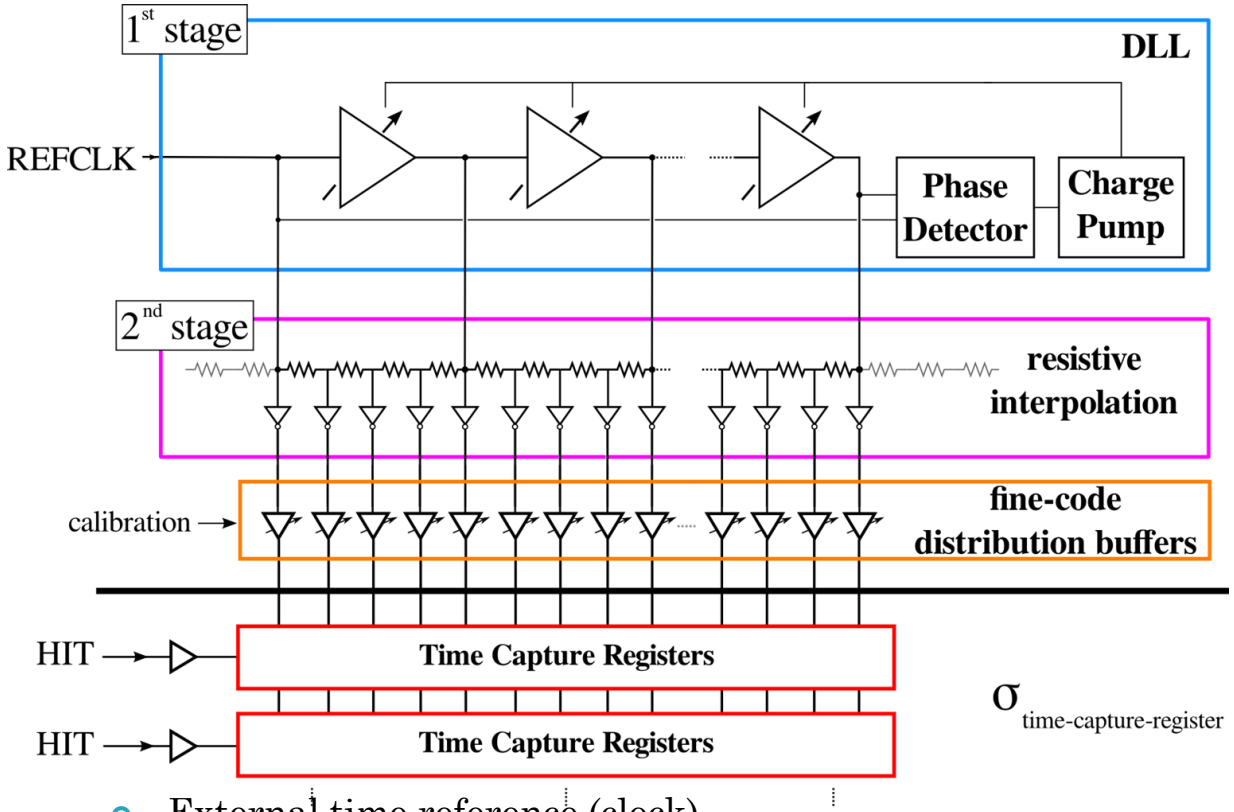
TDC Trends



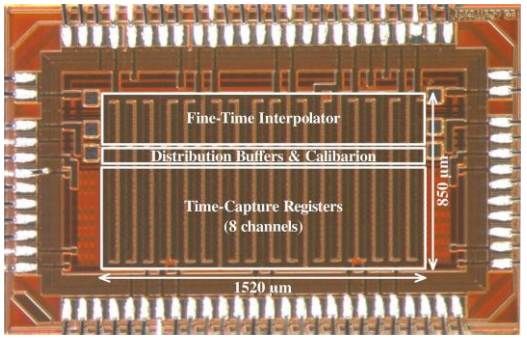
New detectors and sensors require new TDC

- **3ps binning (1-2ps RMS)**
- **High integration**
- **Flexible**

TDC ARCHITECTURE PROTOTYPED IN 130NM

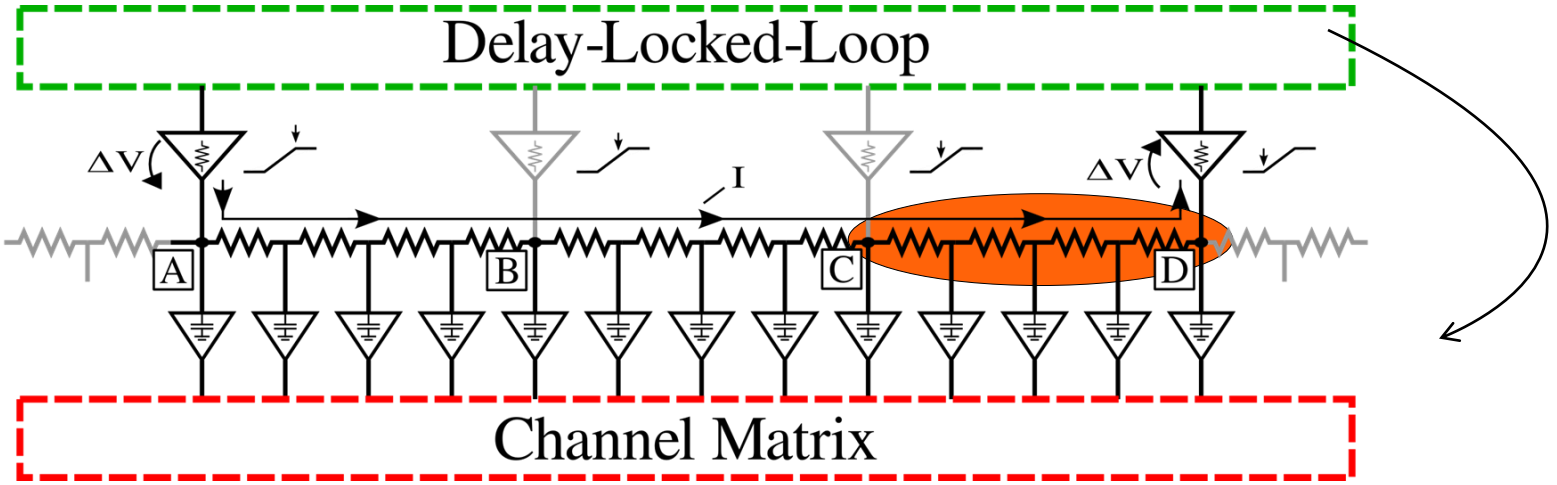


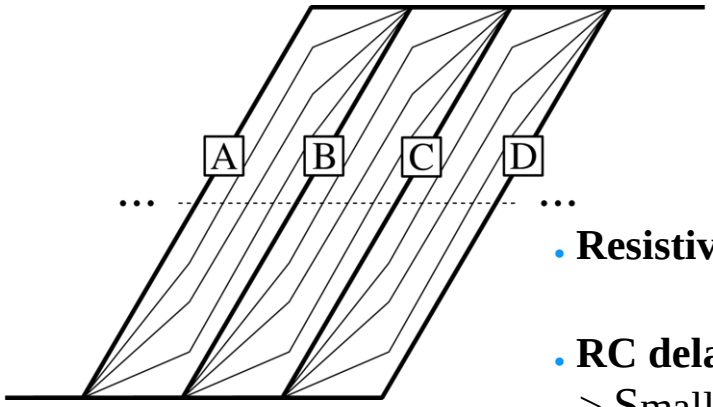
Counter

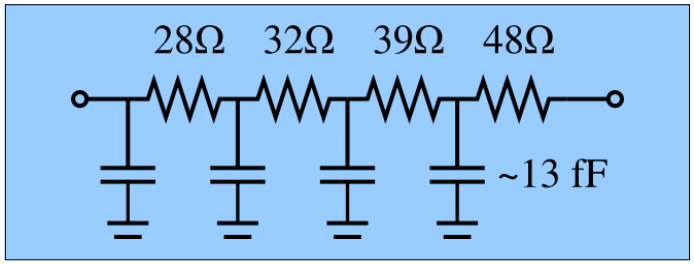


- External time reference (clock).
- 3 stage time measurement:
  - Counter: 800ps, Delay locked loop: 25ps, Resistive interpolation: 6.25ps (65nm: 400ps, 12ps, 3ps))
- Self calibrating using Delay Locked Loop (DLL)
- Can be scaled to the number of channels required.
- Prototyped in 130nm CMOS and extensively characterized by Lukas Perktold.
- Measured time resolution: 2.5ps RMS

Resistive Interpolation



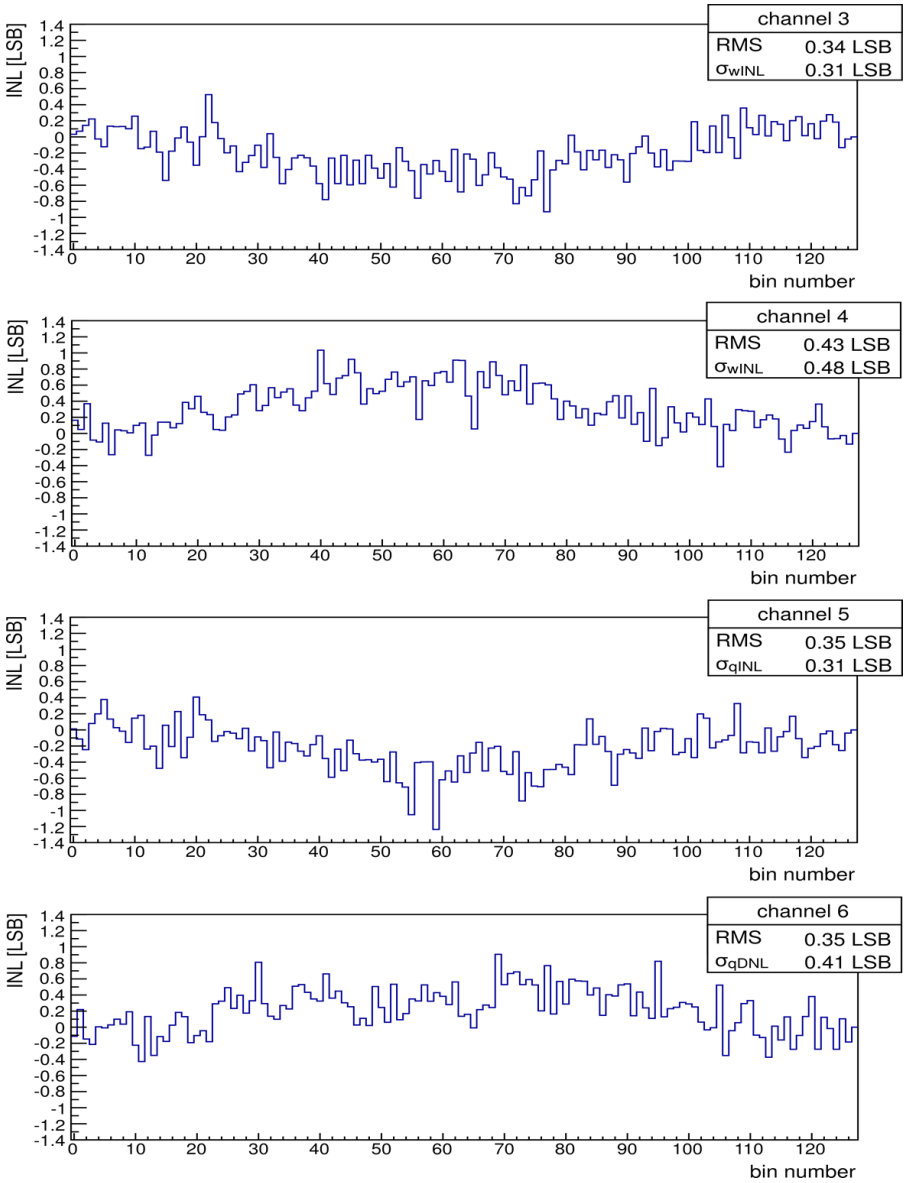




- **Resistive voltage divider**
  -> Signal slopes longer than delay, stabilized by DLL
- **RC delay** (capacitive loading)

- > Small resistances, small loads
- > Simulation based optimization of resistor values

Measured performance



INL = ± 1.3 LSB

RMS = < 0.43 LSB (2.2 ps)

Expected RMS resolution from circuit simulations:
including quantization noise, INL & DNL

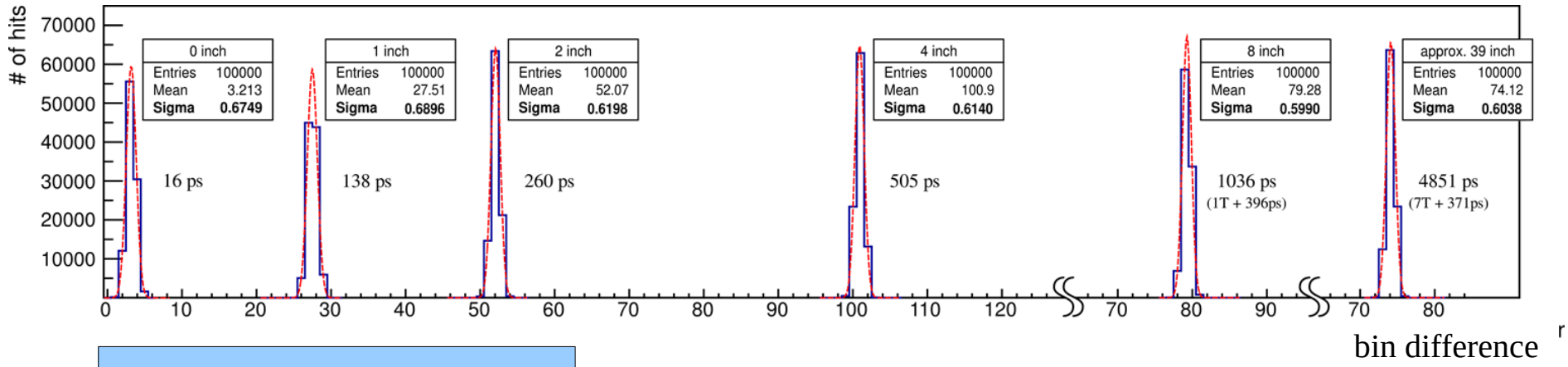
2.3 ps-RMS < $\sigma_{qDNL/wINL}$ < 2.9 ps-RMS

INL can be corrected for in software

DNL, Noise and jitter can not be corrected
(single shot measurements)

Single Shot Precision

- Three measurement series using cable delays
  - Both hits arrive within one reference clock cycle
  - Second hit arrives one clock cycle later
  - Second hit arrives multiple clock cycles later (~5ns)



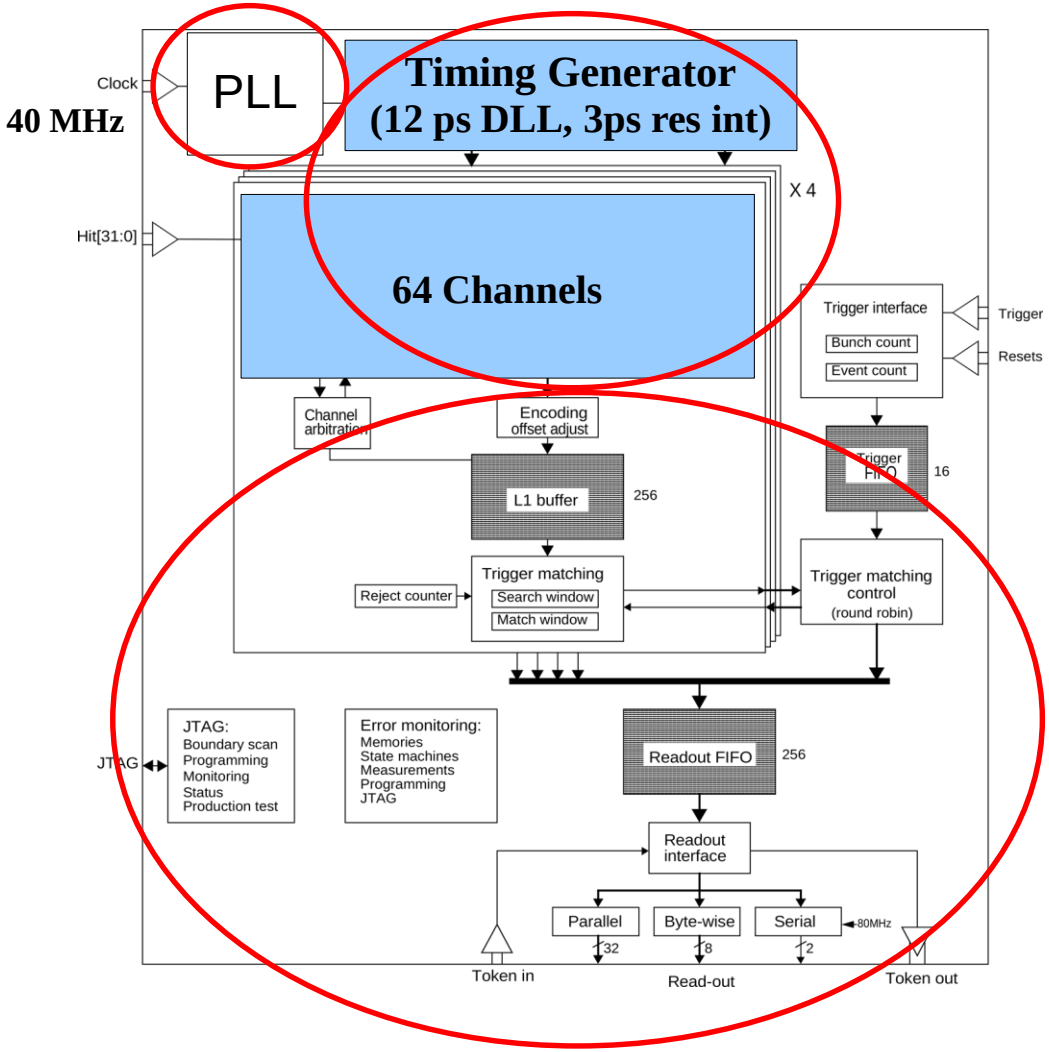
σ_{TDC} < 2.44 ps-RMS

TWEPP2013 slides and paper: https://indico.cern.ch/event/228972/session/6/contribution/61
ESE seminar: https://indico.cern.ch/event/225547/material/slides/0.pdf

Mapping to 65nm

- Uncertain long term availability of IBM 130nm
- 2x time performance: -> 3ps binning
- Lower power consumption: < ~½
  - ~1/8 if DLL binning of 12ps enough (RMS ~4ps).
- Larger data buffers
- More channels
- Smaller chip
- But higher development costs
  - MPW prototyping: ~80k
  - NRE for production masks: ~500k
    Find other project(s) for shared production masks

FULL 65NM PS TDC ASIC



Channels: 64

Binning: 3ps, 12ps, (400ps)
RMS: 1-2ps, ~4ps

Reference: 40MHz clock

Dynamic range: 100us (12bit@40MHZ)

Leading, Trailing, TOT

Hit rate: < 320MHz/channel

Data buffers per channel
(~256 hits per channel)

Triggered/un-triggered

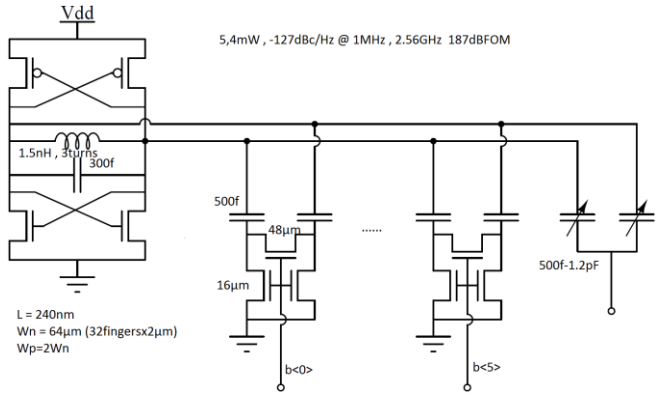
4 readout FIFOs

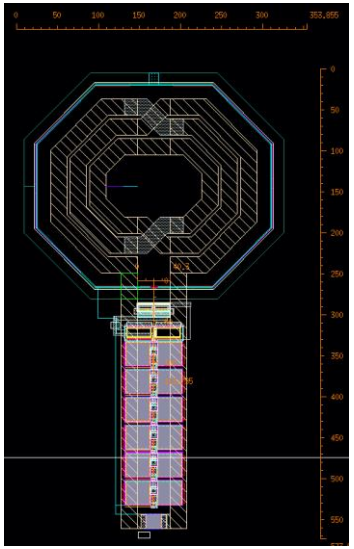
Flexible readout interface

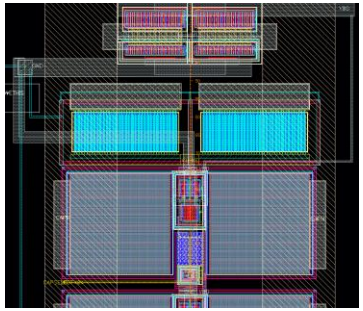
Power: ~1W – ¼ W

Low jitter PLL

- Clock multiplication from 40MHz to 2.56GHz for course time counter and time interpolator
  - Low jitter critical: < 1ps
  - Jitter filtering of 40MHz clock to the extent possible
    - 40MHz reference MUST be very clean
  - LC based oscillator
- Internal clock for logic and readout: 320MHz
- Design: Jeffrey Prinzie, Leuven
- Status/plans:
  - PLL circuit analysed and simulated at schematic level.
  - Detailed layout and optimization
  - Prototype submitted May 2015 (Synergy with LPGBT PLL)

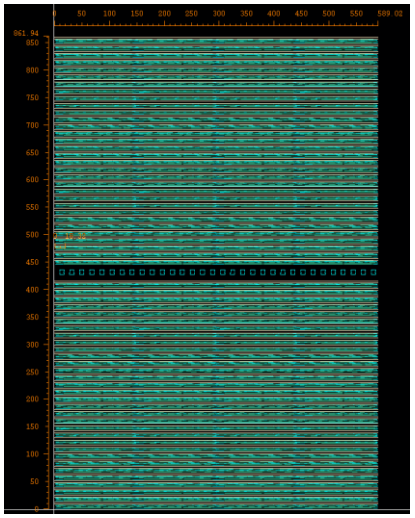


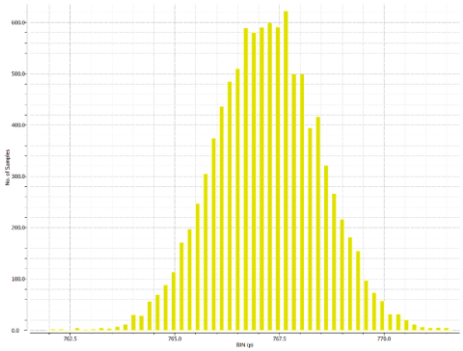




Time interpolator and hit registers

- Full custom layout in 65nm
- Done (95%):
  - 12ps binning DLL
  - 3ps binning resistive interpolation
    - Can be disabled for lower power (~1/4)
  - Timing distribution in array
  - INL adjustment/correction
  - Hit register optimization:
    - Critical for power consumption: 64 x 128 = 8K hit registers clocked at 2.56GHz, plus time decoding pipeline (total ~24K FF)
  - Pipelined time decoding
    - Time critical pipelined time decoding at 2.56GHz
- To be done
  - Integration in global RTL, Final layout integration, optimization and verification
- Designer: Moritz Horstmann

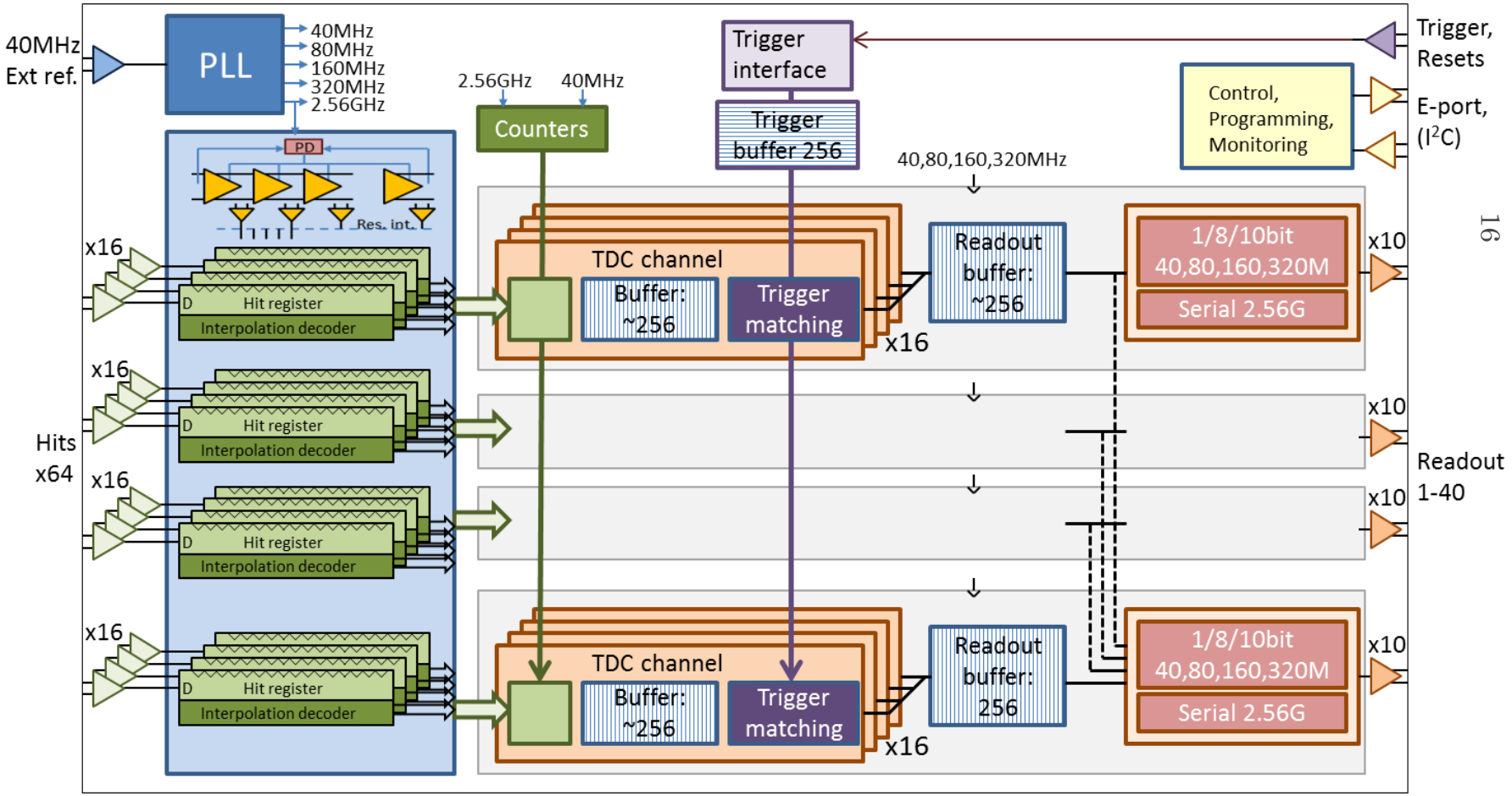




TDC LOGIC

- Synthesized logic from Verilog RTL
- Based on data driven architecture from HPTDC
  - Simplifications with individual buffers per channel
  - Clocking: 320, 160, 80, 40 MHz (hit rates and power consumption)
  - Trigger matching based on time measurements
  - New/additional features ?
- Reuse of HPTDC verification environment
  - This is ~½ the design effort !.
- New interfaces to be defined and implemented
  - Control/monitoring, Trigger, Readout
- SEU/radiation tolerance
  - 65nm technology TID tolerant
  - SEU detection and minimize effects from SEU when it can have major consequences (system sync)
    - As done in HPTDC
  - Not classified as rad hard
- Planning:
  - Verilog code implementation and simulation: March – December 2015

PicoTDC architecture



64 channels, 3ps or 12ps time binning

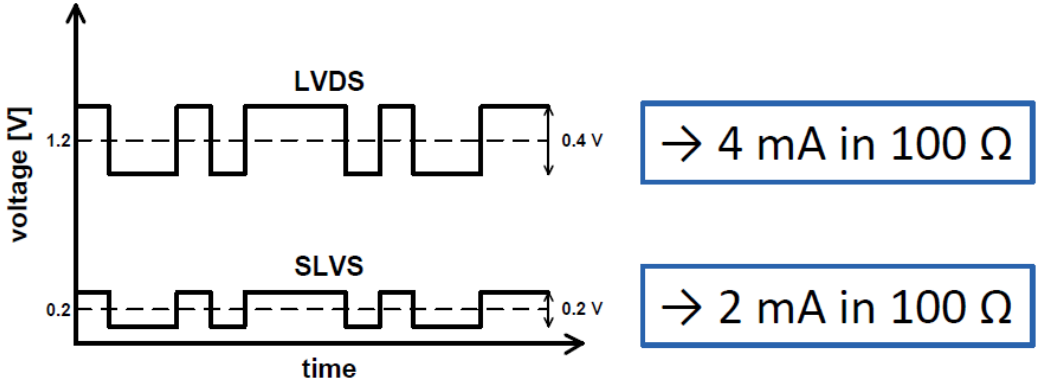
64 channels, 3ps: ~1W

64 channels, 12ps: ~0.4W

32 channels, 12ps: ~0.2W

Interfaces

- Power: 1.2v, ~1.0W (64 ch, 3ps),
  ~0.4W (64ch, 12ps)
  ~0.2W (32ch, 12ps)
  - (Not yet defined if 1.5v/2.5v for LVDS IO)
- Hits: Differential SLVS (LVDS)
- Time reference: 40MHz SLVS
  - Other clock frequencies required ?.
  - Low jitter reference critical for high time resolution (especially for large systems time measurements across many channels/chips/modules)
- Trigger/BX-reset/reset: Sync Yes/No, Encoded protocol
- Control/monitoring: GBT E-link and I2C
- Readout SLVS: 4 readout ports of 1-10 signals
- (JTAG boundary scan + production test ?)
- Packaging: ~250 FPBGA



Schedule

- Interpolator circuit prototype: Done
- Technology choice: Done
- Final Specifications: Q1 2015
- Finalize TDC macro: Q1 2015
- PLL prototype: Q2 2015
- Final RTL model: Q4 2015
- P&R and Prototype submission: **Q1 2016**
- Prototype test: Q2 2016
- Final production masks/prototype: Q3 2016
- Production lot: **Q4 2016**

Resources

- R&D
  - 2-3 man-years chip design:
  - Main designer: Moritz Horstmann (“new” CERN fellow)
  - PLL: Jeffrey Prinzie, Leuven (synergy LPGBT)
  - Supervision: Jorgen Christiansen
  - Low jitter/power SLVS differential: Synergy with LPGBT
  - Contribution from others ?
    - Interfaces/RTL/FPGA test board: Paul Davids, Alberta ?
    - Testing/characterization ?.
  - ~100k CHF prototyping, packaging, testing: ~Funded
- Put in production
  - ~500k: NRE , Packaging, test
  - Shared engineering run?.
    - We may have to contribute 250k – 100k.
  - Funding from clients/users/projects required
    - No large user that can pay it all
    - To be defined in detail in 2016, When full prototype available.
      - Entry price to get access to chips
      - Pro-rata to number of required chips

Users/ clients

- No commercial multi-channel TDC of this type available
  - That's the reason that so many have used the HPTDC
- CERN HEP:
  - TOTEM
  - CMS HPS and ATLAS FP420 (very forward detectors)
  - LHCb Torch (upgrade option)
  - CMS endcap Calorimeter with timing ?
  - ATLAS muon upgrade ? (low resolution)
- Other HEP
  - TICAL
  - PANDA, CBM
  - Many experiments needs multi channel high/low resolution TDC
  - Many would like to explore ps timing as new "dimension" in HEP experiments. Detector and analog FE critical (e.g. CFD)
- Non HEP research
  - Medical imaging: TOF PET
  - Florescence imaging
  - Other
- Instrumentation:
  - CAEN, , ,
- Other "clients" will show up when working device available
- TDC users meeting Feb. 12: https://indico.cern.ch/event/366097/

Backup slides

Next – next generation: Femto-TDC

- Sub 65nm technology
- More channels ?
  - Anybody needs more than 64 channels per chip ?
- Better resolution ?
  - Does anybody have a detector with sub-ps resolution ?
  - How to use sub-ps at system level ?
- Lower power ?
  - We always want lower power
- Higher rates ?
- Higher integration ?
  - Integrate analog front-end plus CFD (makes chip detector specific)
- Novel applications
  - SPAD arrays with ~ps TDC
    - https://indico.cern.ch/event/121655/
    - https://indico.cern.ch/event/149010/
  - SI-pixels with high time resolution
    - https://indico.cern.ch/event/302077/
    - https://indico.cern.ch/event/267425/
  - Other ?

Readout

- 1 or 4 readout ports
  - 4 ports: High rate applications (e.g. non triggered)
    16 TDC channels per port
  - 1 port: Low-medium rate
    64 channels (or 32channels in 32 channel mode)
- Readout data: 32bit words
  - Headers, trailers, TDC data, status, etc.
- Readout ports interface
  - Byte wise:
    - 40, 80, 160, 320 MHz
    - Clock driver by data destination (FPGA or GBT): **To Be Confirmed**

    A. 8bit data with data strobe, event strobe (driven by TDC)

    B. 8B/10B encoded

    - **(way to block data flow ?: X-on – X-off)**
  - Serial:
    - 8B/10B or 64B/66B encoding
    - Low speed: 40, 80, 160, 320 Mbits/s
    - High speed: 2.56 Gbits/s
- TDC readout bandwidth:
  - Max:
    320MHZ x 8 x 4 = 10Gbits/s (~4Mhits/s per channel without triggering)
    2.56Gbits/s x 4 = 10Gbits/s
  - Min: 1 x 40Mbits/s= 40Mbits/s

Framing

- Triggered: Event framing
  - Event header
  - TDC measurements (relative to trigger)
    - Single edge
    - Leading + TOT
  - (Errors, per event)
  - (Debugging, per event)
  - Event trailer
- Non triggered: Stream of individual channel TDC measurements
  - TDC measurements (absolute)
    - Single edge
    - Leading + TOT
  - (Errors, when they occur)
  - (Debugging, when ?)
  - (Counter overflow)
- Idle/empty frame/byte
  A. No date strobe
  B. Idle character in 8B/10B or 64B/66B encoding

Data Type identification

"4" bit data type identifier in 32bit words.

- TDC measurements: Maximize number of bits (31) available for TDC data
  - Type: 0xxx (xxx part of channel ID)
- Header: Triggered
  - Type: 1000
  - Event ID: 12bit
  - Bunch ID: 12 bit
- Trailer: Triggered
  - Type: 1001
  - Event ID: 12 bit
  - Status/error flags: 8bits
    - Buffer overflows encountered.
    - ?
  - Number of hits or Check sum: 8bits
- Errors: Triggered or non triggered (can be enabled/disabled)
  - Type: 1010
  - Status word with bit signalling what error
    - Buffer overflows, Hit error (time decoding), PLL loss of lock, DLL loss of Lock, SEU detect ?
  - Error flags reset after having sent error status

  (error flags can also be read and reset via control/monitoring interface)
- Monitoring/debugging: Triggered (can be enabled/disabled), **To be determined**
  - Type: 1011
  - Buffer occupancy full: 64 L1 buffers * 10bit + 4 Readout FIFOs * 10 bit = 720bits !
  - Buffer occupancy short: 2bits per buffer: 144 !.

  (can also be read via control/monitoring interface)
- Counter overflow
  - Type: 1100
- Other ?

32bit frames

TDC measurement

Event header

Event trailer

Errors/status

Monitoring data, possibly with sub-types to read out all buffer occupancies

Coarse count overflow

“Absolute” TDC data

- 4 readout ports, 16 channels
  1 readout port, 32 channels

16/32 channel mode: FULL TDC data, **DEFAULT FORMAT**

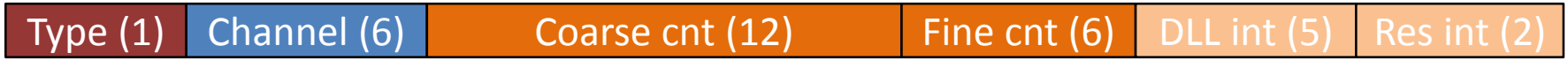
“Absolute” TDC data

- 1 readout port, 64 channels

DEFAULT: One course count bit less:

POSSIBLE OPTIONS: To be define which ones to implement

No edge bit: If only measuring leading or trailing



No resistive interpolation:

(No type identifier: Exception , use of 8B/10B, 64B/66B to mark when no data !)

Leading + TOT

- Packet Type: 1bit
- Channel ID: 4 - 6 bits
- Leading: >16 bits
  - Large dynamic range
    - 16bit 3ps resolution: 200ns
    - 19bit 3ps resolution: 1600ns
  - **Programmable part of full 25bits leading TDC**
  - (**Relative to trigger to be useable**)
- TOT (Relative to leading): >8 bits
  - Short dynamic range:
    - 8bit 3ps resolution: 780ps
    - 11bit 3ps resolution: 6.1ns
  - **Programmable part of full 25bits TOT difference**
    - TOT assumed to be used for offline time-walk correction of leading.
- Alternative: Readout of Individual Leading and Trailing edges with full range/resolution
  - 2x readout bandwidth

4 readout ports, 16 channels

1 readout port, 64/32 channels

Relative to trigger

A. Single edge
B. Leading + TOT with prog. Resolution

A: Triggered with relative time: Same as absolute

4 readout ports, 16 channels or 1 readout port, 32 channels

1 readout port, 64 channels

B: Triggered with relative leading and TOT: Same as absolute Lead. + TOT

4 readout ports, 16 channels

1 readout port, 64/32 channels

Buffering and readout architecture

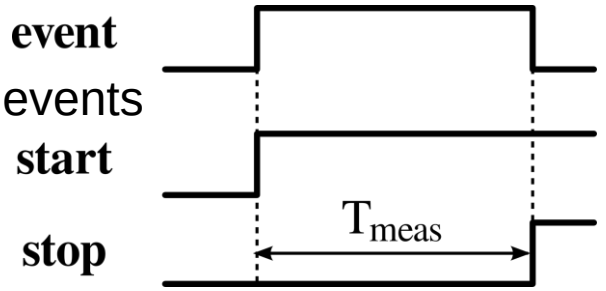
- Hit buffer per channel: ~256 hits
- Trigger matching/data merging into readout FIFOs organized in groups of 16 channels
  - 4 readout FIFOs of ~256 hits
  - 1 readout FIFO if only using 1 E-port
- Readout interface: Connecting to GBT and FPGA's
  A. 1-4 E-links, one for each group:
     - Max: 8 x 320Mbits/s = 2.5Gbits/s
  B. 1-4 high speed serial 2.5Gbits/s

  Max bandwidth: 10Gbits/s
- Data format: 32bit data words
  - Triggered: Event frame with header, TDC data, Trailer
  - Non triggered: Stream of TDC measurements

Time Measurements

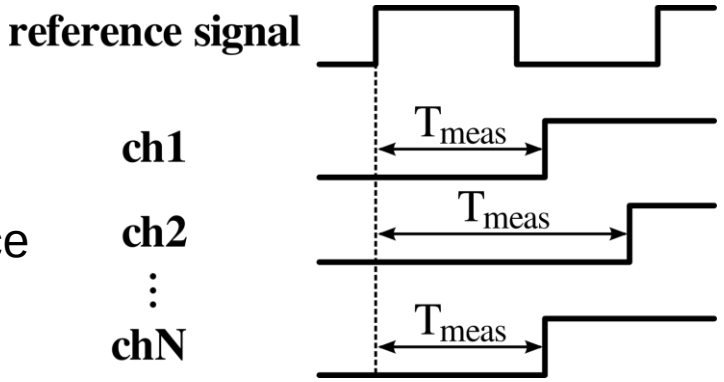
Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications

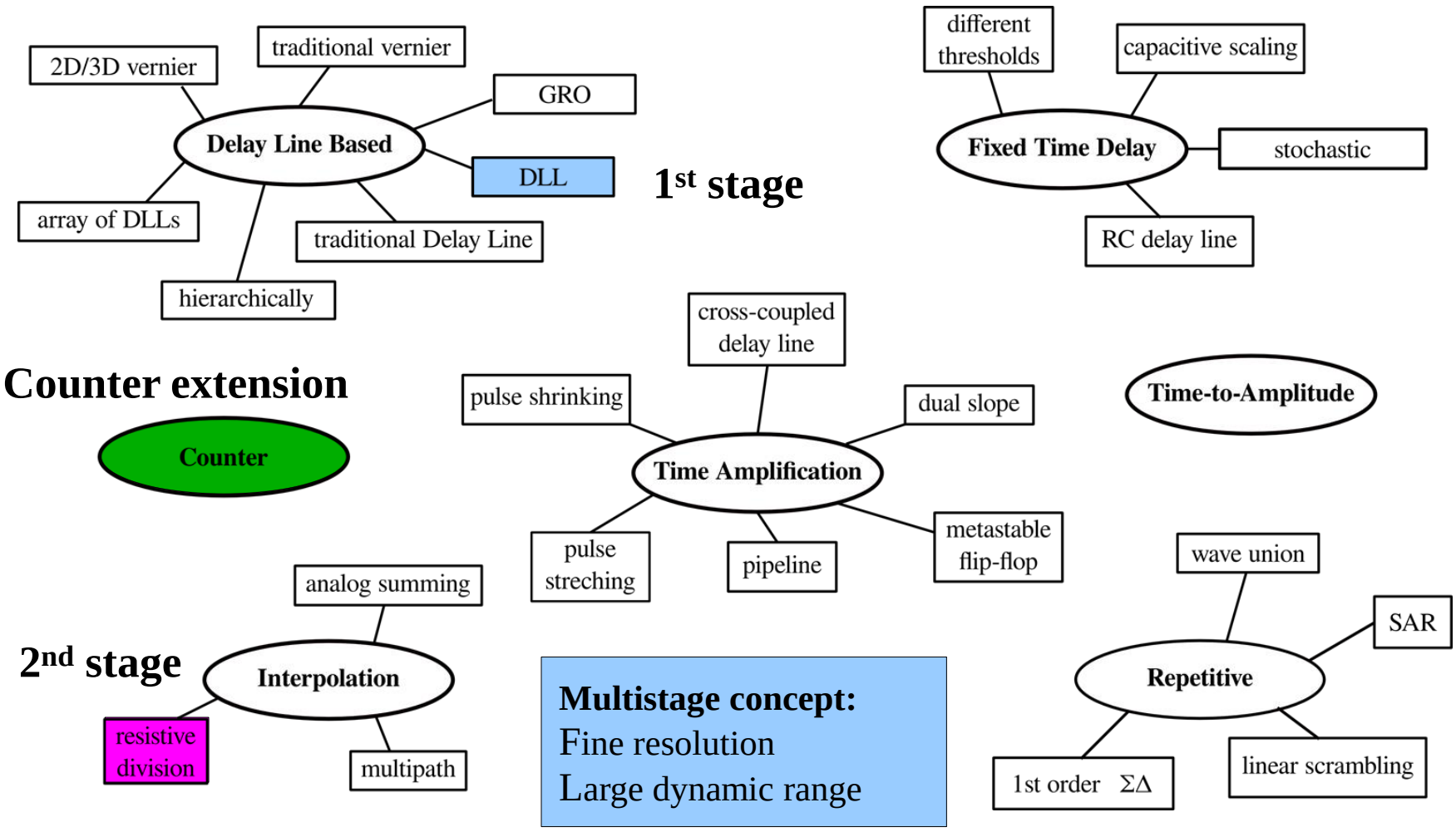


Time Tagging

- Measure “absolute” time of an event
  (Relative to a time reference: clock)
- For large scale systems with many channels
  all synchronized to the same reference



TDC Architectures

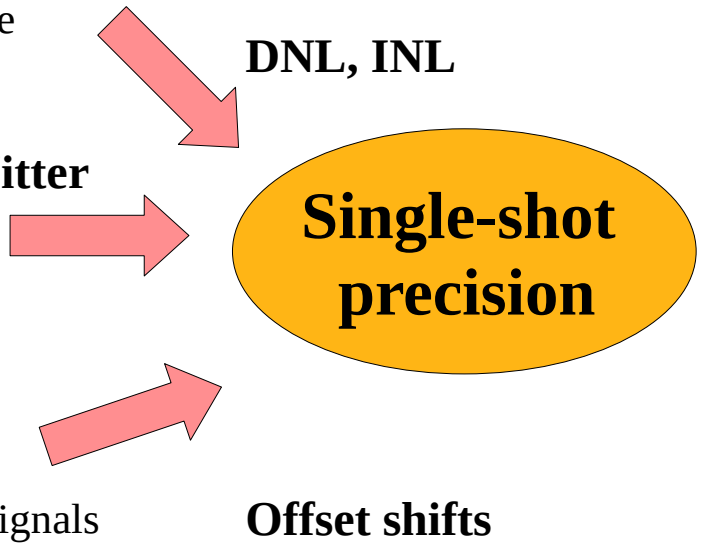


Difficulties in ps range resolution

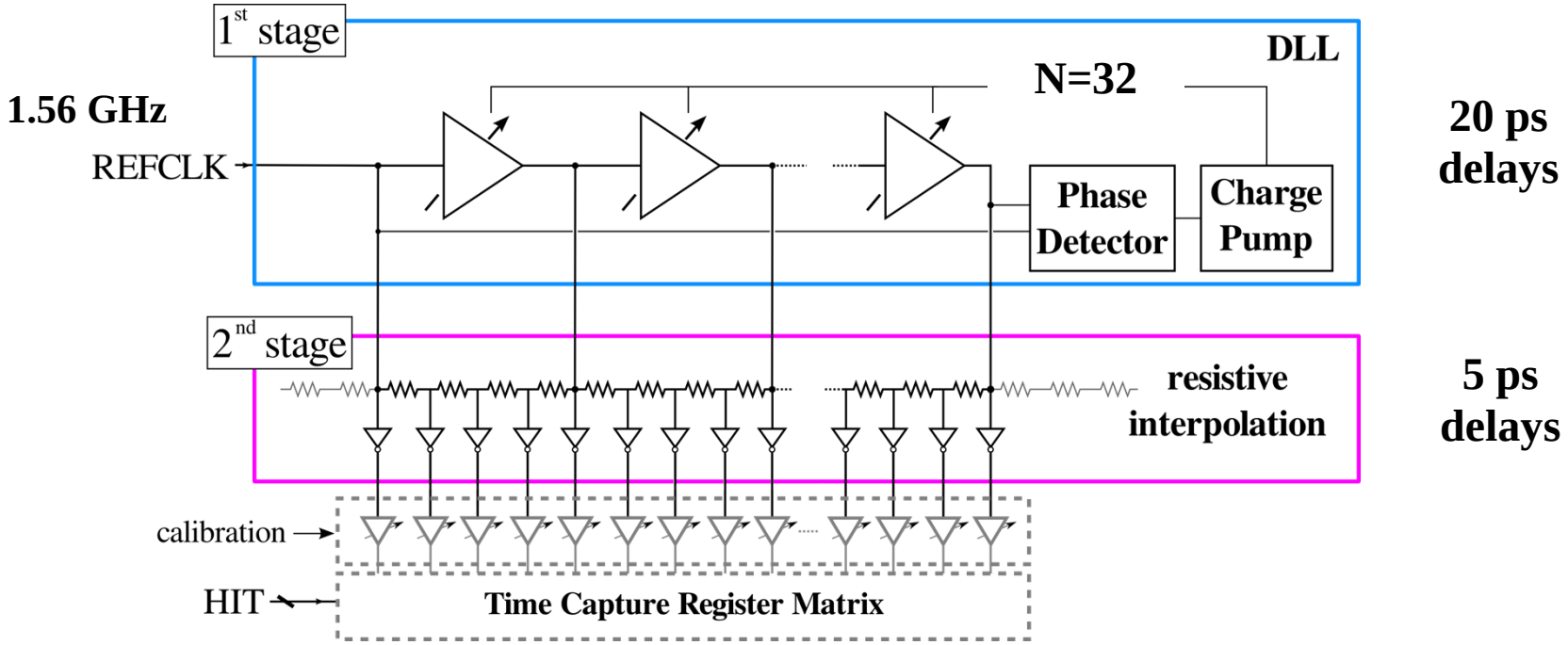
LSB/sqrt(12) ≠ rms

It is not worth making a fine binning TDC if resolution is lost in imperfections/noise

- **Device mismatch**
  - -> Careful simulation and optimization
  - -> Major impact on design and performance
- **Noise** (power supply)
  - -> **Short delays, fast edges**
  - -> Separate **power domains**
  - -> **Substrate isolation**
  - -> Crosstalk
- **Signal distribution** critical
  - -> RC delay of wires
  - -> Balanced distribution of timing critical signals
- **Process-Voltage-Temperature variations**
  - -> Auto calibration to compensate for slow VT variations: Delay locked loop
  - -> Global offset calibration still required

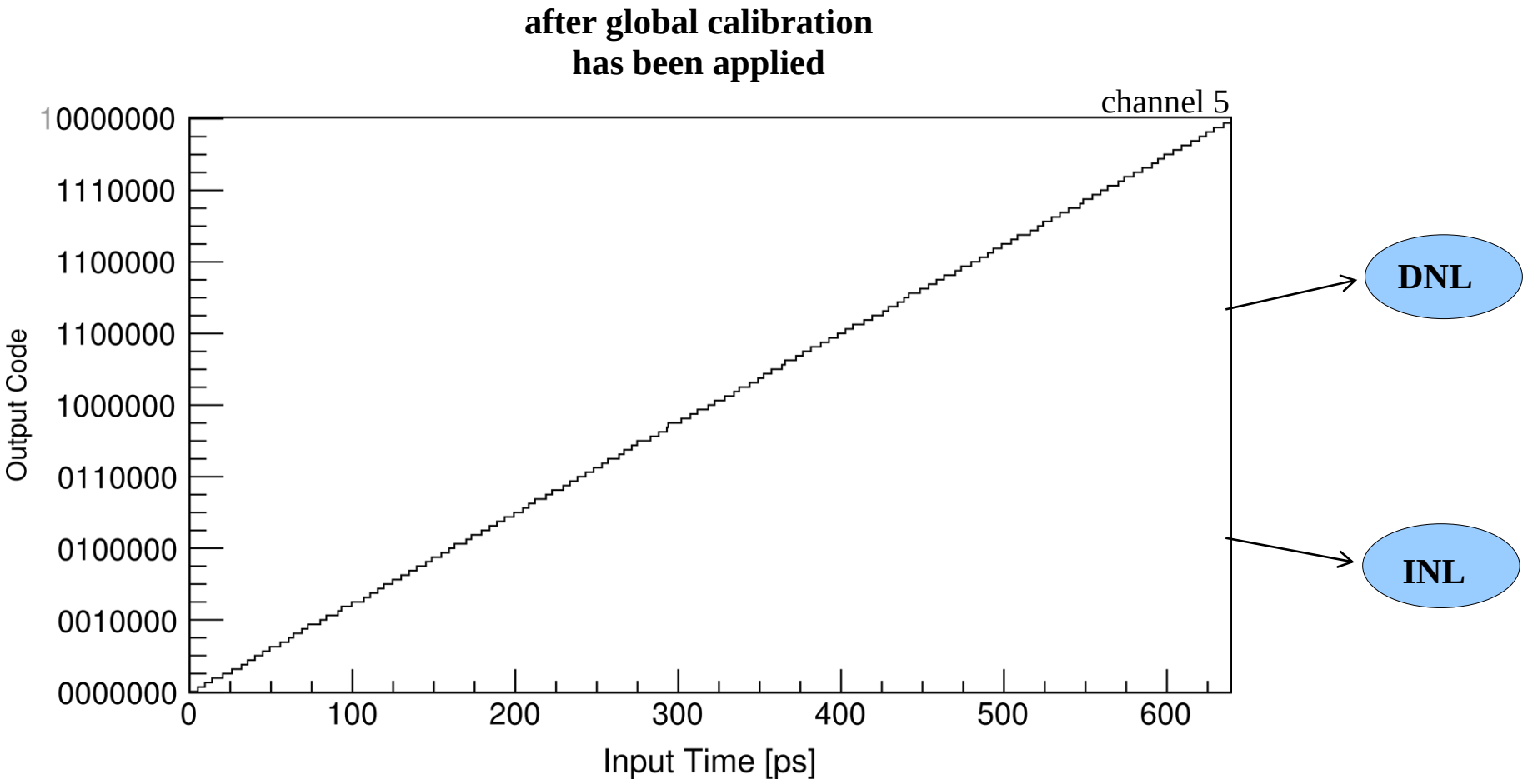


Fine-Time Interpolator

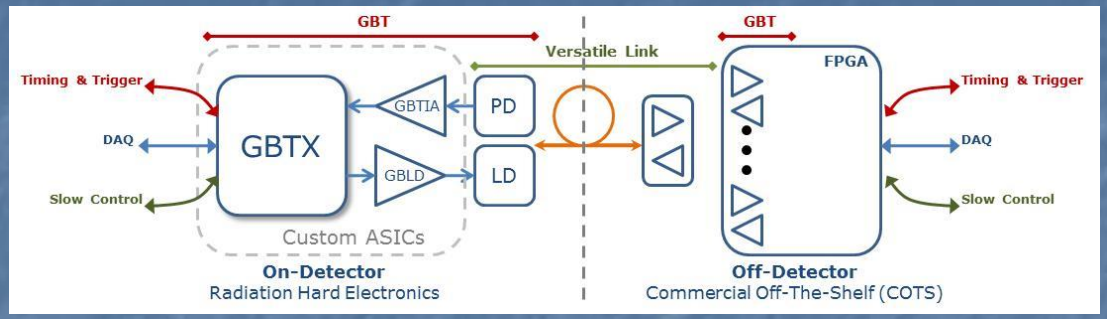


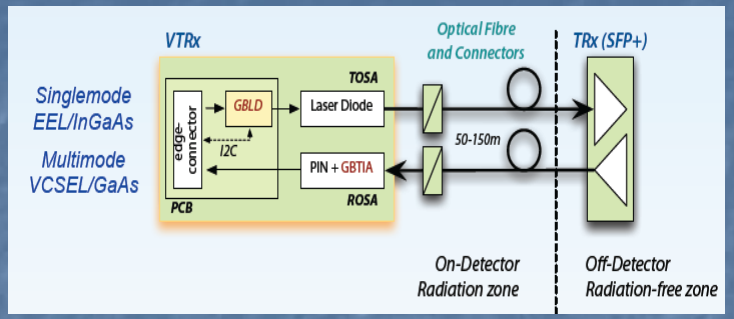
- **DLL to control LSB size**
  - -> 32 fast delay elements in first stage - 20 ps
  - -> Total delay of DLL 640 ps at 1.56 GHz
- **Resistive Interpolation to achieve sub - gate delay resolutions**
  - -> LSB size of 2nd stage controlled by DLL
  - (Auto adjusts to DLL delay elements)

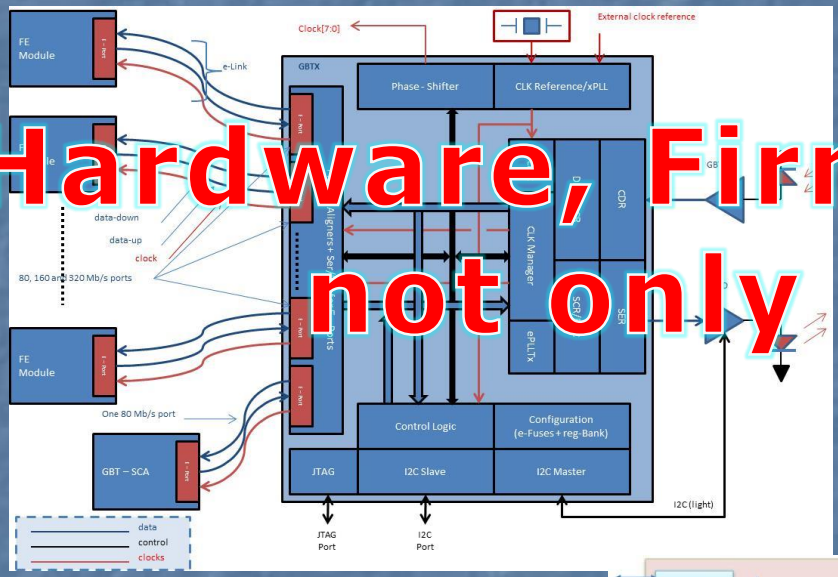
Reconstructed Transfer Function

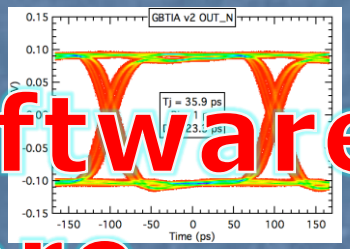


GBT, Versatile, GLIB

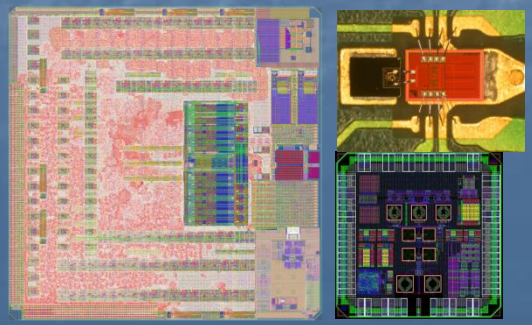


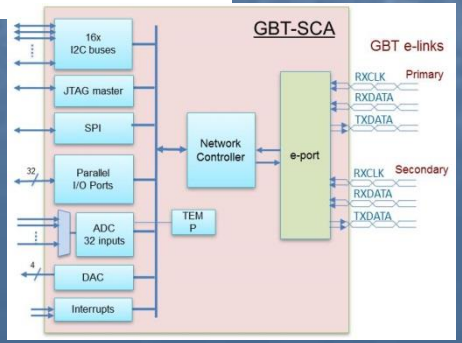


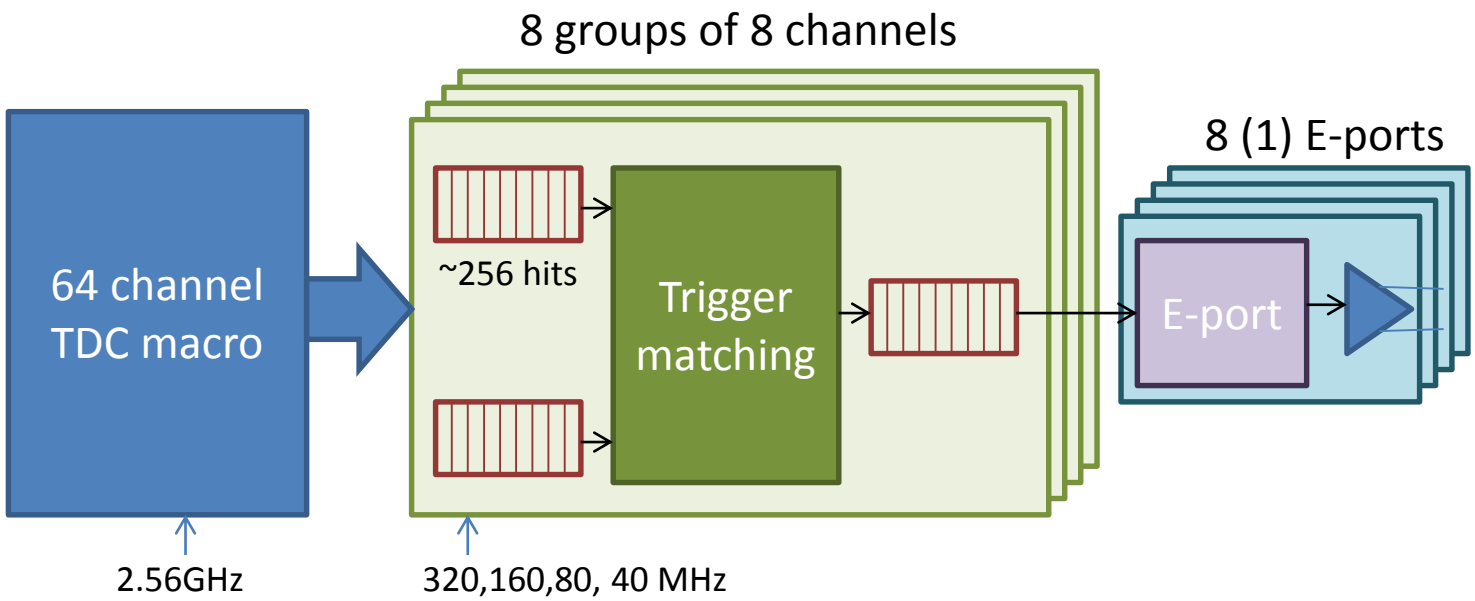




Hardware, Firmware, Software, not only Dream-ware






8 groups of 8 channels
64 channel
TDC macro
~256 hits
Trigger
matching
8 (1) E-ports
E-port
2.56GHz
320,160,80, 40 MHz