

# BE/OP VIEW

## LS1 TE/MPE REVIEW



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on behalf of the OP team



“The team is responsible for the general organization and execution of the powering tests, **interface to coordination and other teams**, as well as with other teams preparing beam operation”



Organization  
and  
coordination



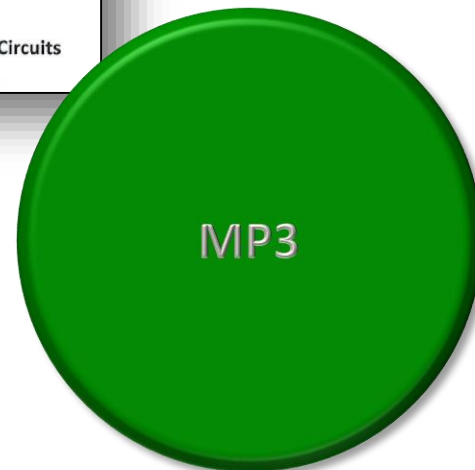
MP3 is responsible to:

- “define the procedure and the criteria for test analysis”
- “identify, track and document exceptions”
- “give recommendation for future operation”



Automation

“The team will ensure that tools are available for the follow-up of all phases [...] assume responsibility for providing the sequences and provide tools for automatic testing of circuits and analysis of test steps”



MP3



## Coordination and communication

- Main communication channels
  - 8:30 meeting, mails, telephone calls
  - Suggested at MP3 review - fault tracking with JIRA to be implemented: should be used as main communication channel (can be assigned to the concerned specialist)...**lengthy and heavy procedure, to be discussed and investigated!**
  - Communication with QPS team improved with continuous information exchange...
- What went wrong:
  - ...still not easy and to be more properly organized (no excel file,...)
  - **Information several times not transferred to the field teams**
  - Wrong synchronization of the activities (i.e. access in a time slot foreseen for test)
  - No clear limit between planning and PT coordination
  - Misunderstanding overlap between MP3 and PT coordination
  - Is EIQA part of the powering tests? To be clarified...
  - LS1 should finish before the beginning of the powering tests
- Condemnation
  - The procedure is clear, but it should be followed by **everybody**, to avoid condemnation/de-condemnation iterations!!!
  - A better (mid/long-term) planning would help improve efficiency
- NCs: a bit of confusion on who has responsibility to follow them...



## Test planning

- Test planning was considered too optimistic/optimized, without contingency
- Some problems were coming from the very late approval of activities (i.e. CSCM, 3 sectors vs whole machine) - ideally, should have an early approval
- Planning/coordination inside groups to be optimized
  - Realistic time estimate
  - Information flow to be improved
- Test preparation should be completed earlier
  - Earlier definition of what to test and how
  - Procedures should be APPROVED before test start
    - Implementation in the sequencer
  - Too many signature changes were applied during PT
  - No major changes should be applied DURING PT

## Manpower

- QPS: Limited number of experts available (in general, lacking in-house resources)
- Presence of experts in CCC is a priority
  - MP3 and EPC were properly represented
- PIC has no support -> require a constant availability of the 2 experts



## Software

- Very high responsiveness of the SW support team (critical)
- LS1 for software providers should finish earlier
- LSA dev should be a mirror of LSA pro (for pro-GUI debugging issues)
- **QPS PM timing mismatch was an important issue**
- Automation was a key ingredient for success
  - Low current circuits analysis is fully automatized (automation of 600 A next)
  - PIC had 5000 interlock tests to be done and analysed and it was almost transparent
    - automatic analysis was not working perfectly due to continuous changes
  - In general too many changes on QPS side, not clear which buffers, etc.
- Not clear definition of EE signature was a problem



## Tests

- EIQA
  - Many years of experience and well defined procedures
  - Very detailed in NC follow-up
  - Great response at each time they needed to intervene
- PIC
  - No issues, even if 9/36 PIC units were moved due to R2E
  - interface tests and in general IST done before the powering
    - errors detected and corrected before PT (only one at P3 was discovered later, due to a database mismatch for ROD/F)
- QPS
  - IST is using an important part of the initial powering tests
    - Should investigate a way to optimize the process (performing a part of the IST when the sector is being prepared)
  - **Need of a test bench to debug SW and HW changes**
- EE
  - Automated analysis of the test would be an important improvement
  - The system was tested and debugged during SCT





## Tools

- Accelerator Test Tracking should be modified
  - Add filtering on GUI to better select circuits/sectors
  - Reporting tool to be implemented
  - Better integration with Post-Mortem Event Analyser to be developed
  - Interlock Tests (water-cooled cable, current lead thermo-switch) to be integrated
  - Follow-Up of issues to be improved (ref. to JIRA)

## Mid-term actions

- Procedures
  - Need to formalize and document all parameters
  - Piquet documentation
- Sanity check being to be put in place
  - Scanning the critical signals to check whether they are live, sanity check in the ramp
  - Macro to reset the nQPS
  - Pre-operational check to be implemented

## On a longer term...

- Reference test bench to be implemented
- Design of a real test bench (with magnets) to test new SW and debug procedures (SM18?)