Current and future ASICs for Precision Timing Measurement
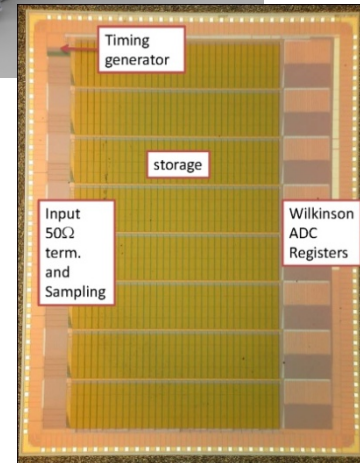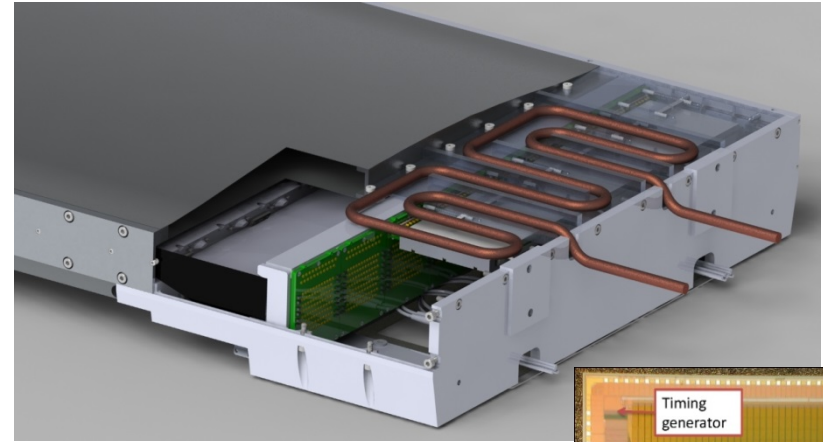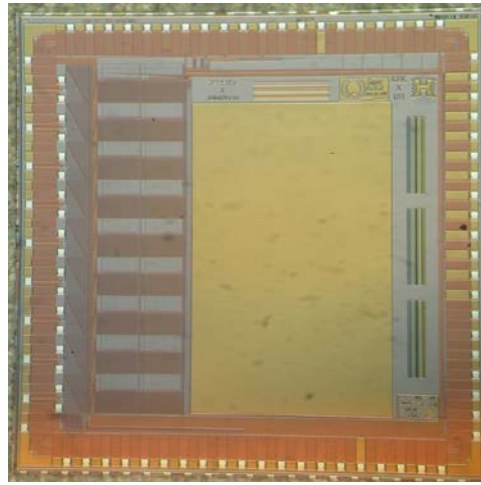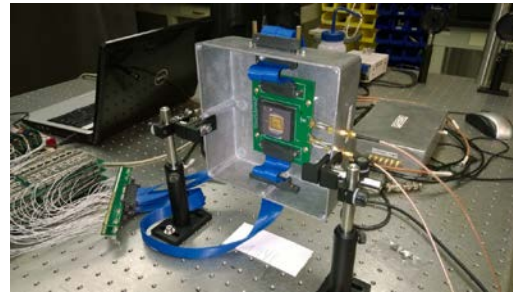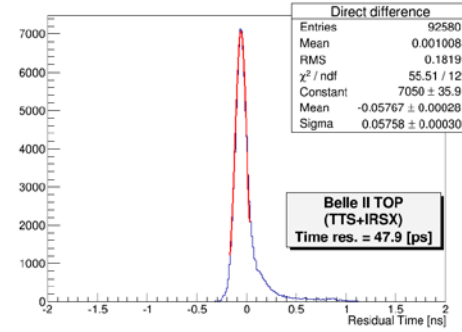
Pardis Niknezhadi, Peter Orel, Gary S. Varner
University of Hawai'i
Prague ps Timing Workshop
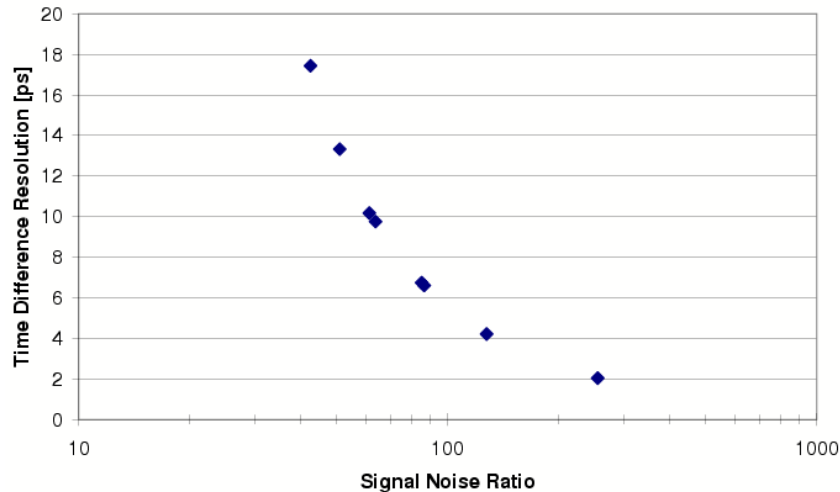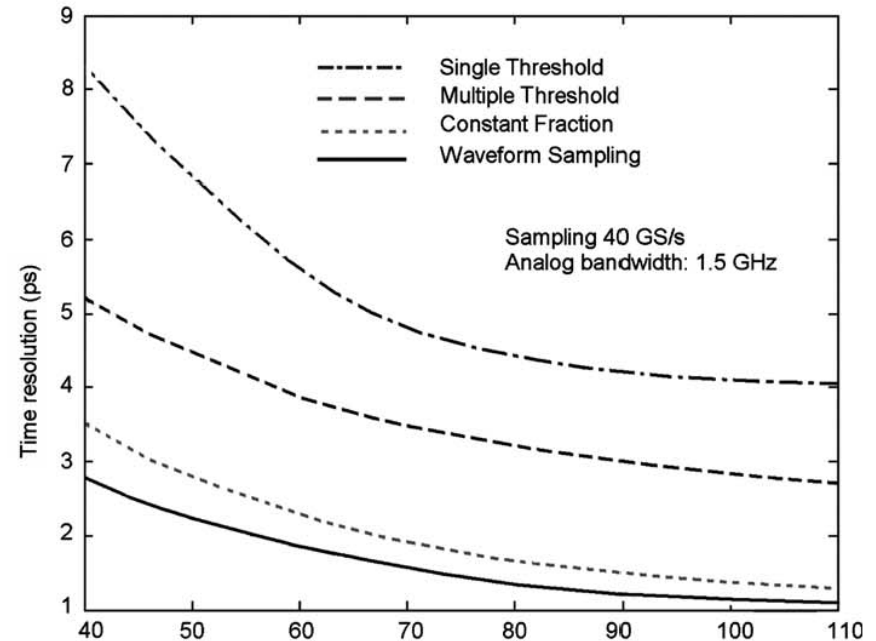June 9, 2015

The Future is …

1GHz analog bandwidth, 5GSa/s

Time Difference Dependence on Signal-Noise Ratio (SNR)
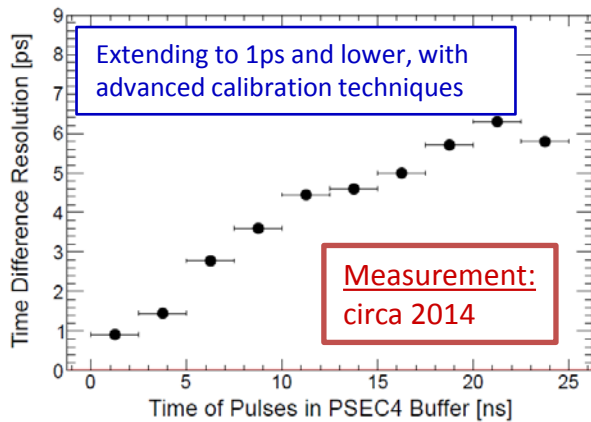

G. Varner and L. Ruckman
NIM A**602 (2009) 438**-445.

Simulation includes detector response

J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

2

Now: high space-time Resolution

In a number of communities (future particle/astroparticle detectors, PET medical imaging, etc.) a growing interest in detectors capable of operating at the pico-second resolution and μm spatial resolution limit (for light 1 ps = 300 μm)

Prediction: circa 2009

Extending to 1ps and lower, with advanced calibration techniques

Measurement: circa 2014

signal electrodes with contact pads to readout

200 – 300 μm

active edges

beam in
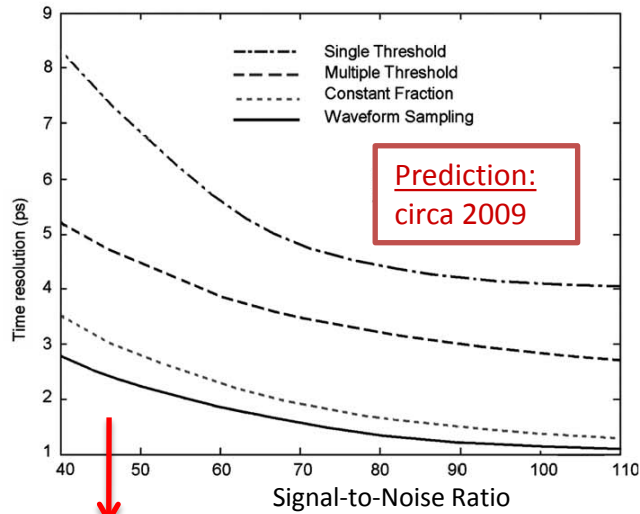
Front-End Electronics
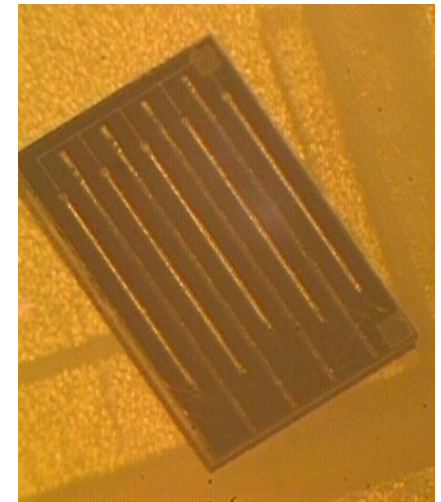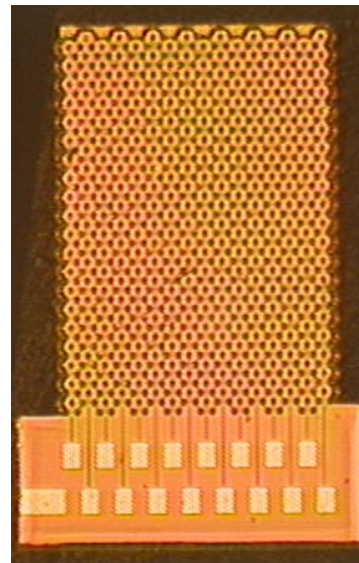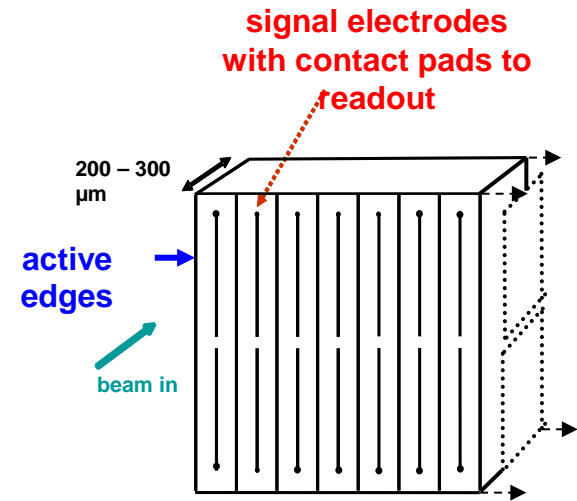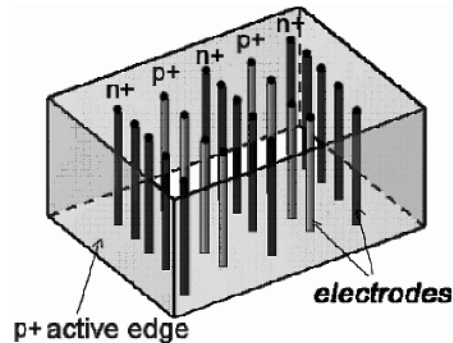
Fast signal collection x-ray detectors

Toward increased timing precision

ASIC	# chan	Depth/chan	Time Resolution [ps]	Vendor	Size [nm]	Year
LABRADOR 3	8	260	16	TSMC	250	2005
BLAB	1	65536	1-4	TSMC	250	2009
STURM2	8	4x8	<10 (3GHz ABW)	TSMC	250	2010
DRS4	8	1024	~1 (short baseline)	IBM	250	2014
PSEC4	6	256	~1 (short baseline)	IBM	130	2014
RITC3	3	Continuous	TBD	IBM	130	---
PSEC5	4	32768	TBD	TSMC	130	---
DRS5	8/16?	128x32	TBD	UMC	110	---
SamPic	16	64	~3 [pic 0]	AMS	180	[2014]
RFpix	128?	TBD	<= 100fs (target)	TSMC	45 ?	---

Waveform sampling ASICs (not just good looking)
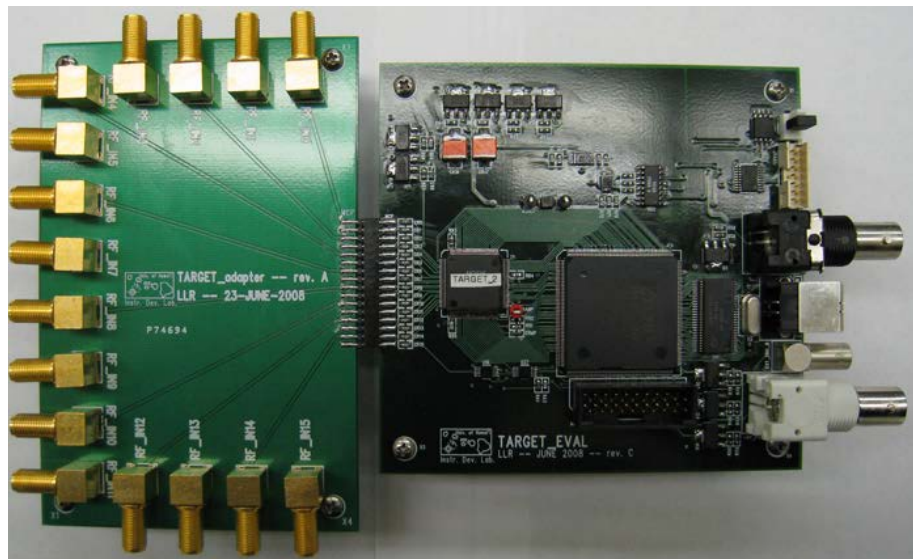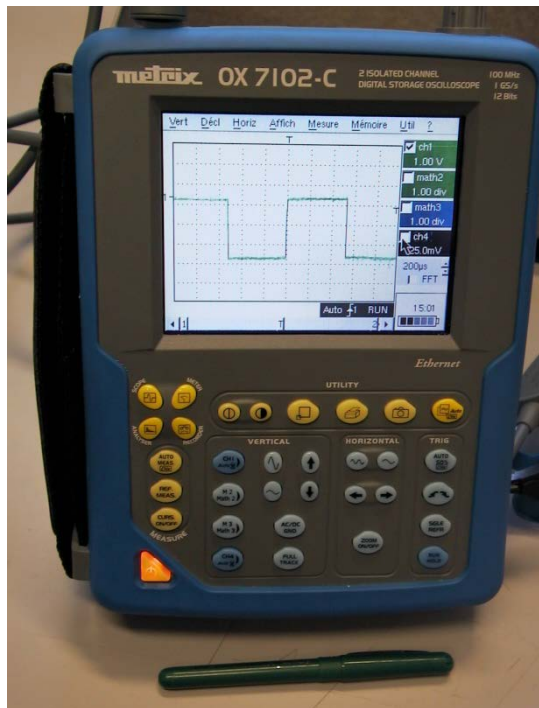
|	WFS ASIC	Commercial
Sampling speed	0.1-15 GSa/s	3 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

Another gaze into the Crystal Ball

Exploration of the space-time limit

-Sampling at high sampling rate and high bandwidth
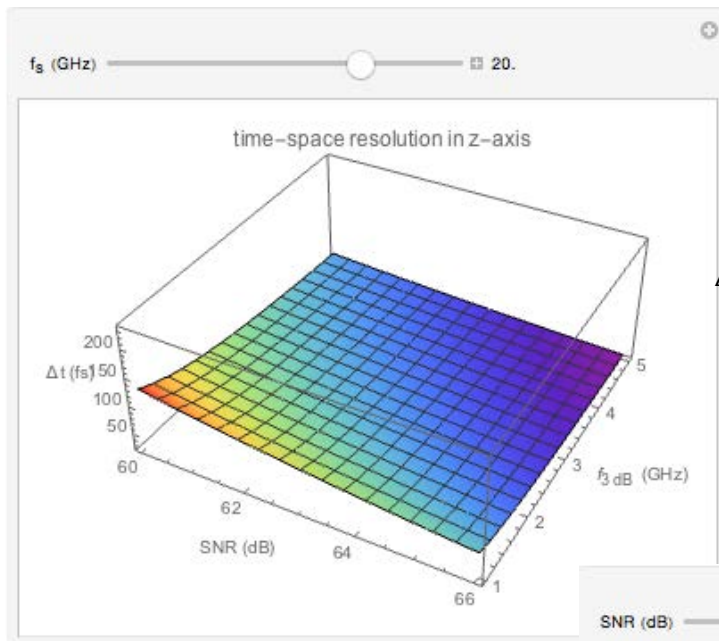
-Resolve small distances

Current Goals: Spatial resolution of 10μm in z and 20μm in rφ

In Silicon 10μm in z corresponds to timing resolution of about 100fs

20μm in rφ will depend on the SNR
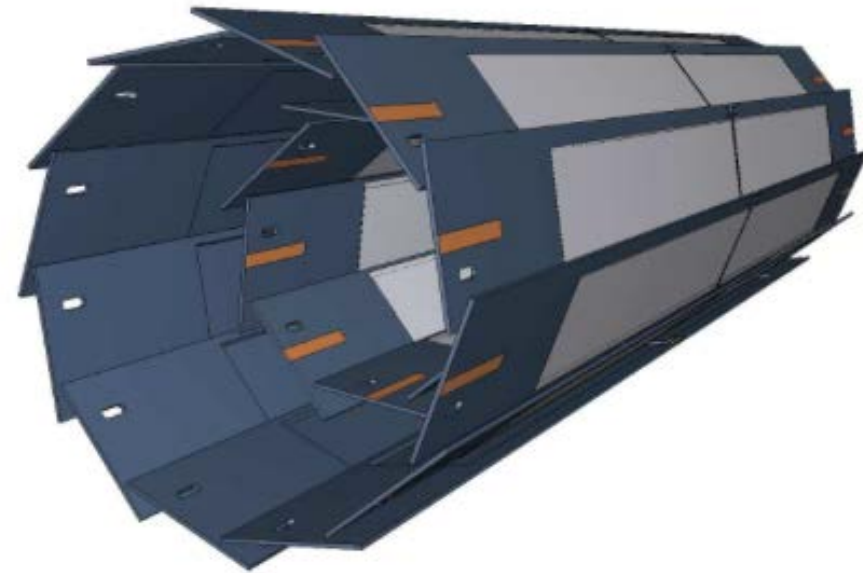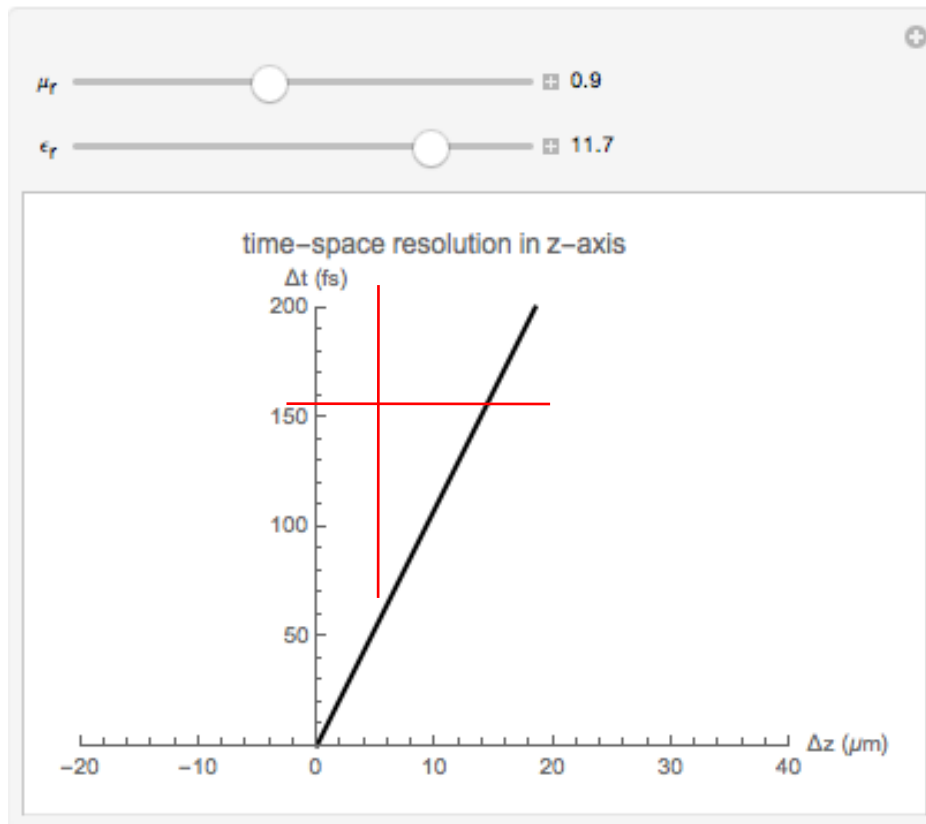
Pixel detector (PDX) at SuperKEKB

Visualizing parameters for time resolution in z

$$\Delta t = \frac{\Delta U}{U} \frac{1}{\sqrt{0.34 * BW * f_s}}$$
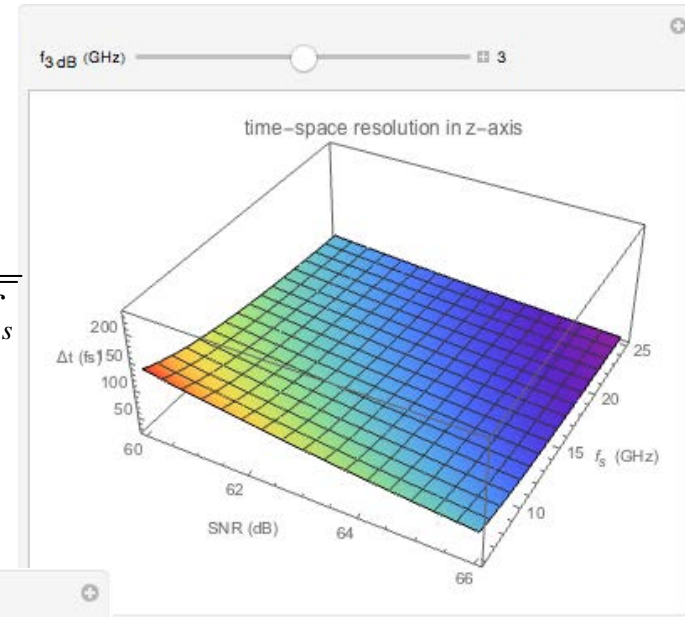
^ Need to hold sampling frequency to least at 20 GHz to have timing resolution in 100fs range
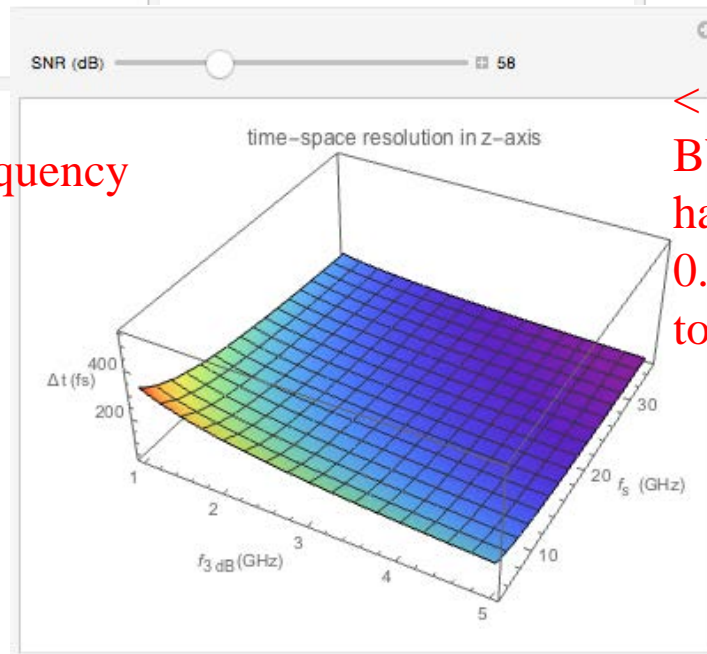
< For the above sampling freq and BW integrated noise amplitude has to be in the range or less than 0.5mV to 0.6mV corresponding to SNR~58dB (V_{pp}=1volts)

SNR~58dB corresponds to 9.4 bits for 20µm resolution in rφ (Ideal ADC)

8

WFS ASIC: Basic Functional components

Single storage Channel

Sample timing Control

Few mm x Few mm in size

On or off-chip ADC

Readout Control
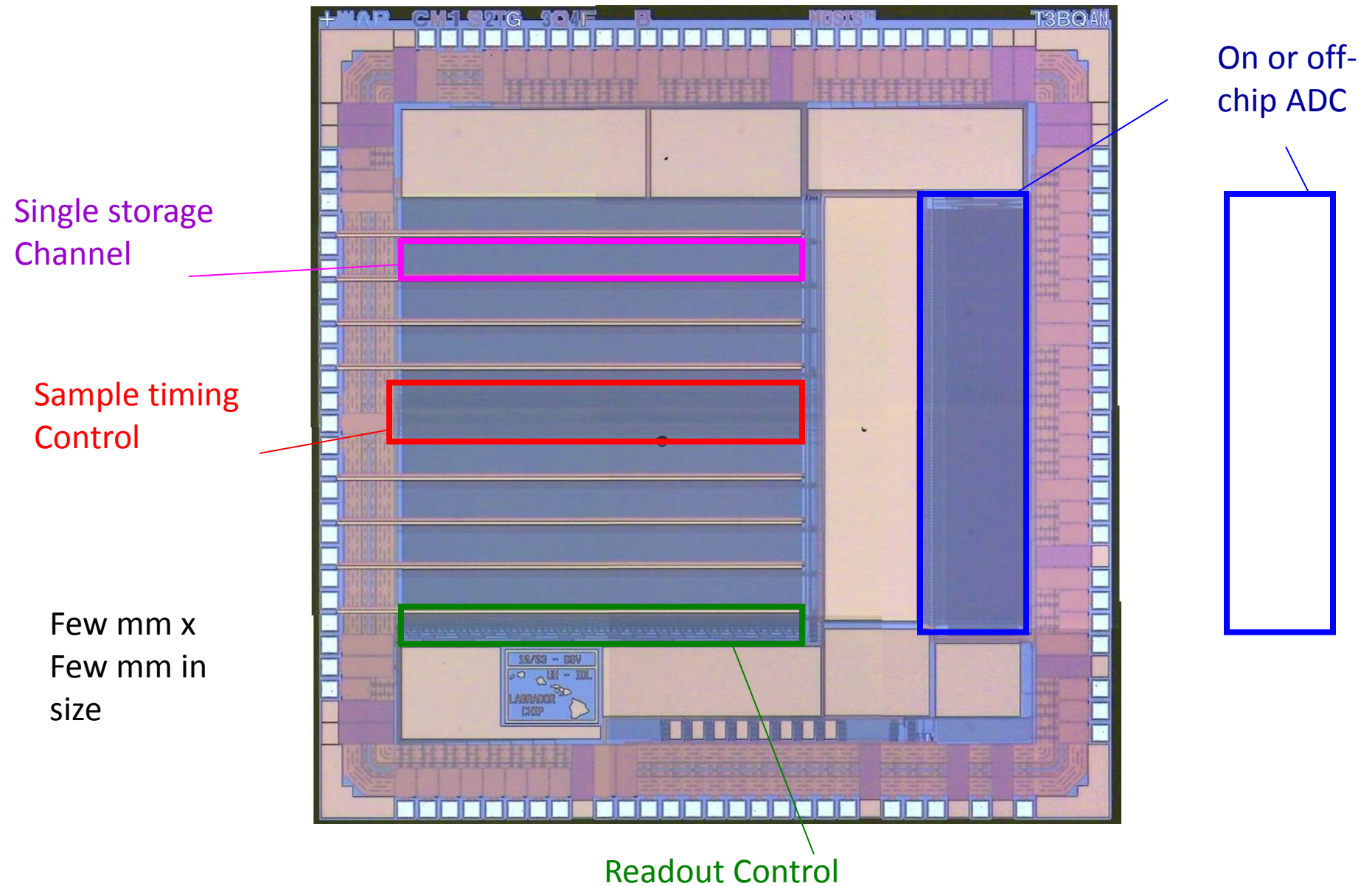
Intrinsic Limitation

No power (performance savings) for continuous digitization

We aren't going to put Analog Devices out of business
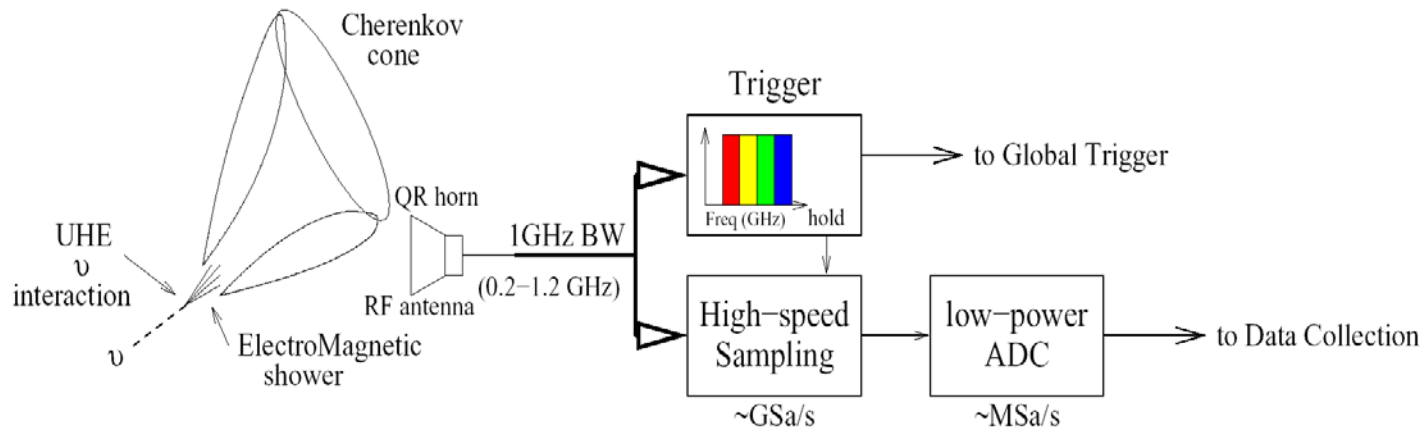
"down conversion"

→ For most "triggered" 'event' applications, *not a serious drawback*

Constraint 1: Analog Bandwidth

Difficult to couple in Large BW (C is deadly)

inside ASIC

RFamp

Z_S

$50\,\Omega$ C_{in}

$f_{3dB} = 1/2\pi ZC$

V_{sig} — Z_S — V_{in}

Z_T
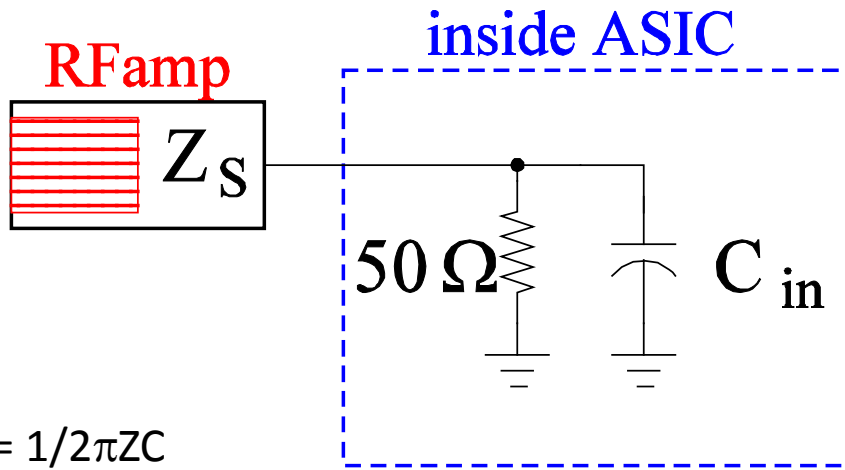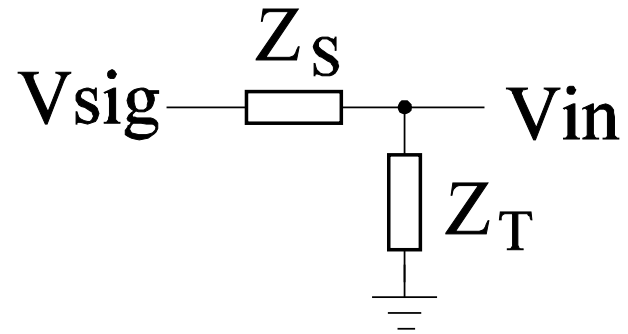
Input coupling versus frequency

Cin=300fF, Rs=50Ohm

Relative amplitude [dB]

Frequency [GHz]
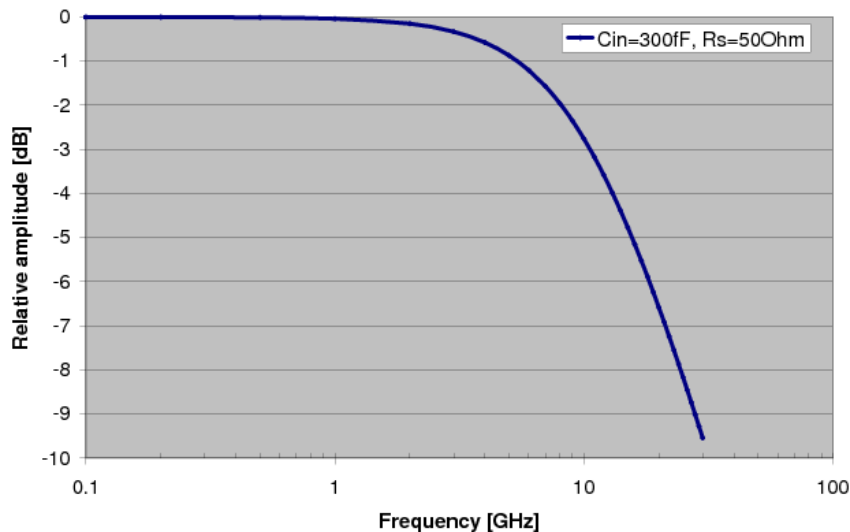
Input Coupling versus total input Capacitance

R_S = 50Ohm

Analog Bandwidth [-3dB frequency]

Total input Capacitance [fF]
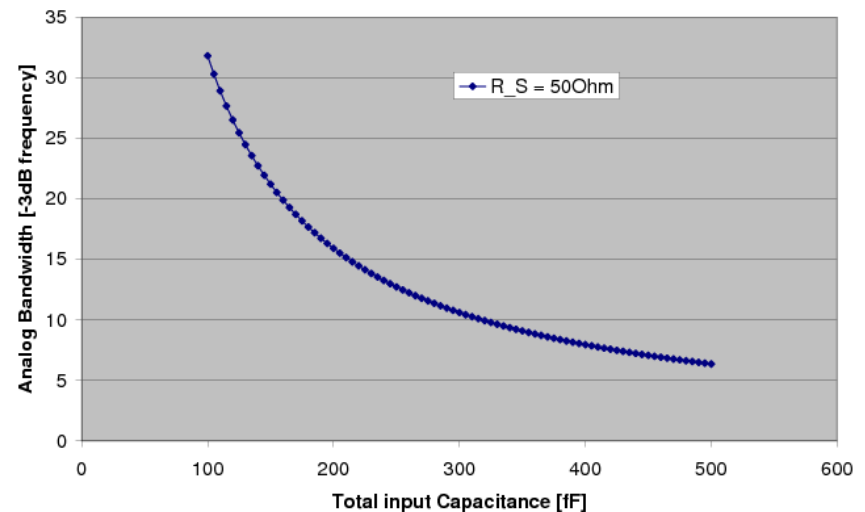
Constraint 2: kTC Noise

Want small storage C, but…
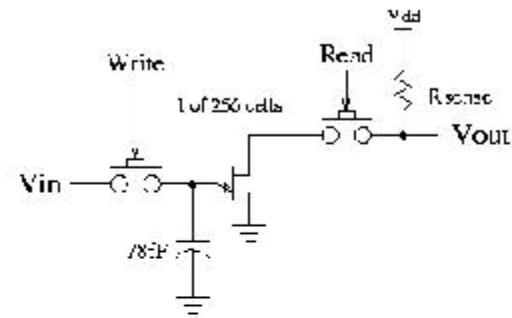
$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

$$C_{store} = 78fF$$

1mV on 16fF is only 100e- !

Impact of Storage Cap size

For 1V useable input range

9bits

10bits

Ref point

11bits

12bits

Vrms

Storage Cap [fF]

Vrms [mV]
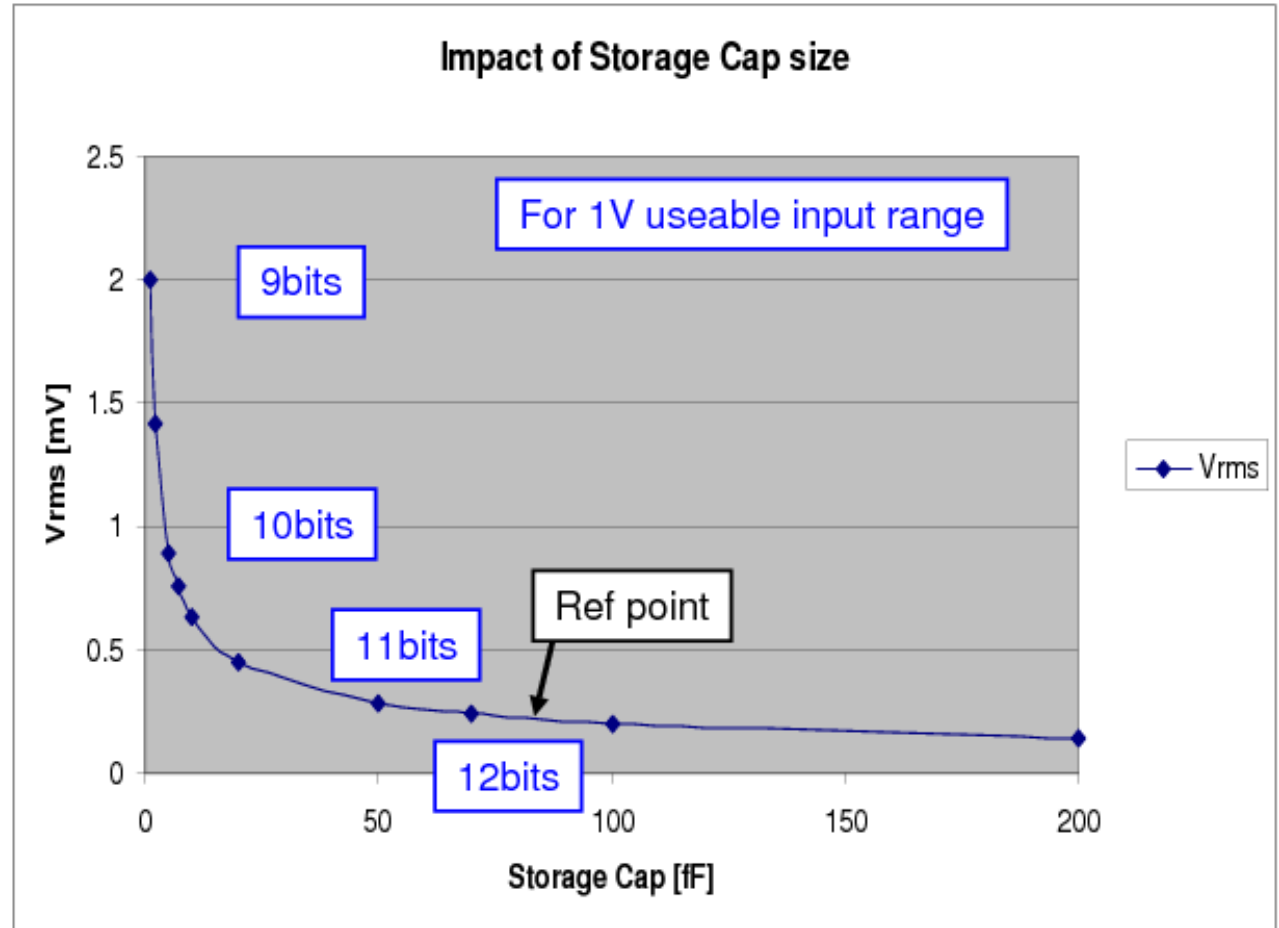
Constraint 3: Leakage Current

Increase C or reduce conversion time << 1mV
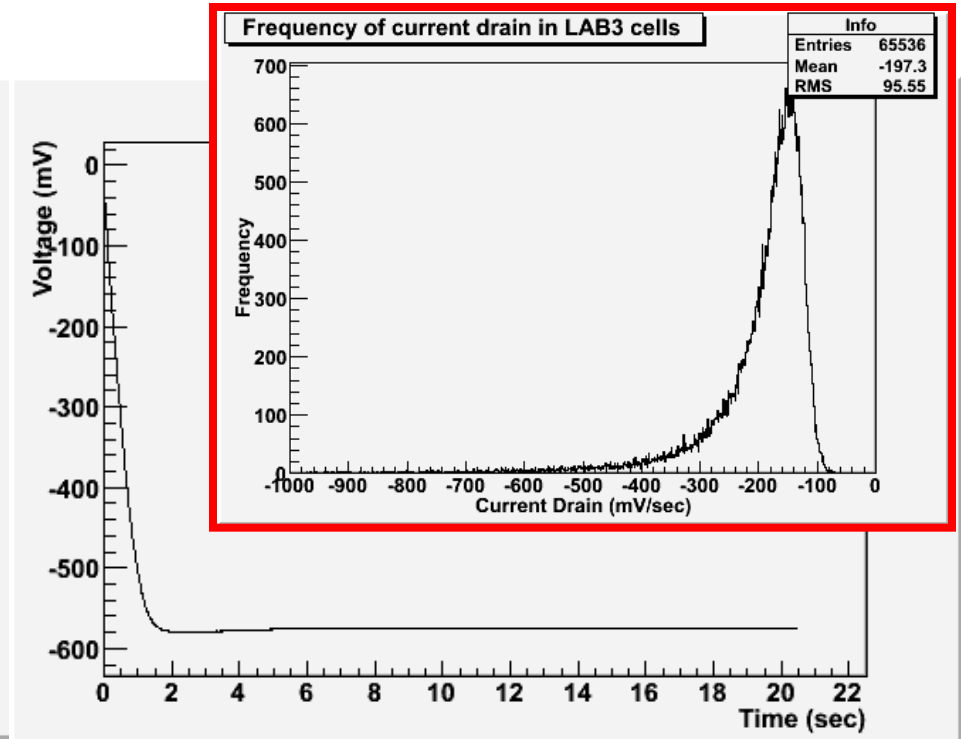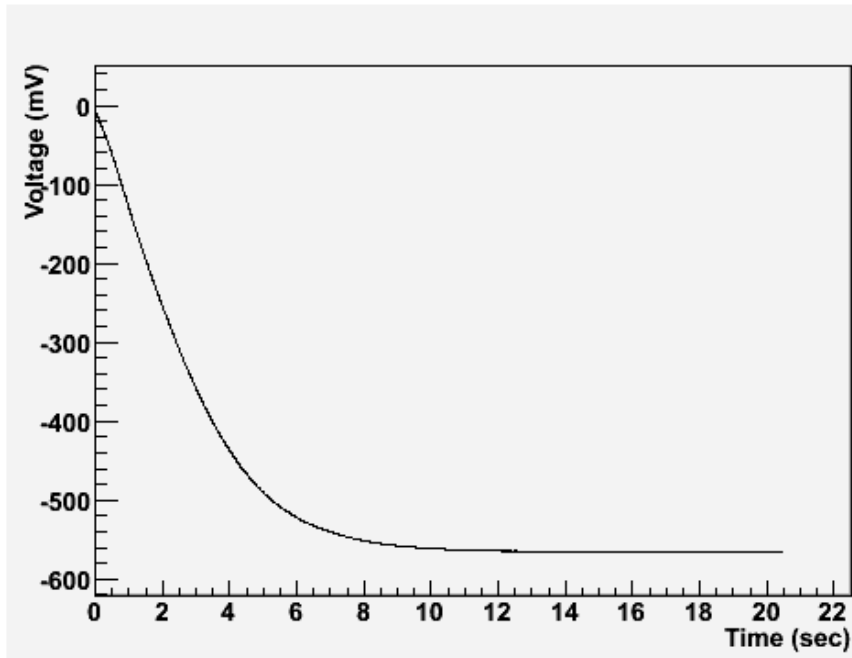
Sample channel-channel variation
~ fA → nA leakage (250nm → 130nm)

Target Specifications (design study goals)

Parameter	Minimum desired value
Sampling frequency (ASIC)	20 GHz
Bandwidth (Detector and ASIC)	3 GHz
Signal to Noise Ratio (Detector and ASIC)	58dB (V_{pp}=1 volts)
Velocity of Propagation (Transmission Line/ strip line)	0.35c
Number of Bits of Resolution	9.4 bit

This is an ongoing study – will show where we are

Take the PSEC4 design as a reference

PSEC4

~1.6 GHz

500mV$_{pp}$ (-2dBm)
50mV$_{pp}$ (-22dBm)

No calibration
With timebase cal.: σ~4.3 ps

15
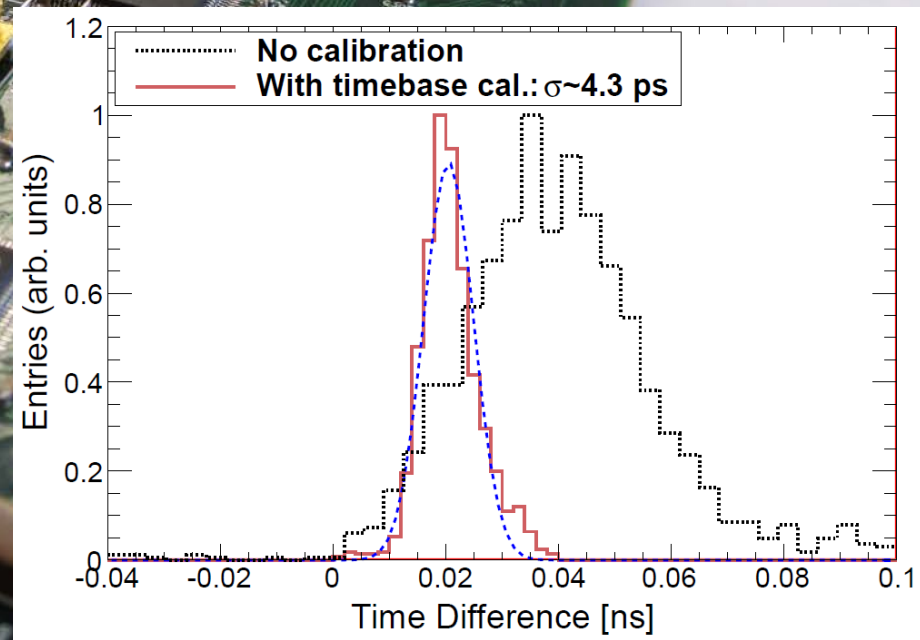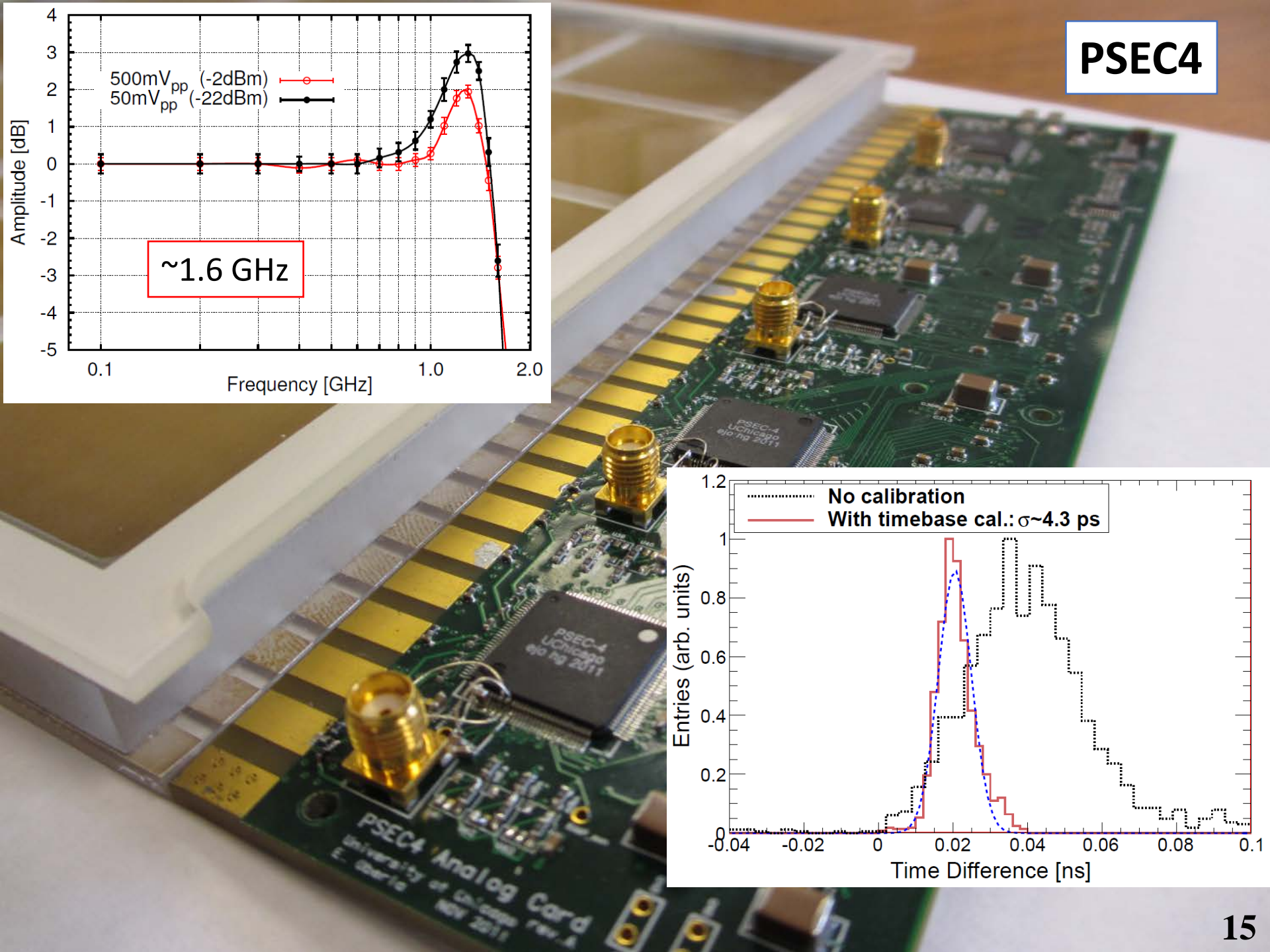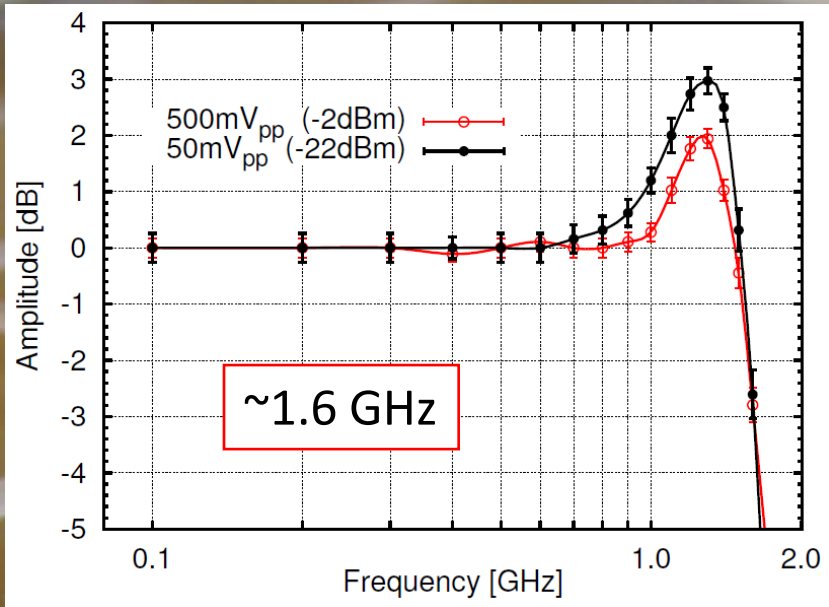
PSEC4: Sampling Analysis

Utilizing PSEC4's SCA as starting place
-Adjustable Sampling rate between 4-15 GSPS
-1.6 GHz bandwidth
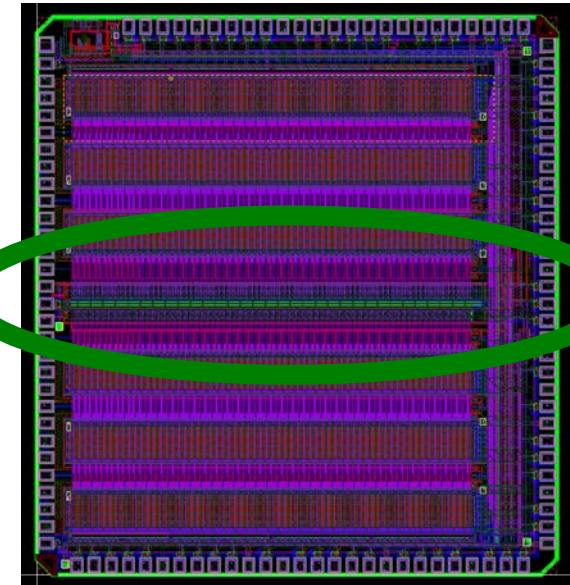
x256
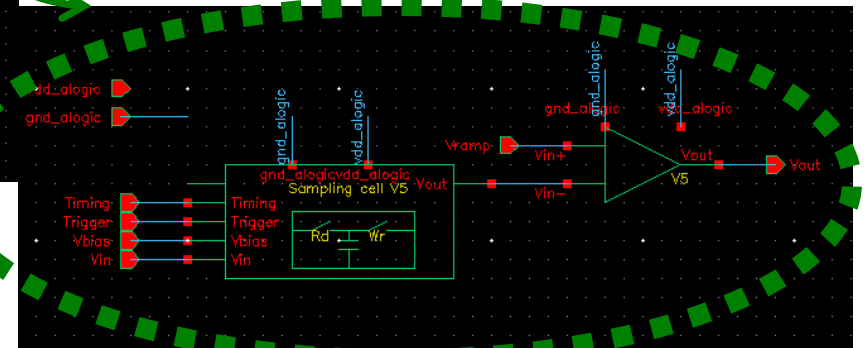
also
-0.13μm CMOS (IBM-8RF)
-10.5 bit DC dynamics

Equivalent Circuit

Multichannel
 sampling array

Gain vs Frequency

Legend:
- First Cell ON w/o Par
- First Cell ON w/ Par
- First 2 Cells ON w/ Par
- First 3 Cells ON w/ Par

17
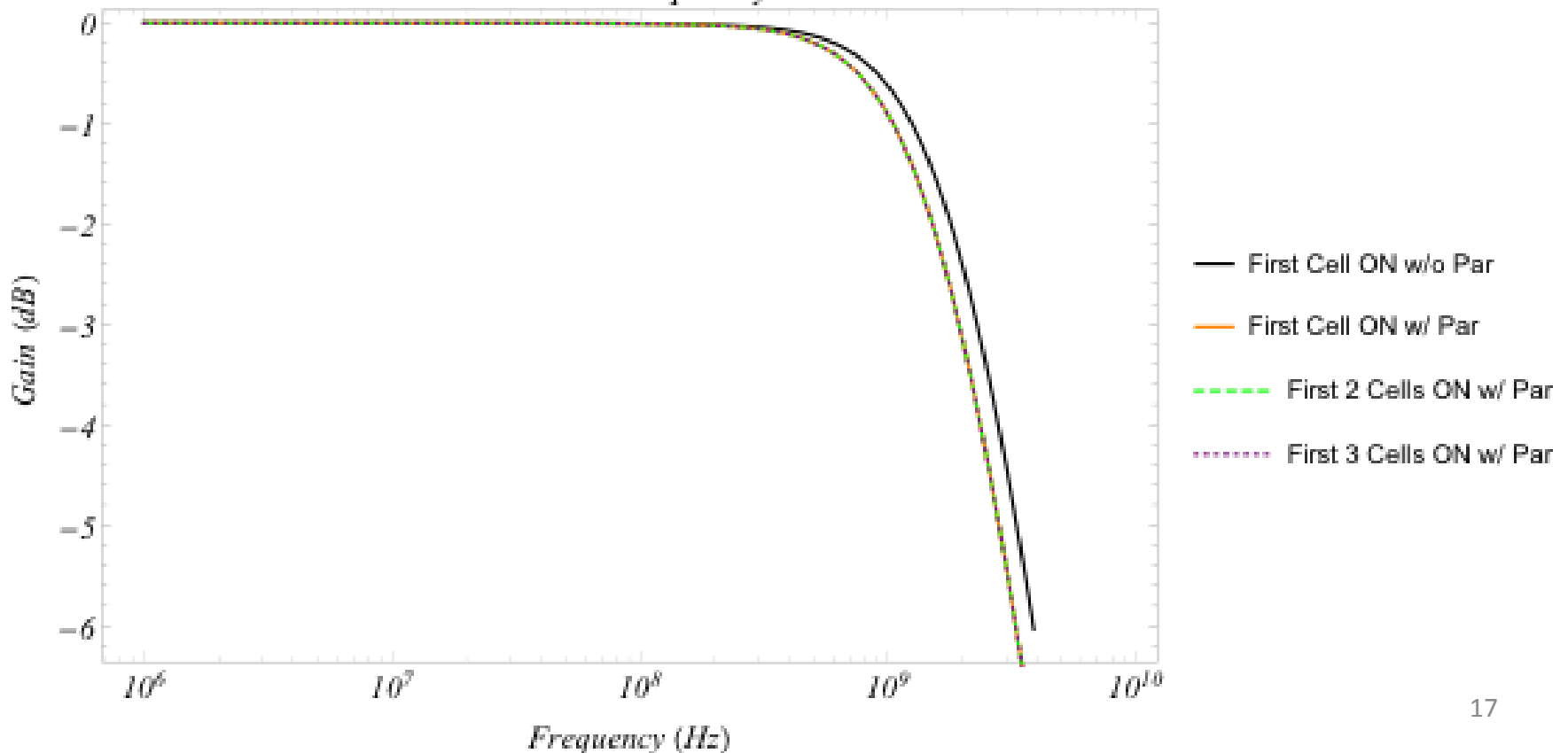
Simulation Results: Bandwidth for worst case operating bias point

Whether the 1st switch is on or the last, Gain is the same

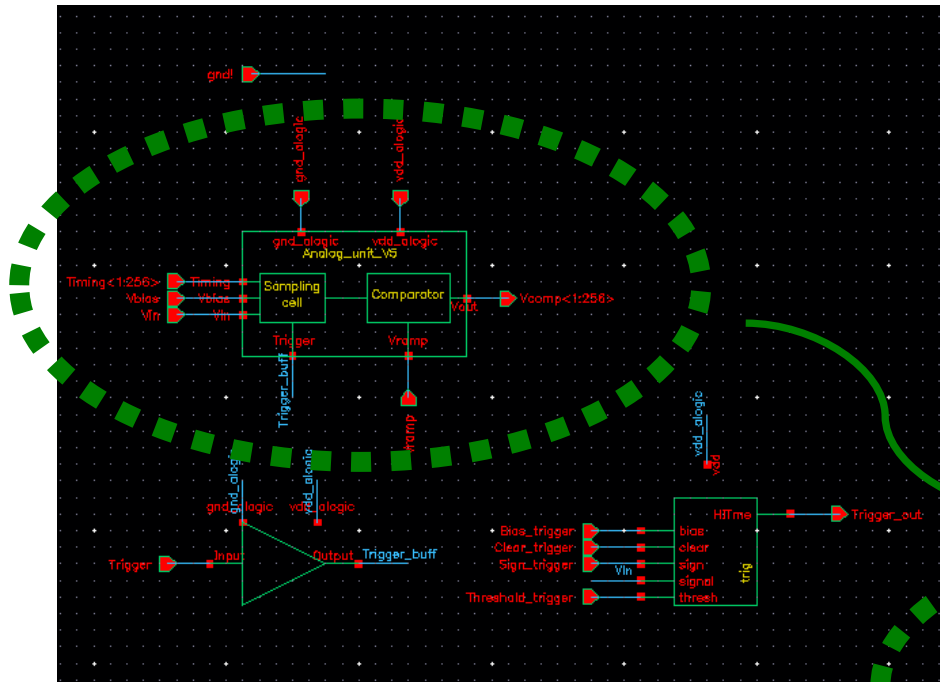Gain vs Frequency

f_{3dB}

w/ Par w/ 50 Ω	1.0 GHz
w/o Par w/ 50 Ω	1.4 GHz
w/ Par w/o 50 Ω	1.9 GHz
w/o Par w/o 50 Ω	2.2 GHz

Legend:
- ----- 1st Cell On w/o Parasitic C
- ----- 1st Cell ON w/ Parasitic C
- .... last Cell ON w/ Parasitic C
- —— w/ 50 ohm 1st Cell On w/o Parasitic C
- —— w/ 50 ohm 1st Cell ON w/ Parasitic C
- ----- w/ 50 ohm last Cell ON w/ Parasitic C
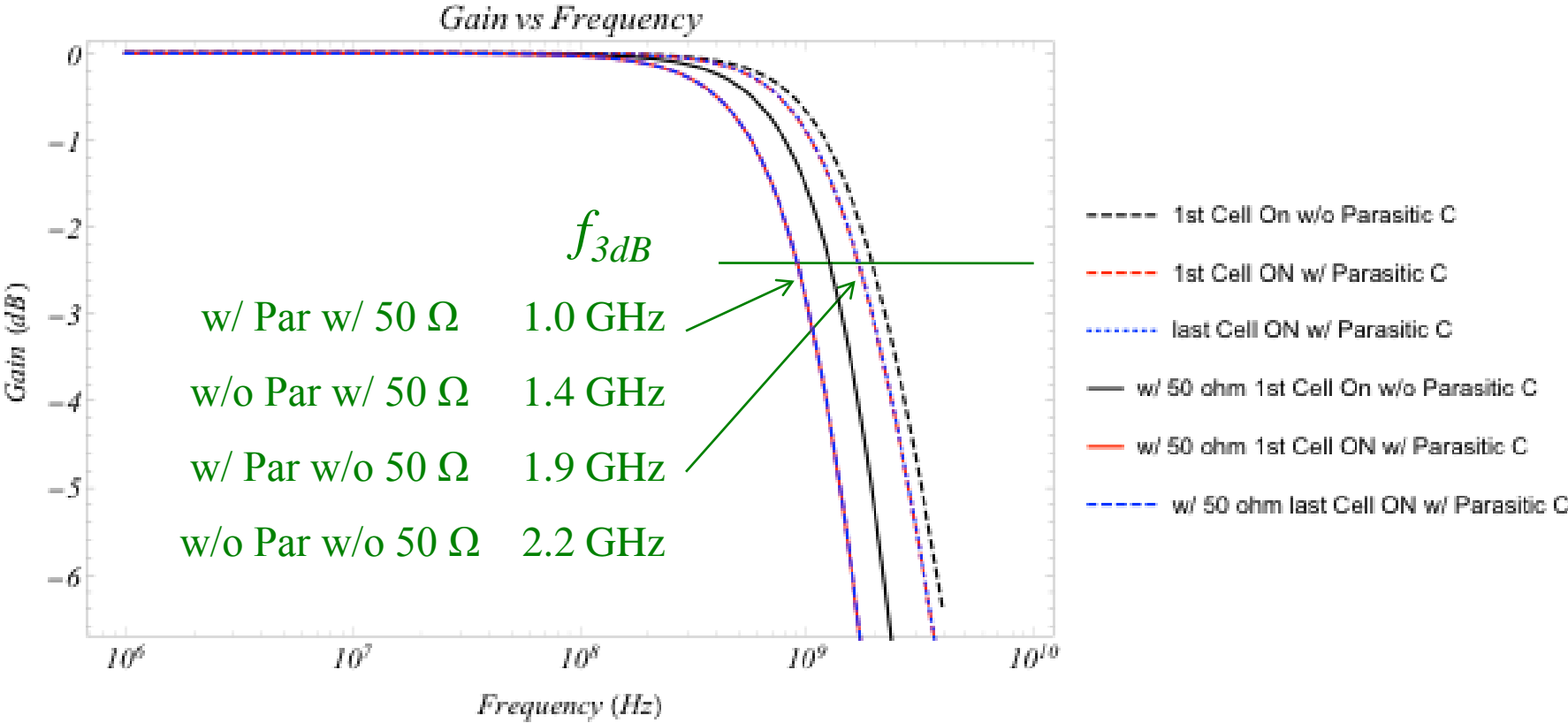
Simulation Results: Group Delay

Group Delay does vary depending which switch is on by ~25ps
 which puts a constraint on sampling time window

Group Delay vs Frequency

- · · · · · last Cell ON w/ Parasitic C
- —— 1st Cell On w/o Parasitic C
- —— 1st Cell ON w/ Parasitic C
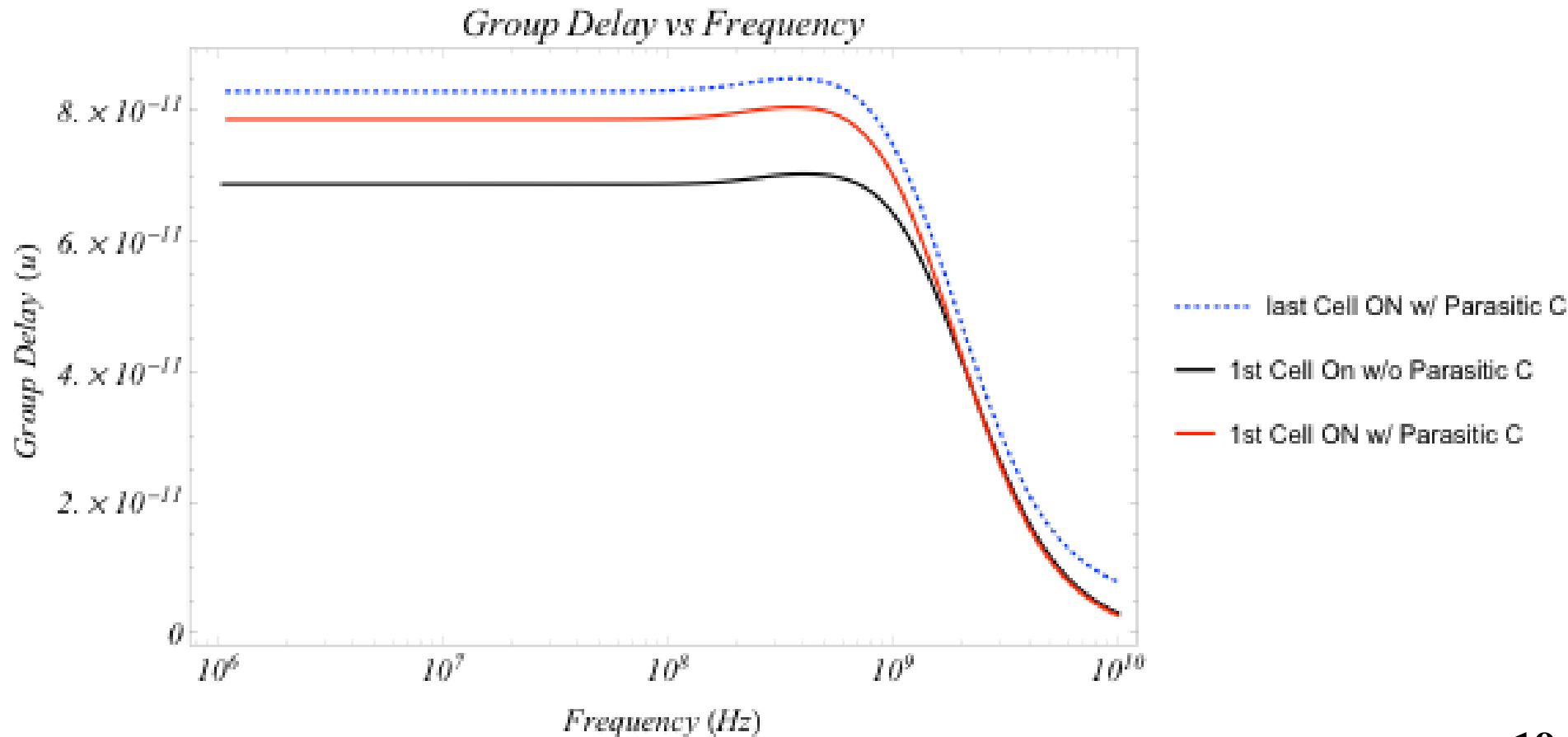
Simulation Results: Phase

- At higher frequencies Phase vs freq behavior is also different and depends on which switch is on

Phase vs Frequesncy
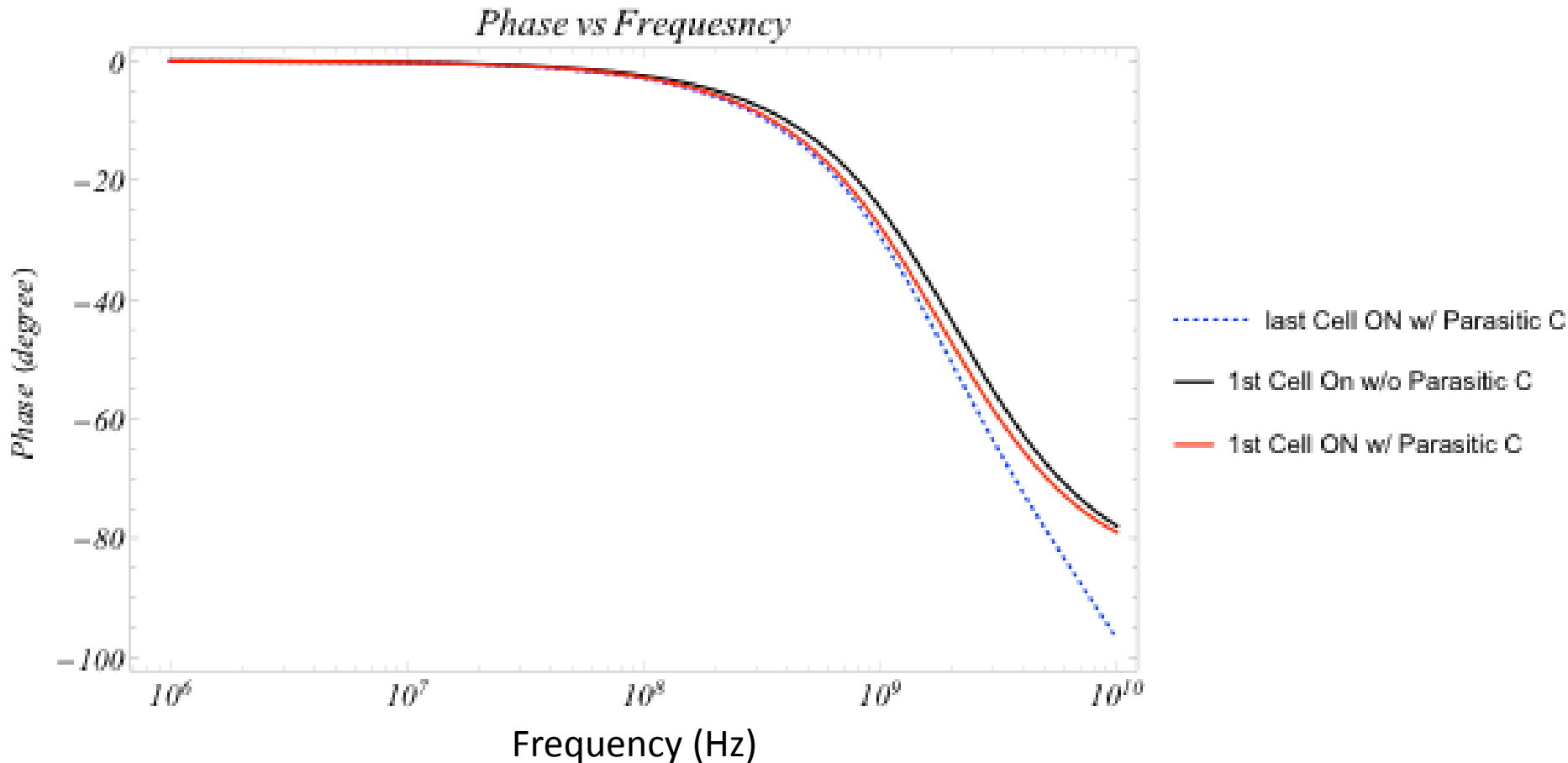
Simulation Results: Capacitance

Capacitance is 2.2 pF and does not dependent on which switch is on

Capacitance vs Frequency

PSEC4 Analysis: Single Sampling Cell

Input pad

Transmission line
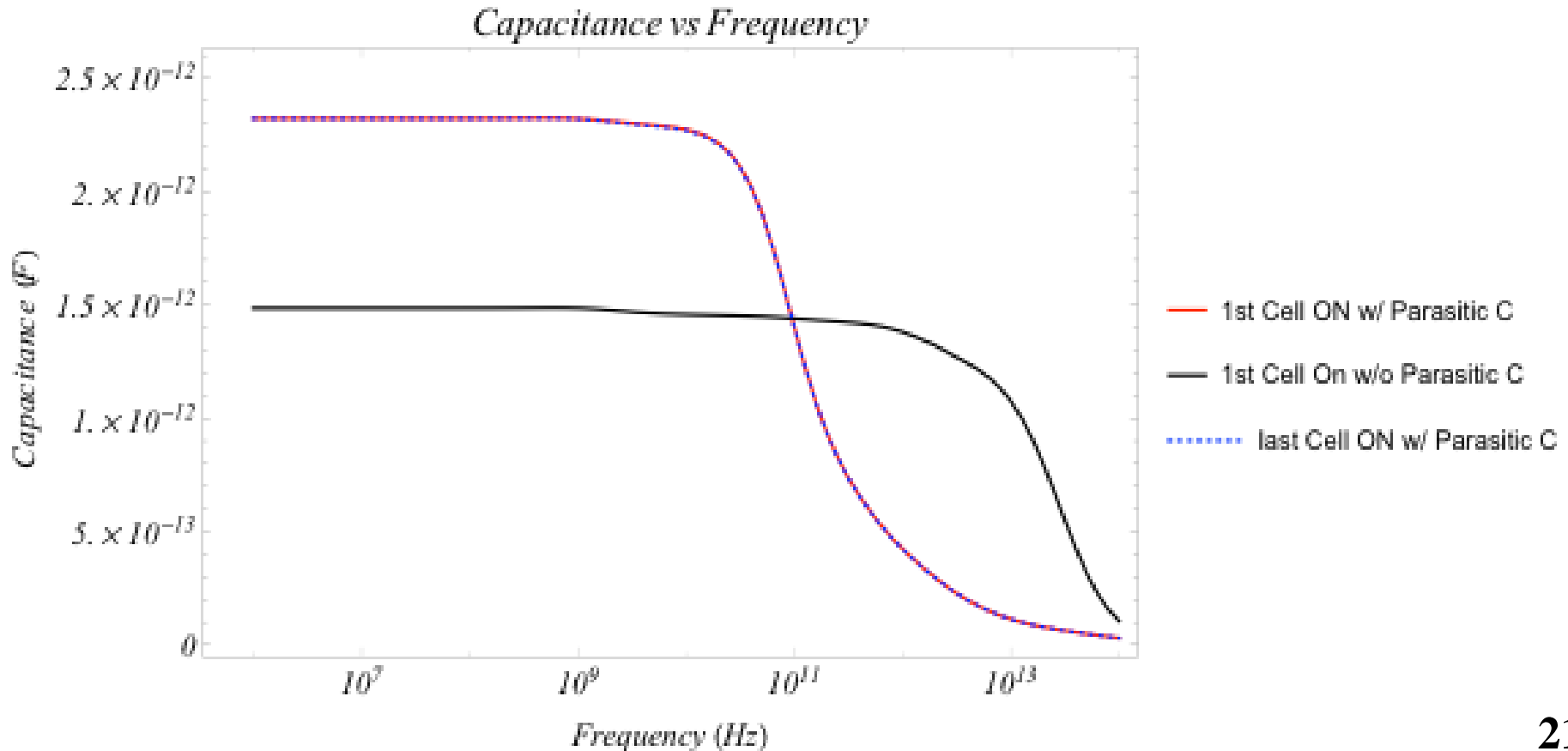
Sampling cell (1 unit)
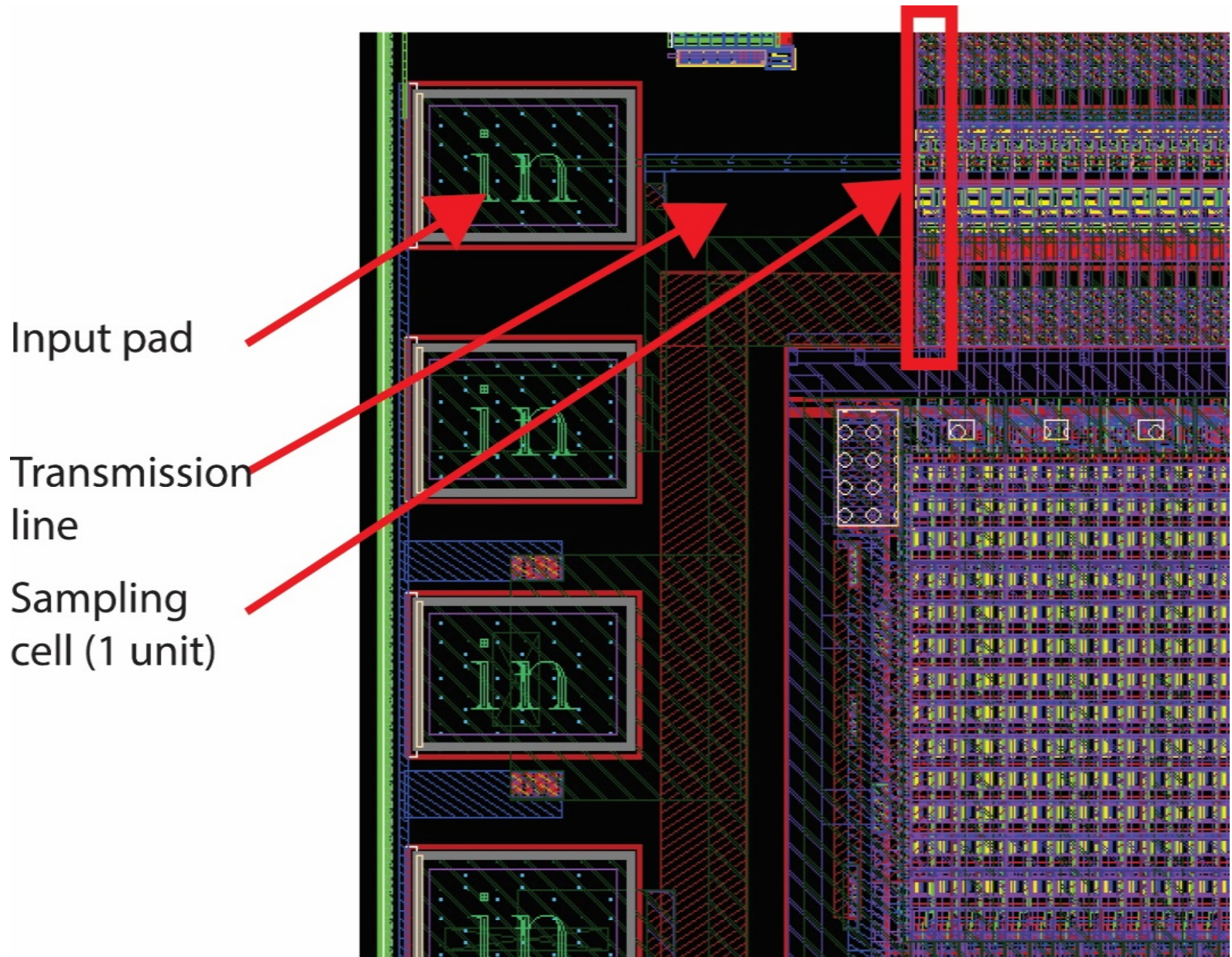
PSEC4 Analysis: Single Sampling Cell

Structure & Layout

Top view

Driver circuit

Switch tranzistors

Sampling capacitor

Transmission line

Side view

Transmission line

Thick Metal

OUT

Capacitor

Switch

Switch Driver

Substrate
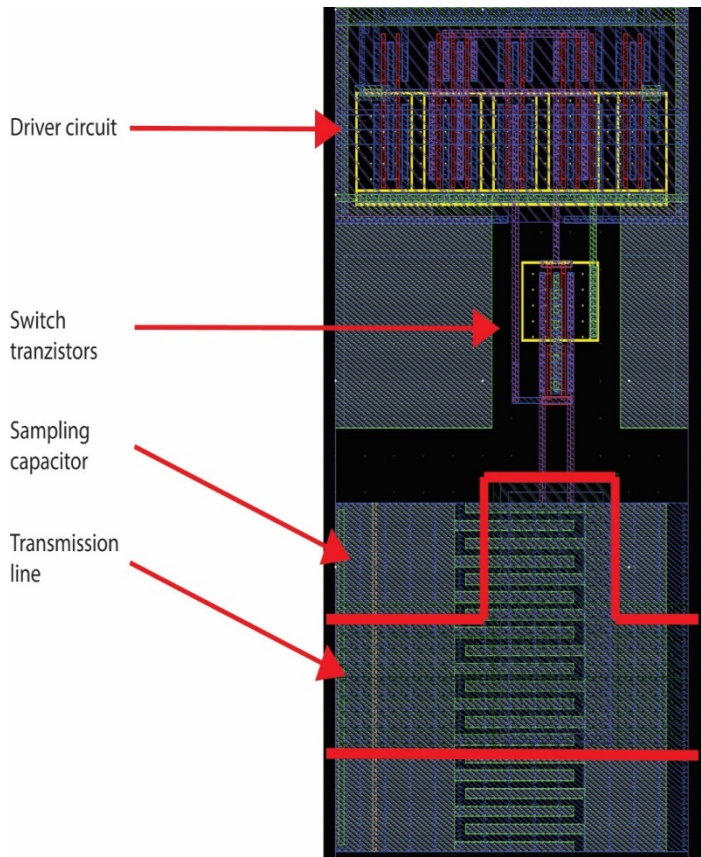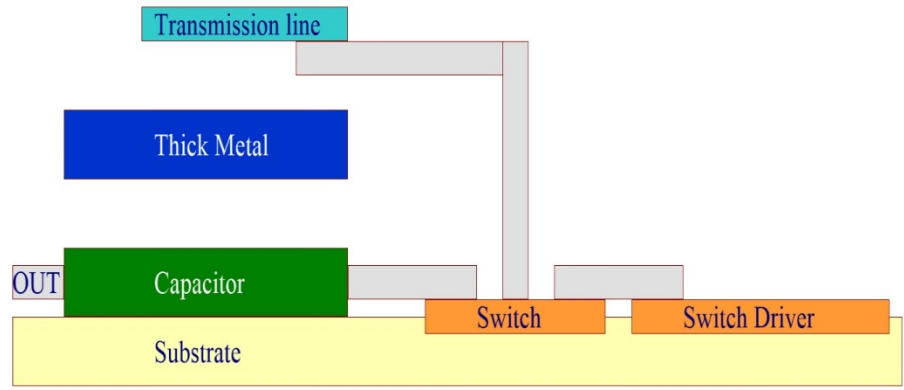
Single Sampling Cell Coupling

Simplified Schematic
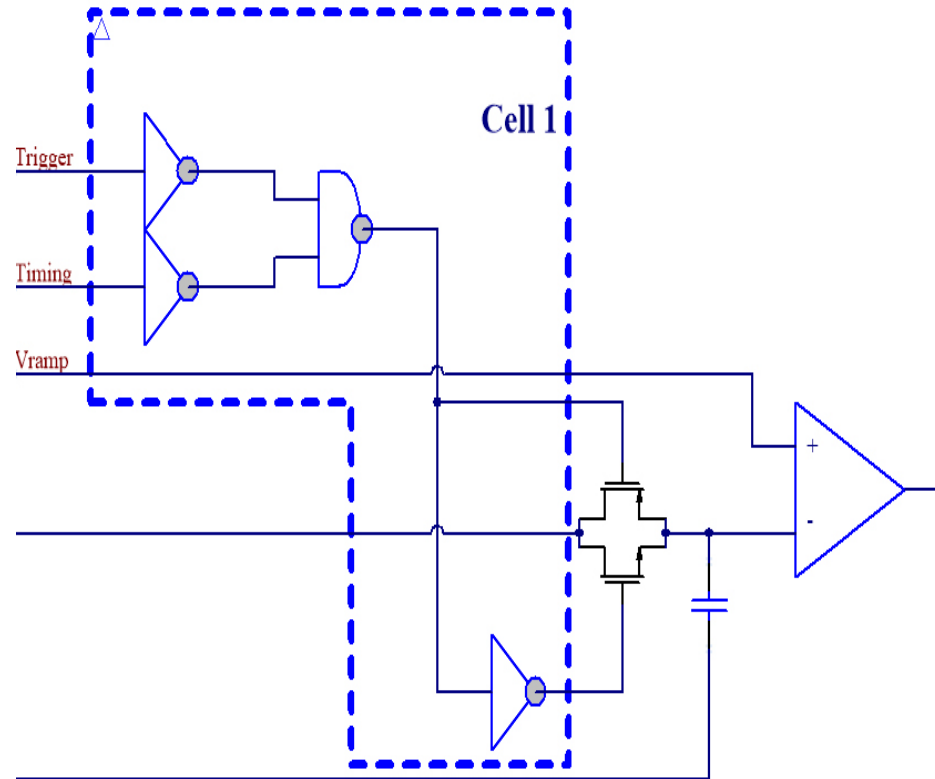
- Driver circuit
- Switch with n-p FET pair
- Sampling capacitor
- Comparator as load

Switch & Sampling Capacitor Equivalent Circuit
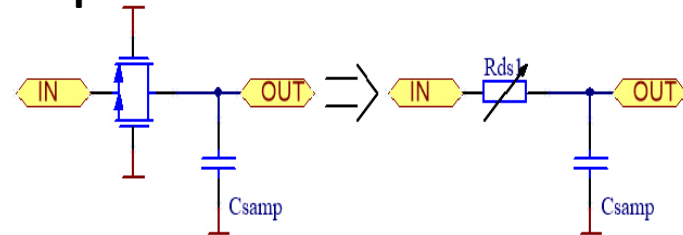
- Check Csampling capacitance
- Identify Ron and Roff

Sampling Capacitor Spread
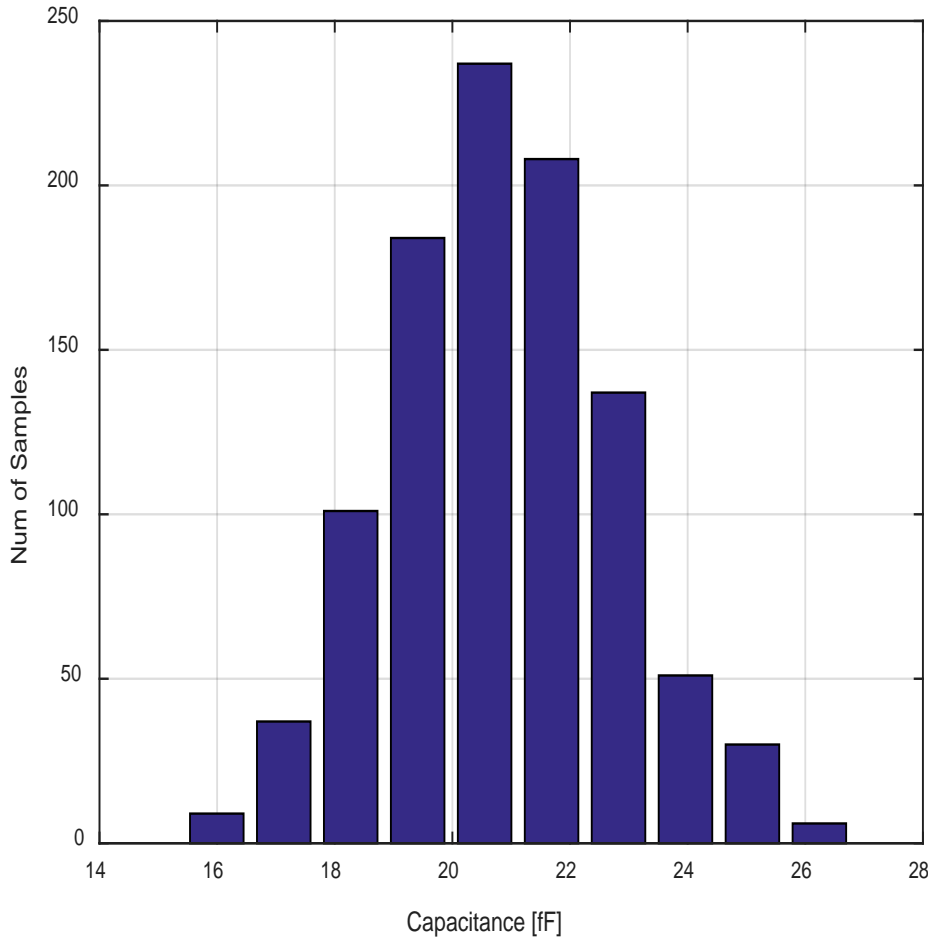
Monte Carlo with process variation and mismatches shows a discrepancy between Csampling Schematic (13.5 fF) and Measured mean (20.27 fF).

The Spread is about 1.9fF which makes the Capacitor tolerance at about 9.3%

Num. of Samp.	MEAN	STD	MIN	MAX
1000	20.27 fF	1.89 fF	14.86 fF	26.24 fF

Pass Transistor (Switch) Resistance

TRACK state
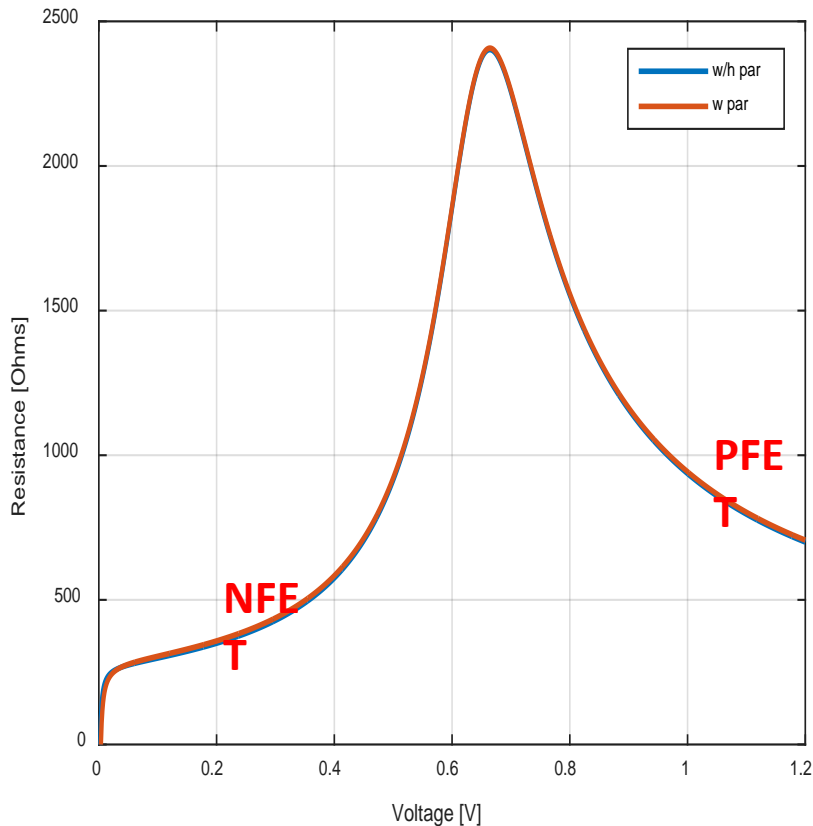
HOLD state

- **Ron=2.4k @665mVdc**
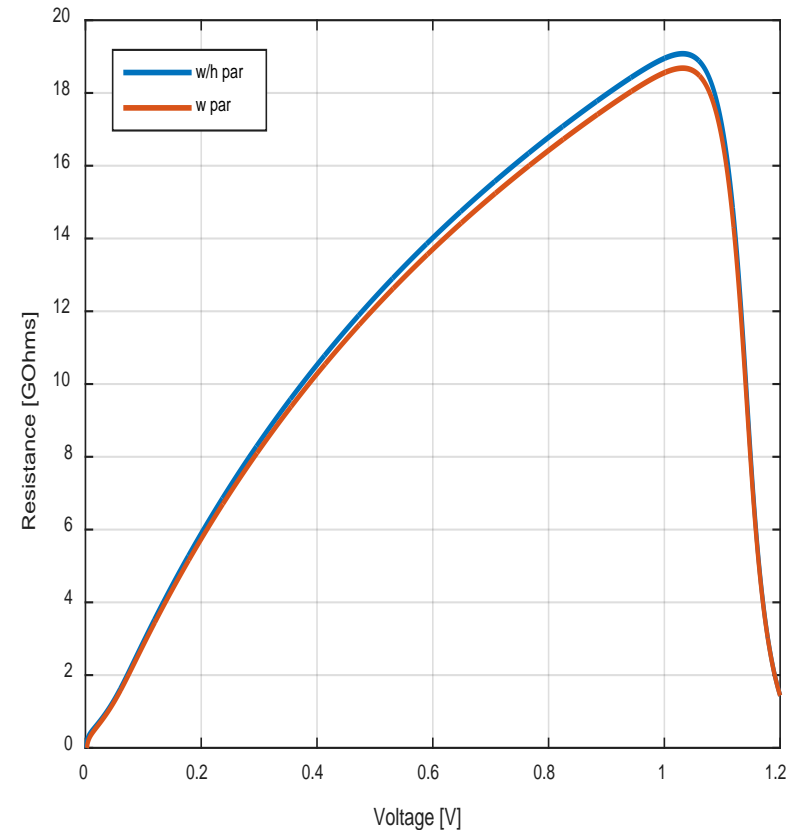
- **Roff is in GΩ**

- **The PFET and NFET are not matched and Ron varies considerably**

Frequency Analysis

Performance: S(Z)-parameter
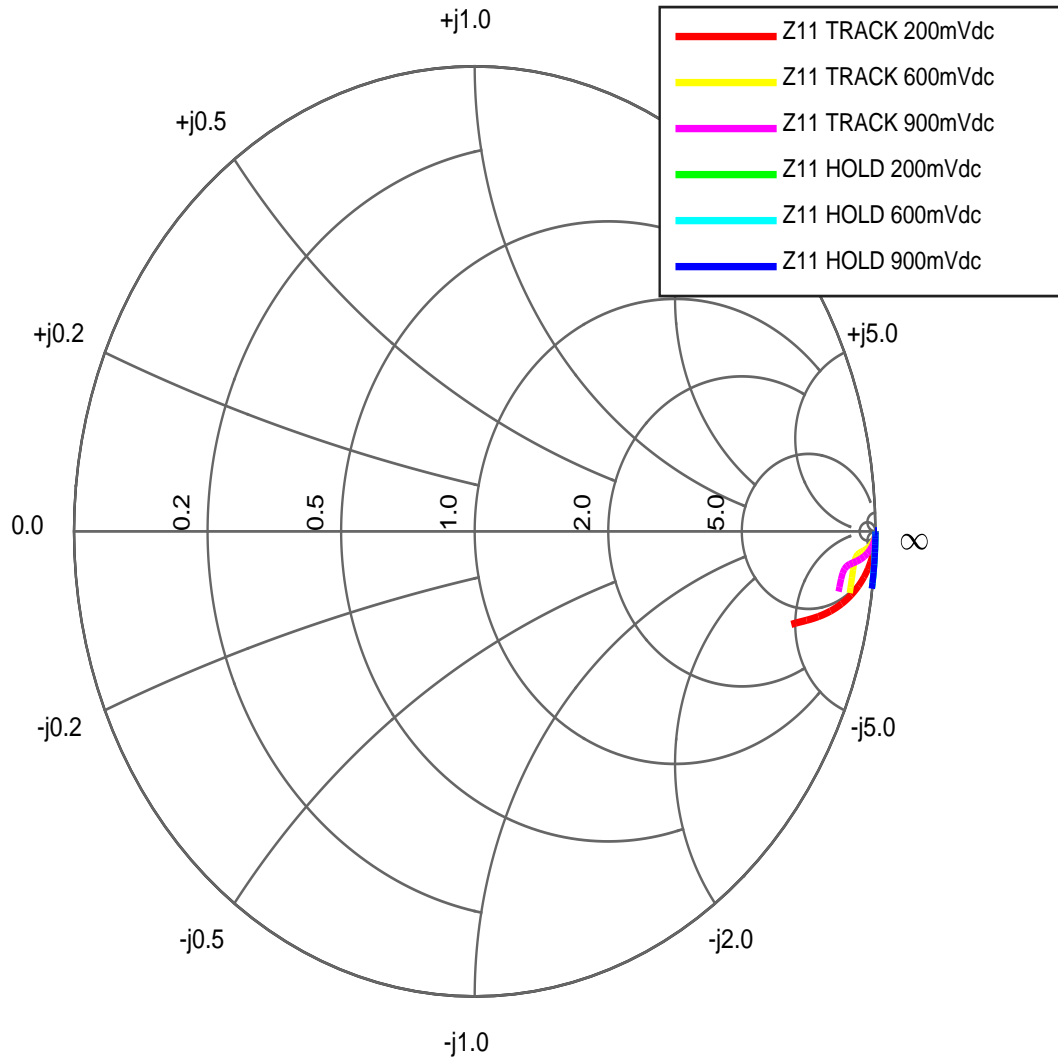
The input impedance is high and it is capacitive.

Input coupling analysis
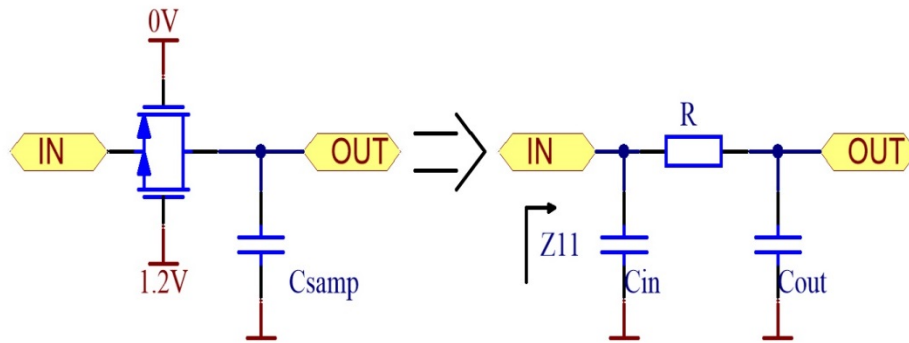
$$Z_{11} = \frac{1 + sC_{OUT}R}{s^2 C_{IN} C_{OUT} R + s(C_{IN} + C_{OUT})}$$

The transfer function parts:
- input parasitic capacitance of the transistor plus capacitance of the transmission line section.
- Series resistance of the transistor channel (Rds)
- Output capacitance which is formed of the parasitic capacitance of the transistor, sampling capacitor and load capacitance
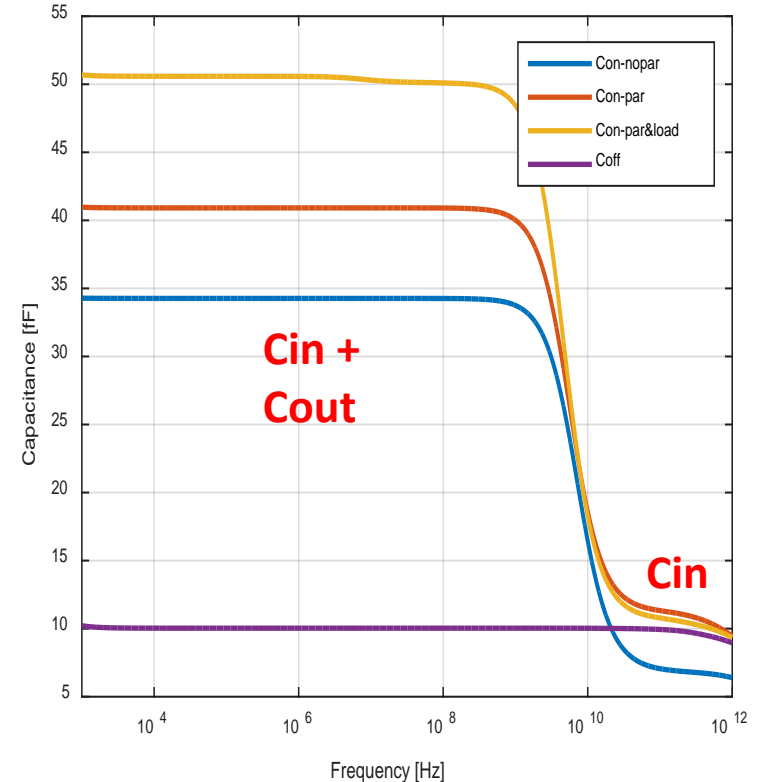
Capacitance	Value [fF]
Cin_open	8fF
Csw_out	10fF
Csamp	20.3fF
Cload	13fF

Small signal frequency response

Bandwidth
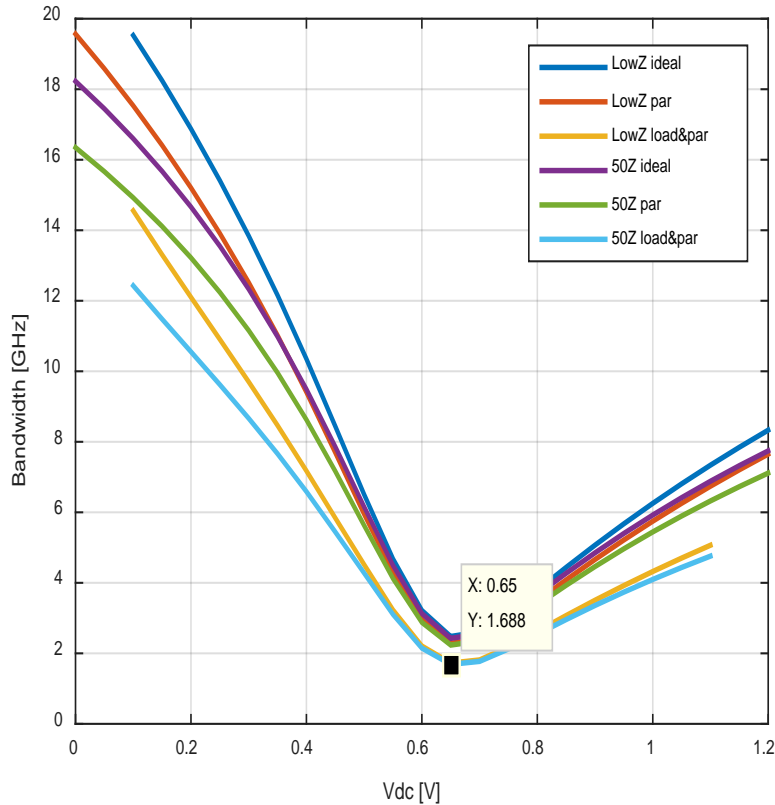
Isolation

- **BWworst≈2.3GHz @665mVdc @LowZ drive**

- **BWworst≈1.7GHz @665mVdc @50Ω drive**
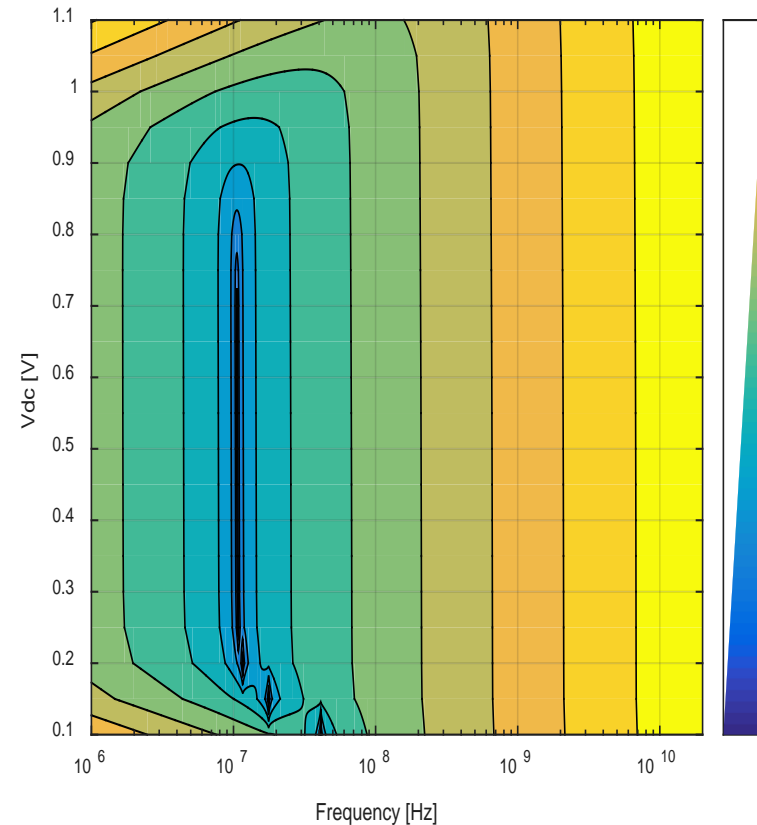
- **Isolation is over 60dB over all parameter space**

Small signal phase analysis

Group Delay without the load
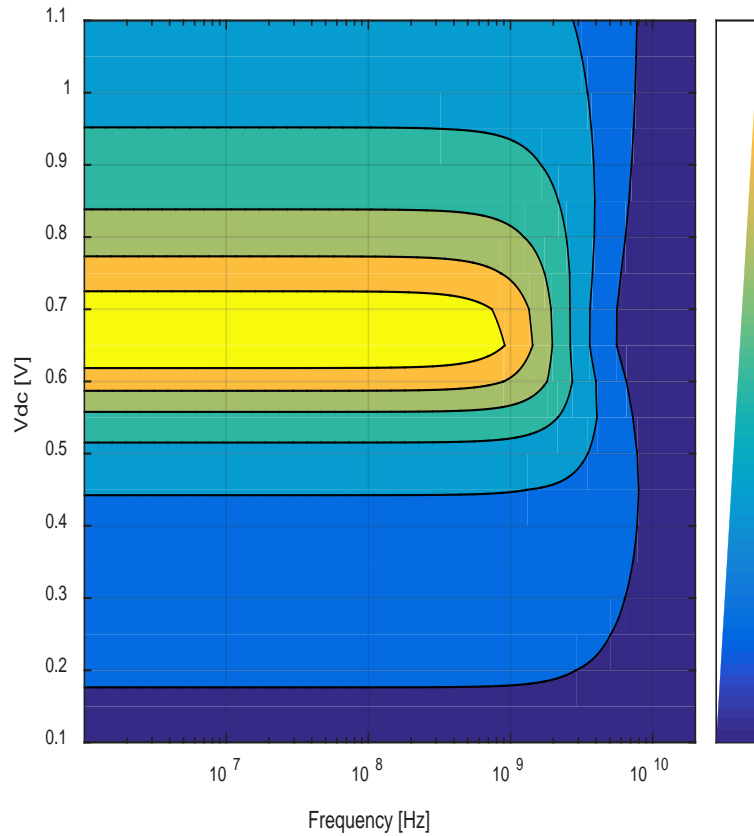
Group Delay with the load
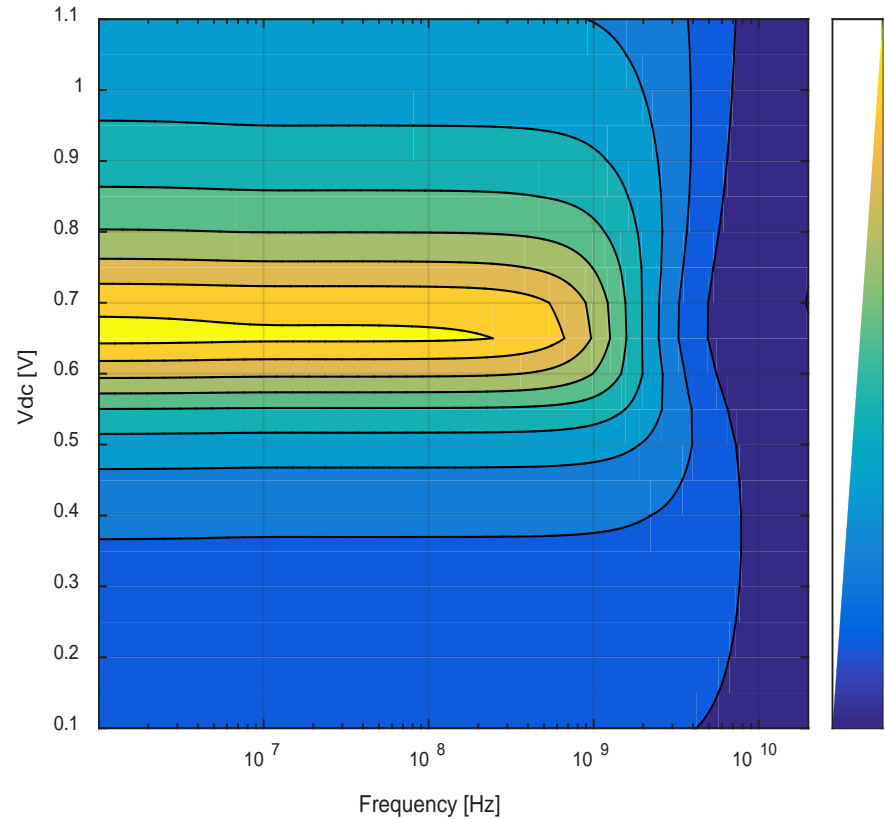
➜ **Large group delay variation points to large distortion**

Large signal response (I)

Low frequency gain compression

High frequency gain compression
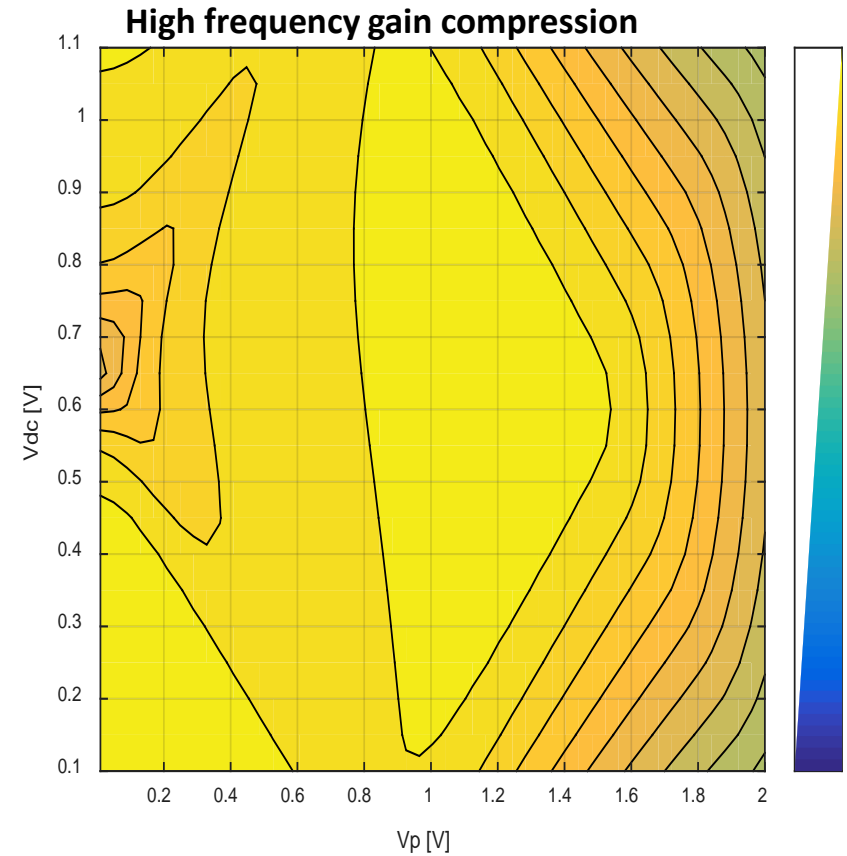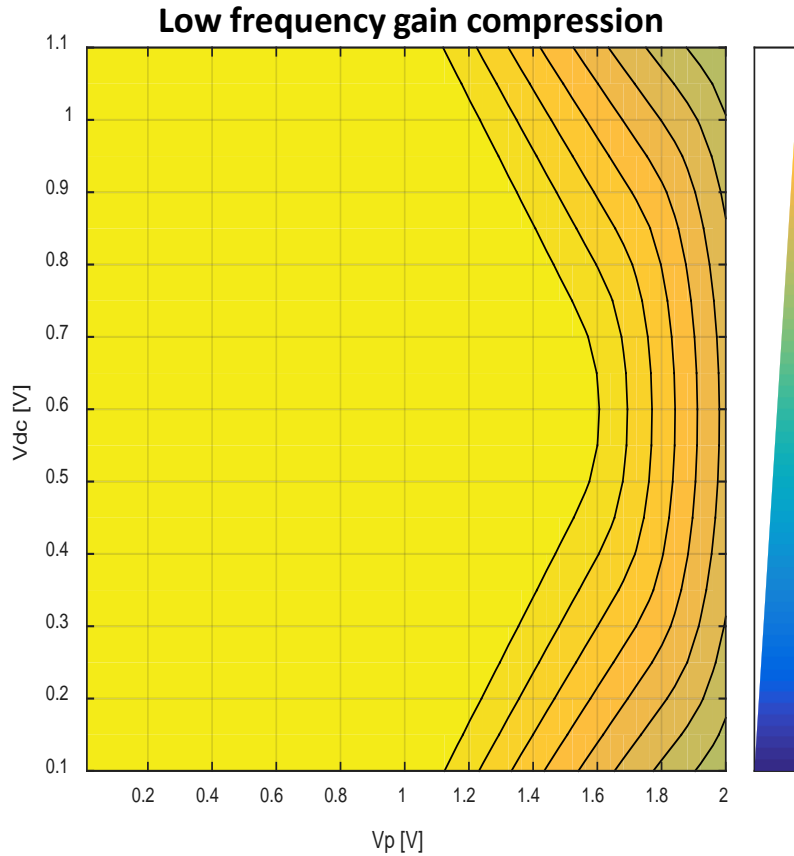
- **Full dynamic range at low frequency, compression appears when reaching the voltage threshold of the PN junctions at the drain/substrate barrier.**

- **Gain compression at lower and higher amplitudes**

Large signal analysis (II)

High frequency gain compression & distortion
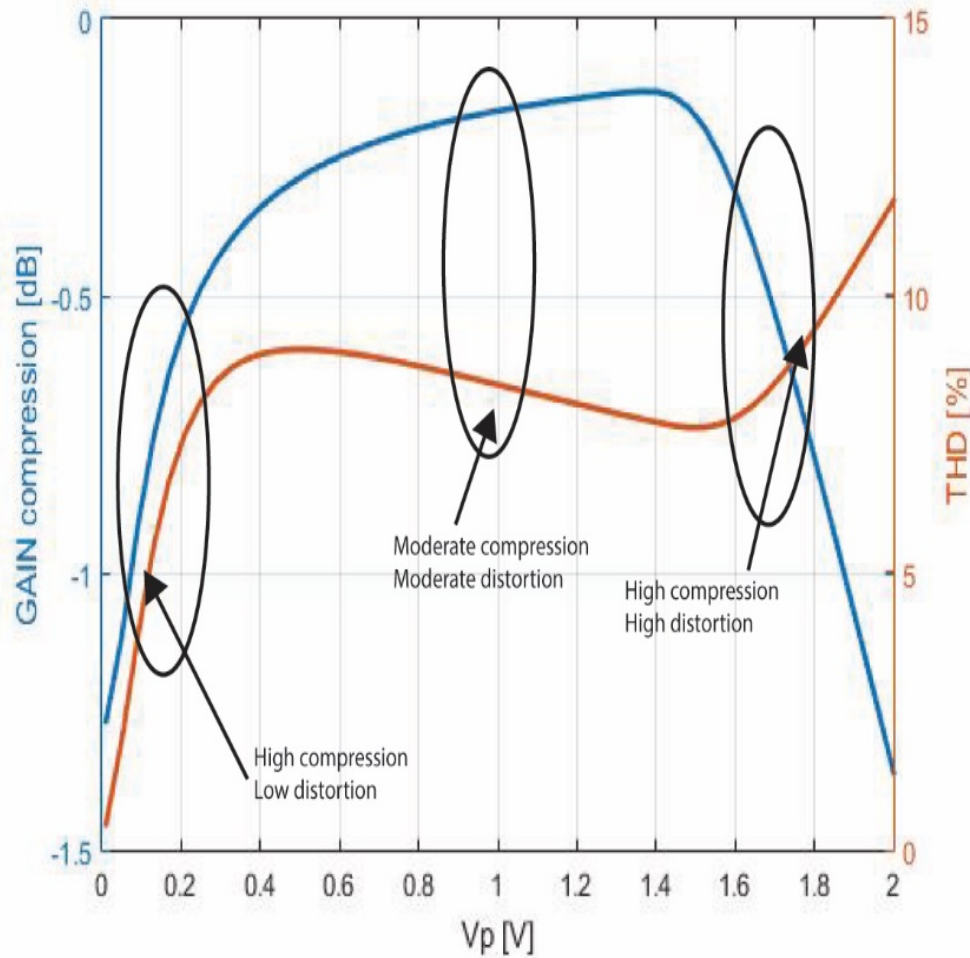
Three region of operation:
- **Low distortion & High compression**
- **Moderate distortion & Moderate compression**
- **High distortion & High compression**
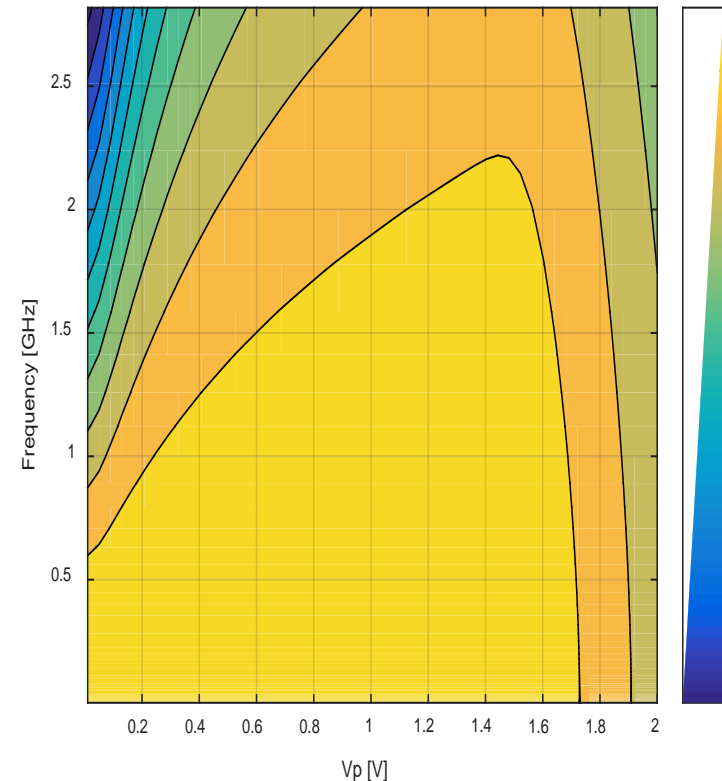
Understanding signal response

Low distortion & High compression
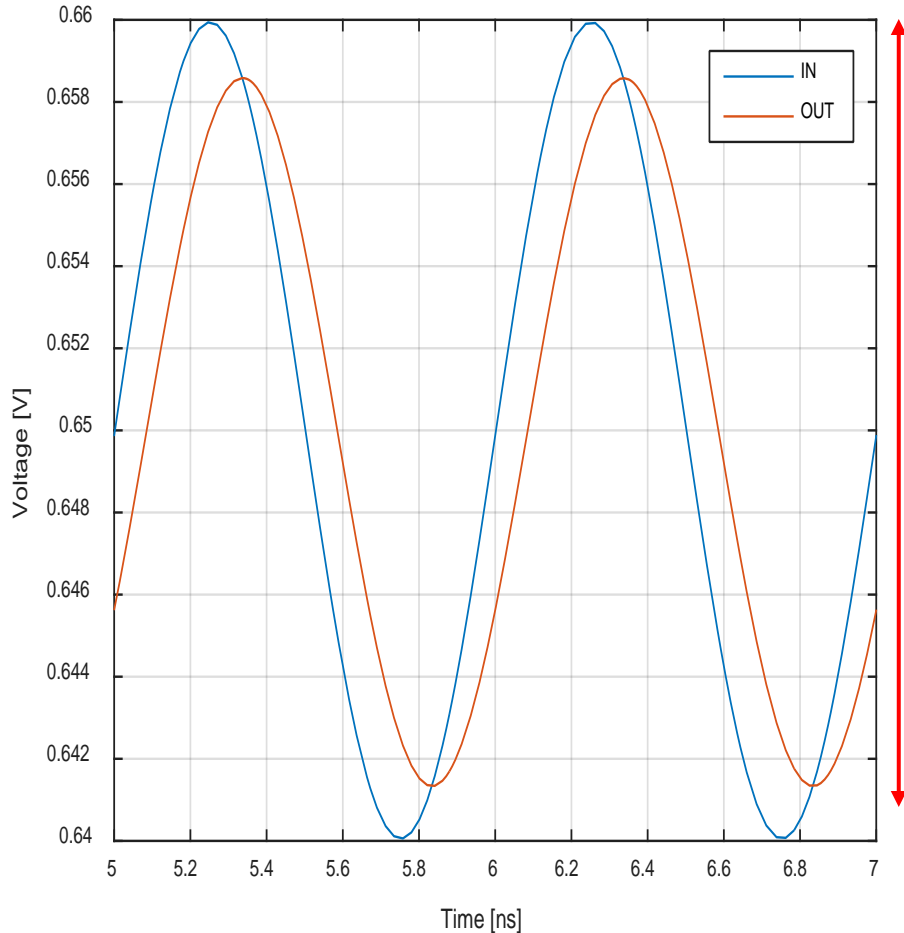
- **Resistance of the channel does not vary much   -> Low distortion**
- **At high resistance the bandwidth is limited   -> lowering of the gain (compression)**

TRACK state
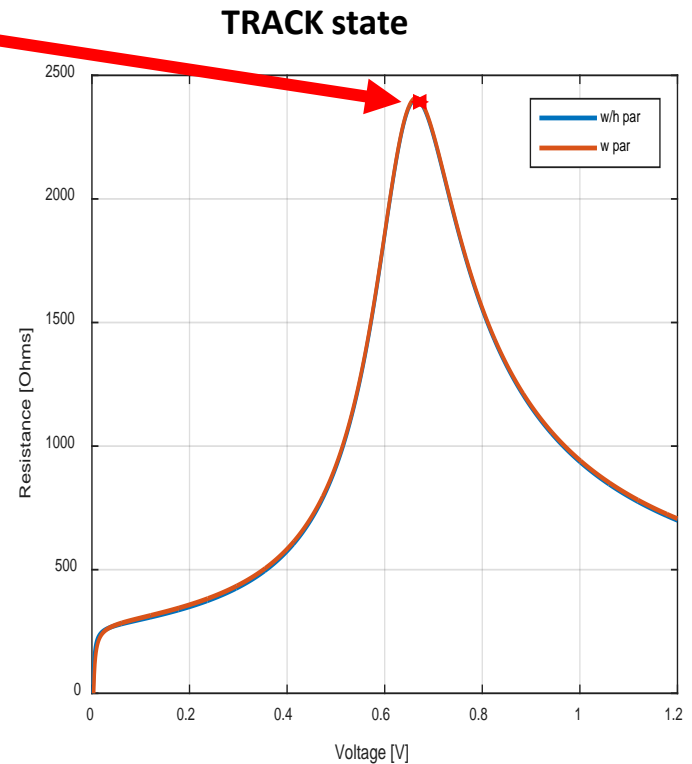
Understanding signal response

Moderate distortion & Moderate compression
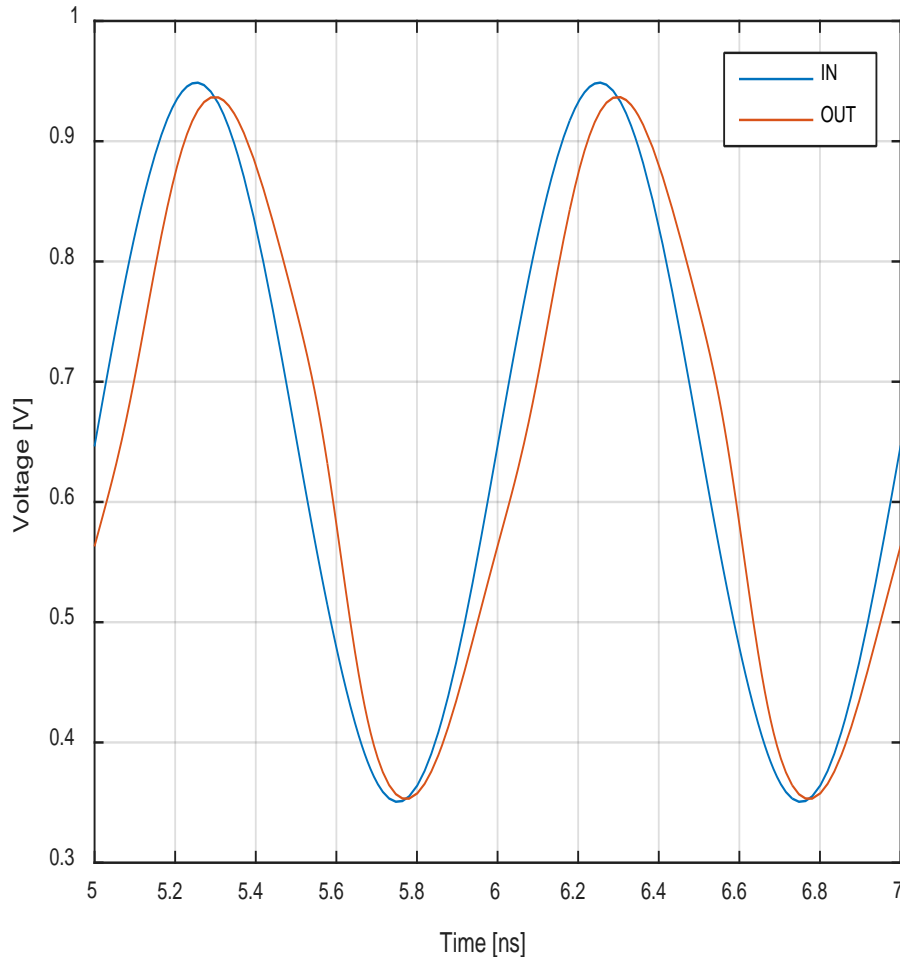
- **Resistance of the channel is varying**
  -> The bandwidth at instantaneous values of the incident voltage waveform is different

  -> In frequency domain this gives rise to higher harmonics, which interfere constructively hence increasing the overall signal amplitude but also increases distortion

TRACK state
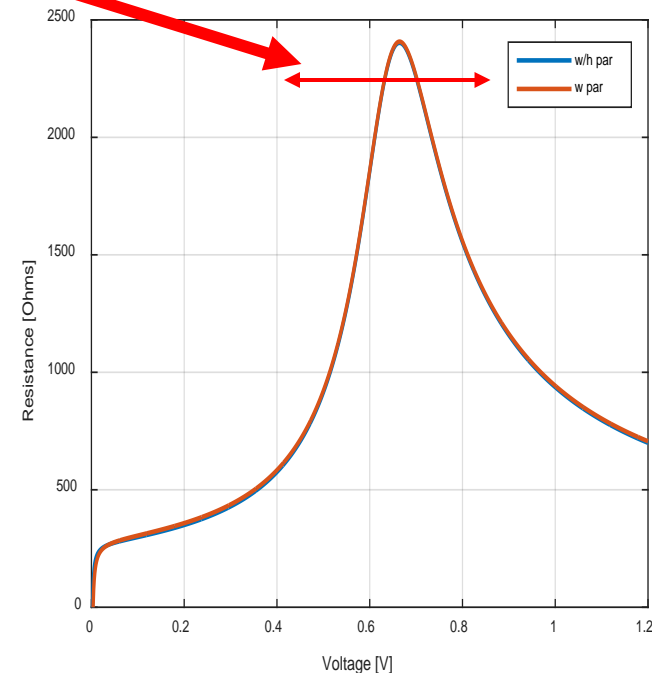
Harmonic decomposition

Time domain decomposition

Frequency domain decomposition
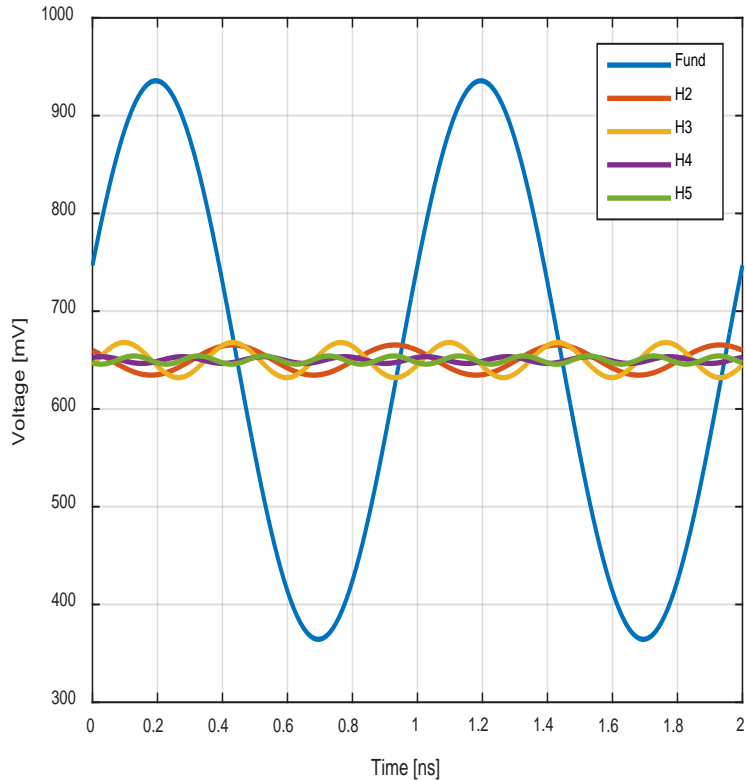
- **Constructive interference of odd harmonics and destructive interference of even harmonics at the peaks**
- **Constructive interference of second and third harmonics at zero crossing**
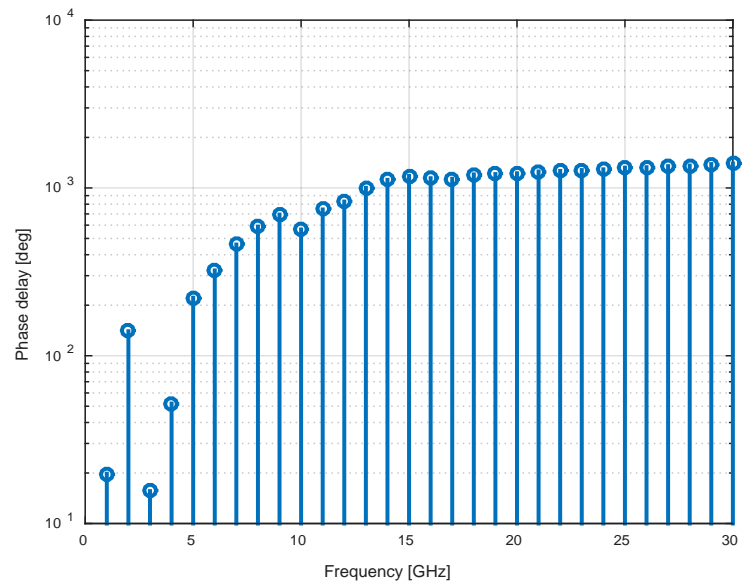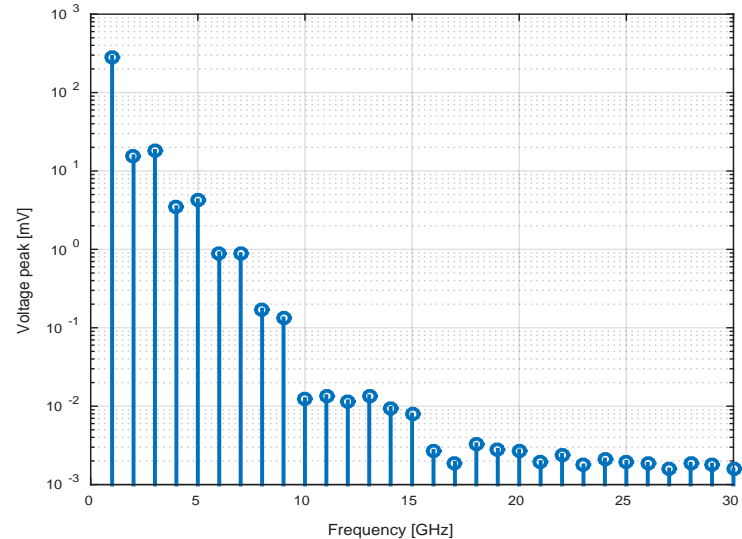
Noise and Distortion

Input referred noise

Integrated referred noise
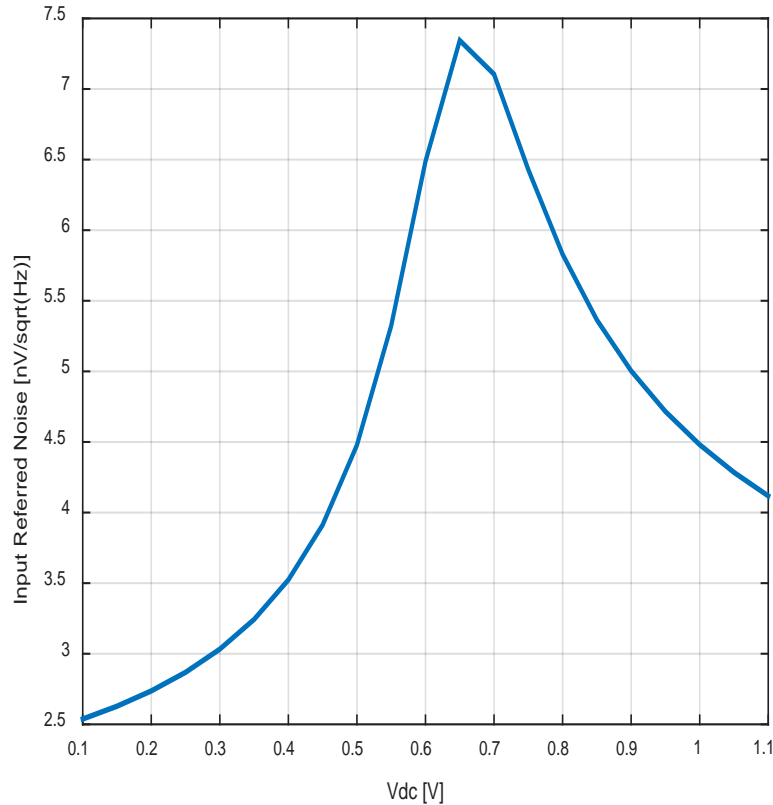
- **Noise dominated by the ON resistance of the channel**
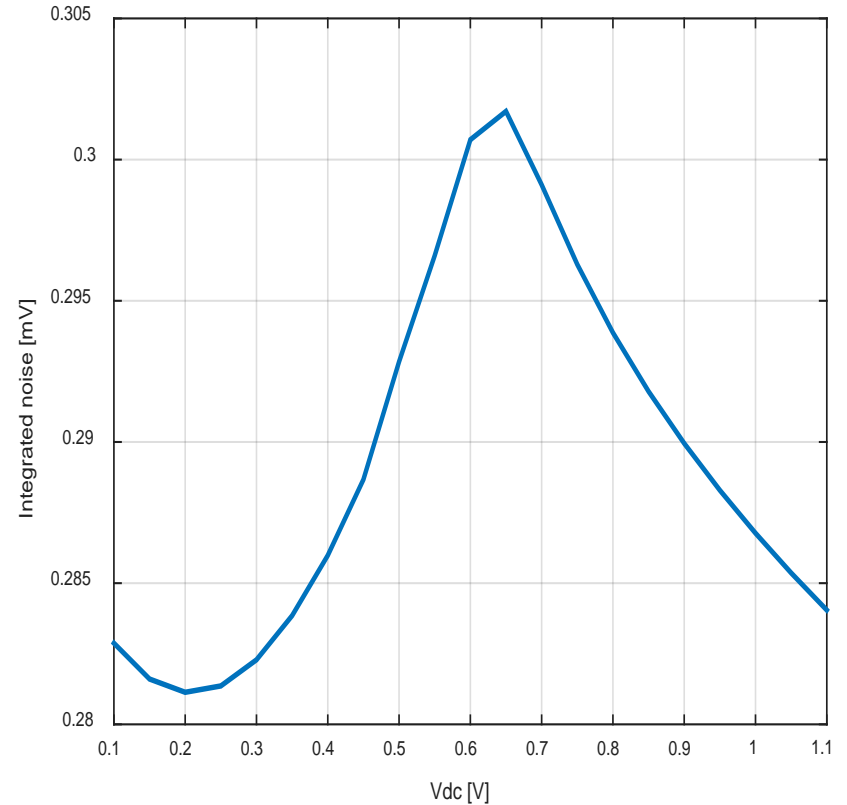
- **Total noise is around 0.29mV ± 0.01 mV**

Noise, distortion and dynamic range

Signal to Noise Ratio at full scale input (1Vpp)
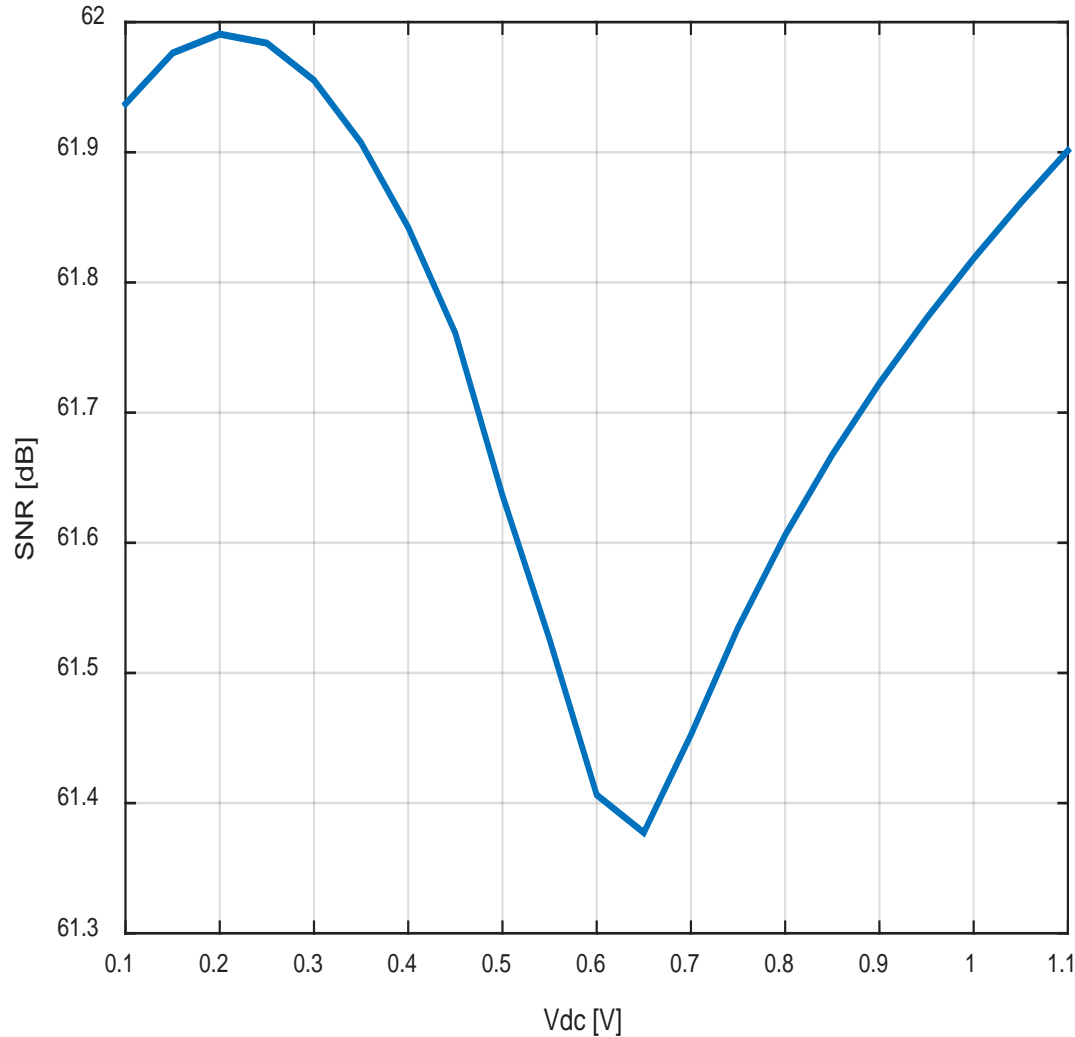
- **SNR is around 61.7dB ± 0.3 dB**

Distortion analysis

Distortion at fixed Vdc
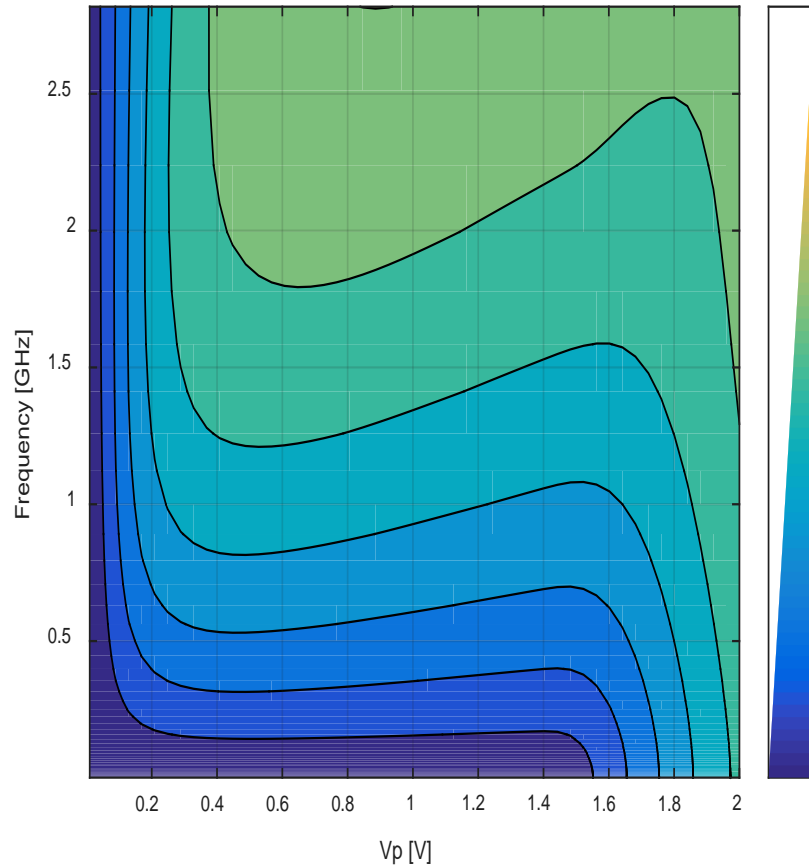
Distortion at fixed Frequency
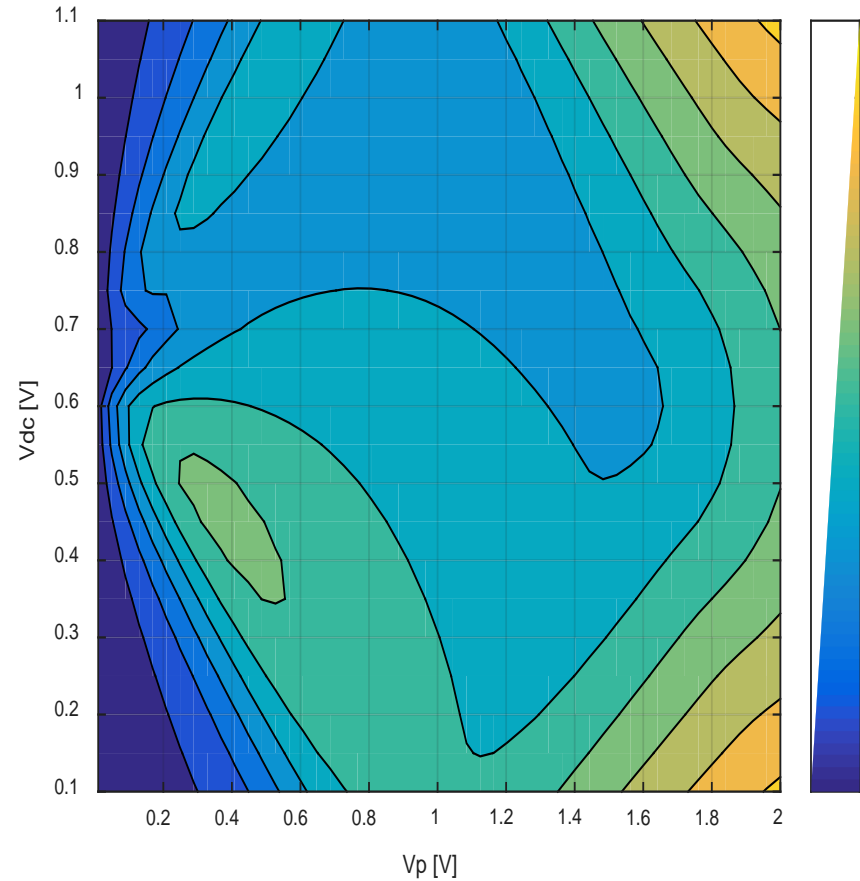
- **Most of the distortion comes from the Ron variation over the input voltage range**

SINAD & ENOB assessment

$$SINAD = -10\log_{10}\left[10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}}\right]$$

$$ENOB = \frac{SINAD - 1.76 + 20\log_{10}\left(\frac{Fullscale}{Input}\right)}{6.02}$$

ENOB versus frequency
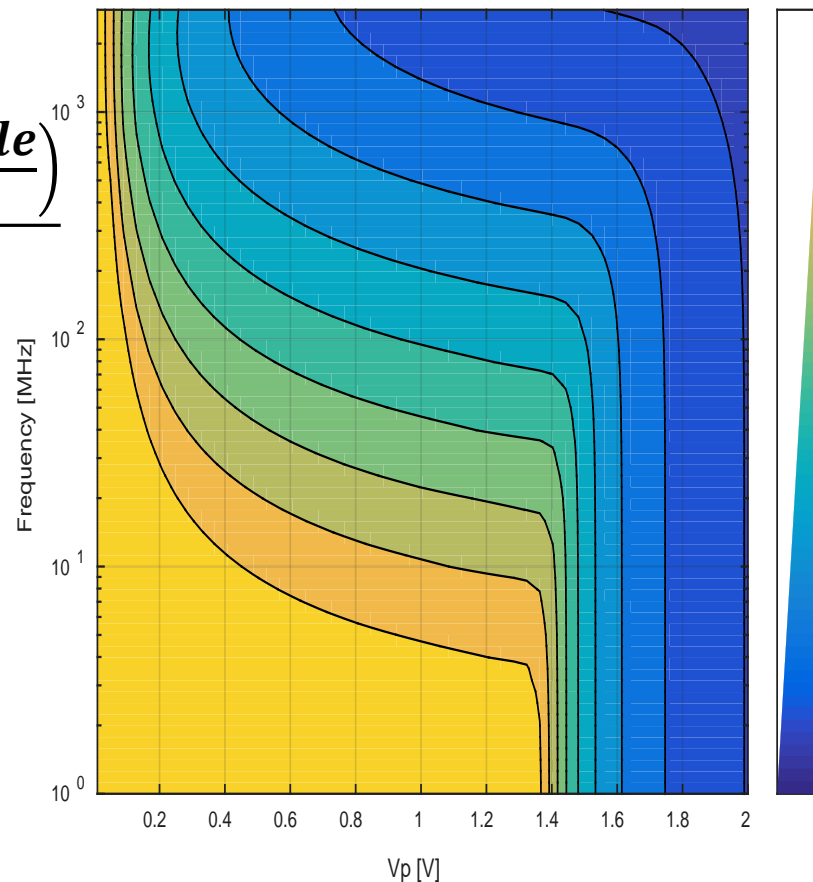
ENOB at low frequency
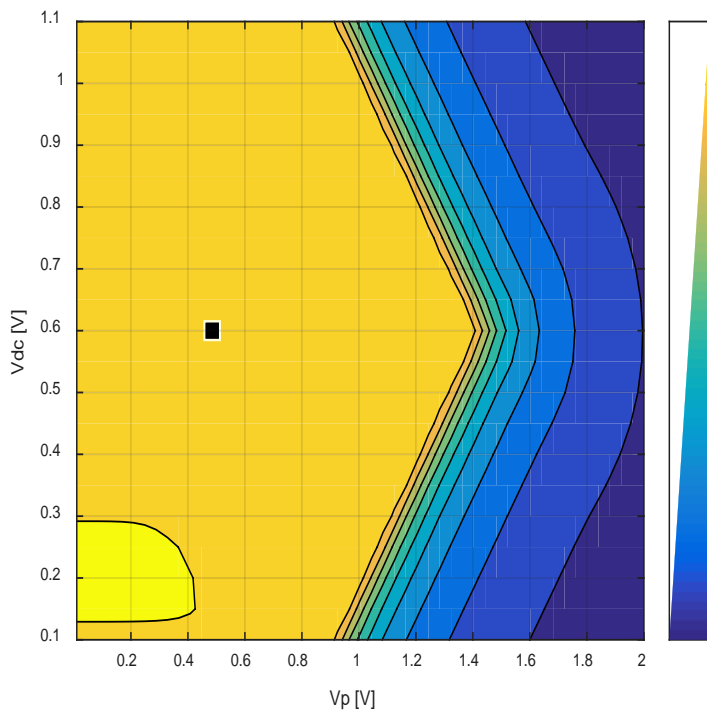
- **ENOB DOMINATED BY DISTORTION**

Transient Response

Transient response at 600 mVdc
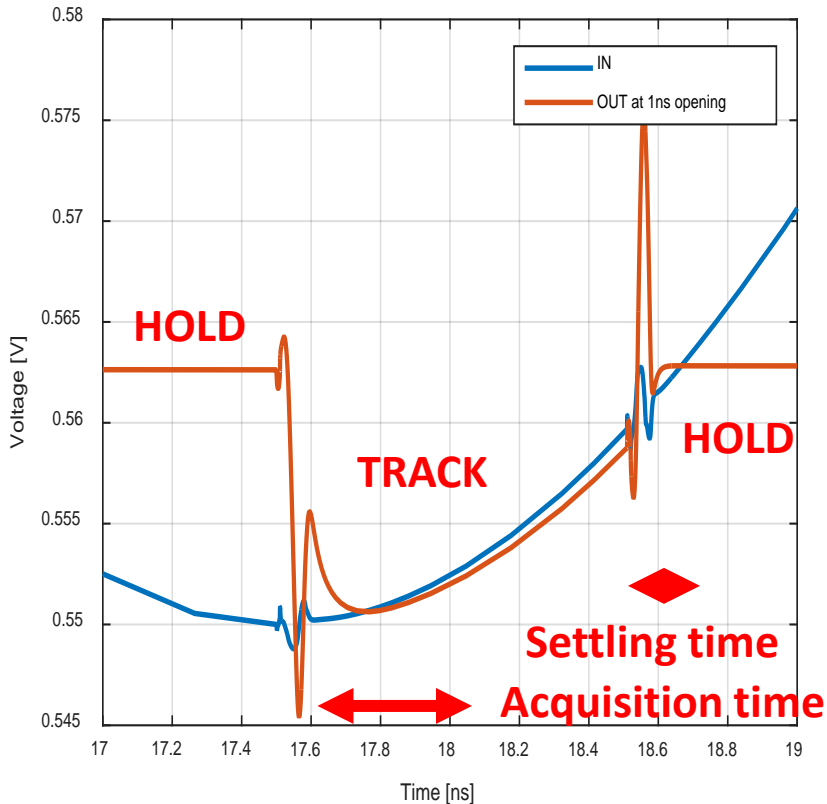
Transient response at 300 mVdc
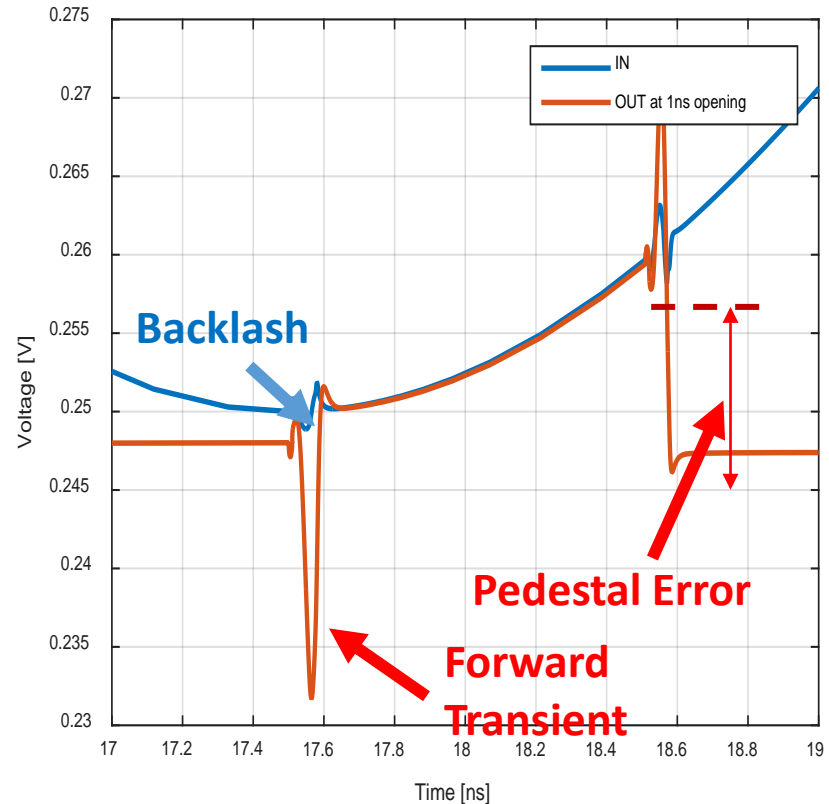
Input Vdc voltage	Acquisition time	Settling time
300mV	0.14ns	0.11ns
600mV	0.68ns	0.11ns
900mV	0.52ns	0.11ns

- **Worst case window time is 0.8ns or 1.25GHz -> due to low bandwidth**
- **Best case is 0.25ns or 4GHz**

- **15% backlash at 30mV forward transient**
- **Pedestal error due to charge injection and transistor mismatch dominate**

Summary – Requirements comparison

Parameter	Measured (worst cases)	Requirement
Bandwidth (Single cell)	1.7GHz @665Vdc @50Ω	3GHz
Bandwidth (Multi cell)	1.0GHz @665Vdc @50Ω	3GHz
SNR	61.7 dB	58dB
ENOB	9.8 bits (small region)	9.4 bits

Things to improve:

- **Reduce Ron variance over the dynamic range to reduce distortion and increase the ENOB**
- **Bandwidth dominated by Cin:**
  - **Reduce Cin or reshape the channel to increase the bandwidth (first pole)**
  - **Reduce Ron overall value to increase the bandwidth (second pole)**
- Speed dominated by bandwidth:
  - Increase bandwidth
  - Overlapping of sampling cell windows to increase the effective sampling frequency
- Use differential configuration to reduce pedestal error and increase noise coupling and crosstalk immunity

Future Plans

- Now in detector, not readout limited timing regime
- PSEC5 ASIC
  - $256 \rightarrow 32$k sample storage
  - Work to optimize bandwidth, ENOB
  - Persistence effects
- RFpix ASIC
  - Push limits of ABW, timing
  - Below 100-200fs, direct spatial measurement becomes interesting
  - Many practical issues, but none fundamental (CF 1ps)
- DRS5, SAMPIC ASICs
  - Will be interesting to see how well can perform

Back-up slides
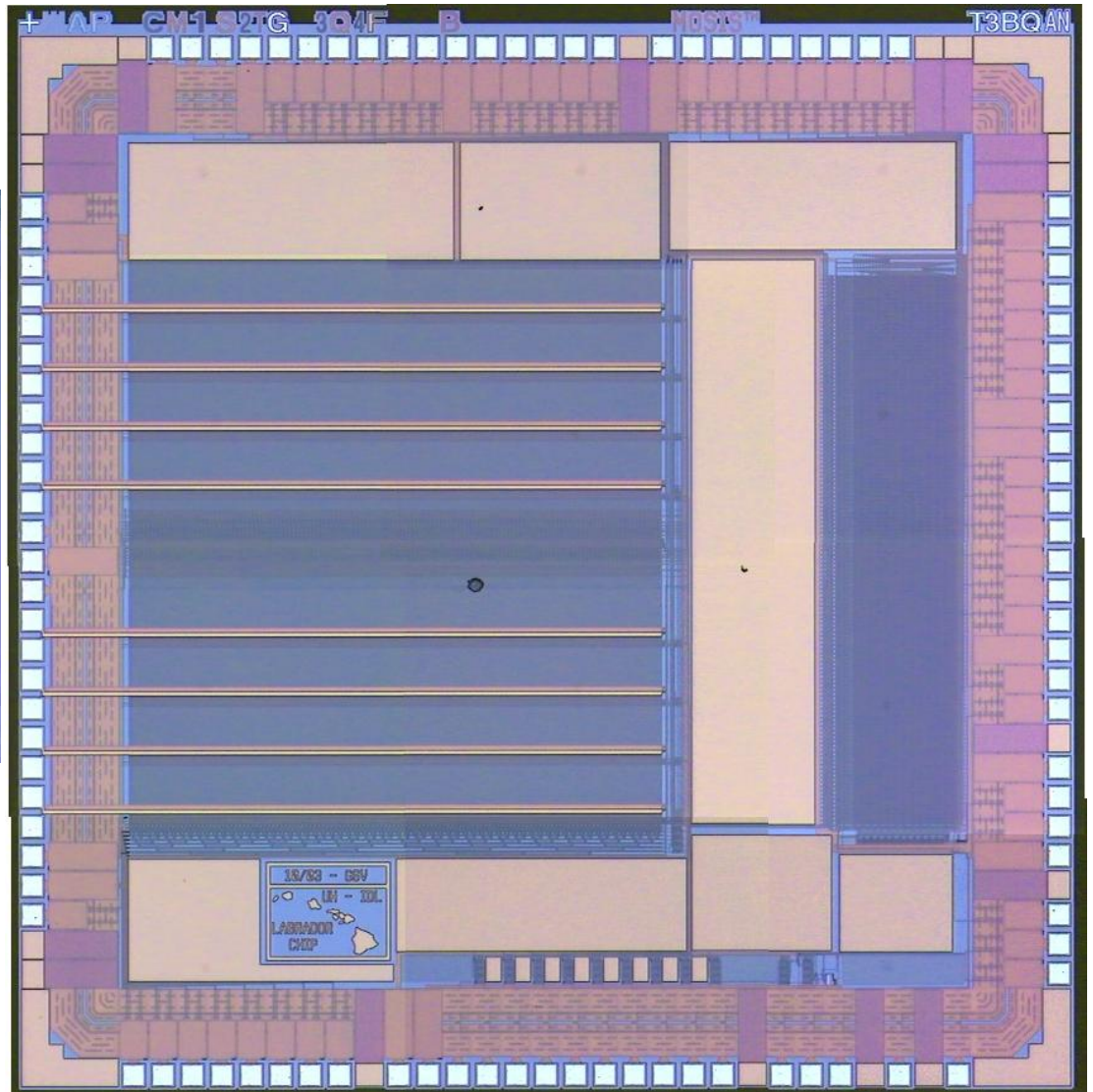
BLAB1 High speed Waveform sampling

- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited

NIM **A602** (2009) 438

CH1

CH2

6.4 psRMS

44
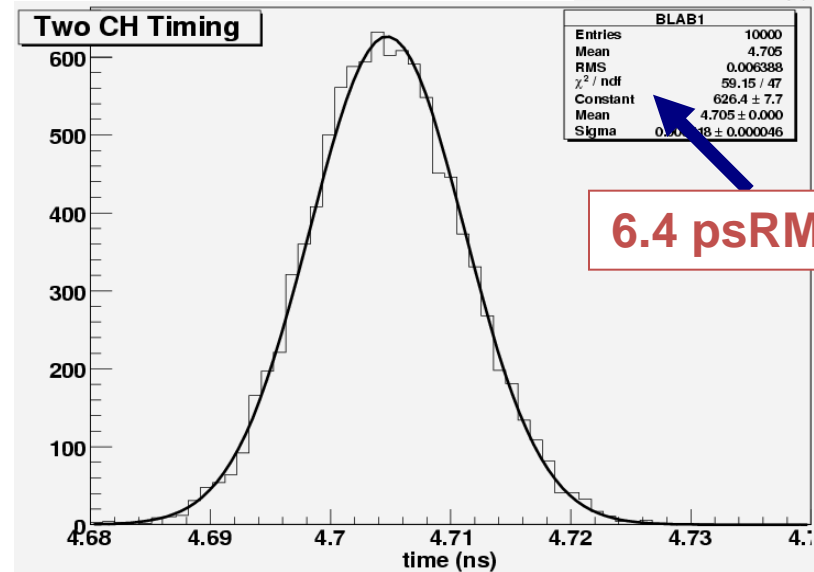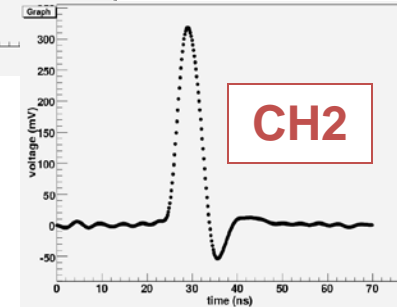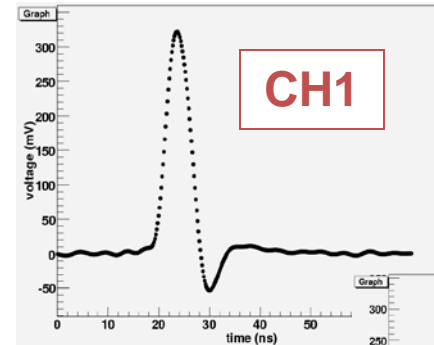
SL-10 Timing Performance
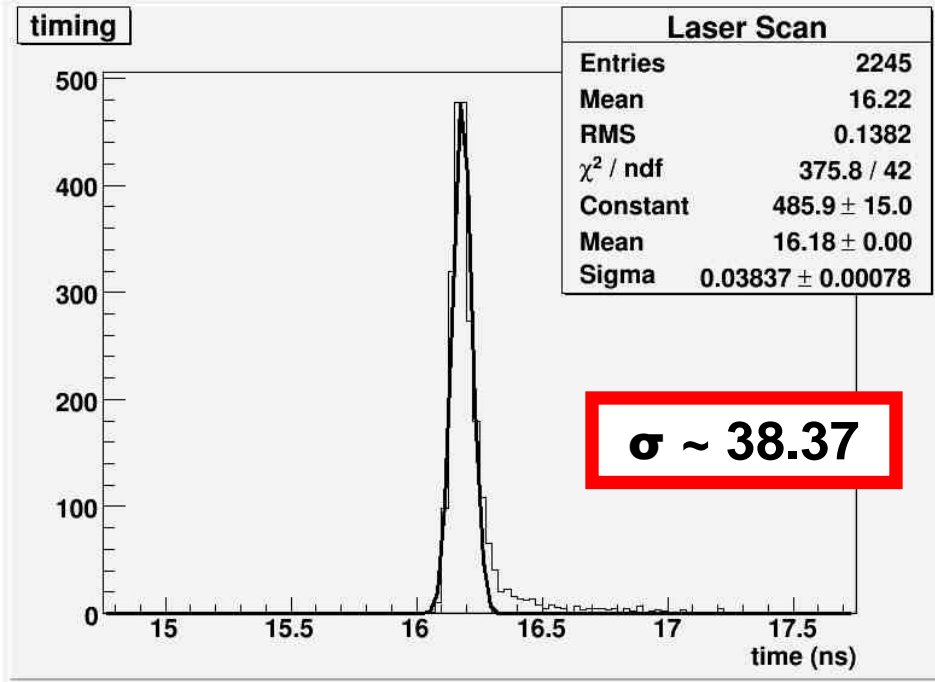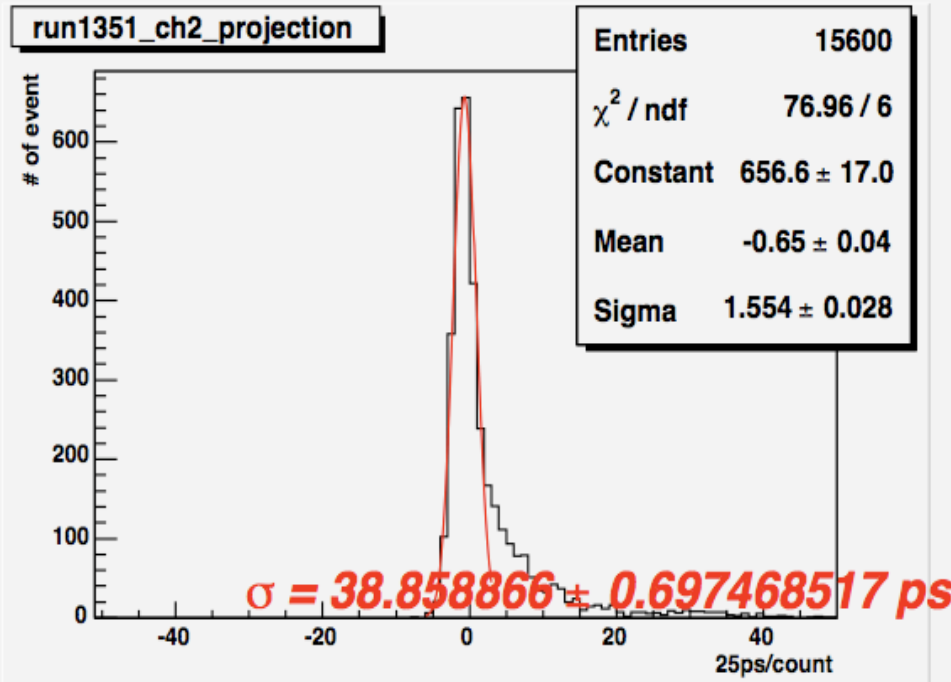
- **Nagoya = constant fraction discriminator + CAMAC ADC/TDC**
- **Hawai'i = waveform sampling + feature extraction**

Design Choices

- **Input coupling**
  - Differential versus single-ended input
  - Needed analog bandwidth
  - Gain needed?

- **Sampling Options**
  - On-chip PLL/DLL
  - External DLL
  - Analog transfer vs. interrogate in situ

- **ADC and readout options**
  - Sequential output select vs. random access
  - On-chip vs. off-chip ADC
  - Serial, parallel, massively parallel

Many variants have been explored…

IRS/BLAB3
Single Channel

- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other ("ping-pong")
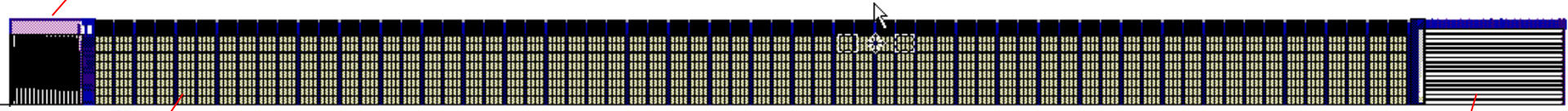
- Storage: 64 x 512 (512 = 8 * 64)
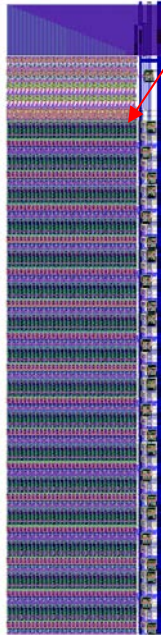
- Wilkinson (32x2): 64 conv/channel

IRS Die photo

5.82mm
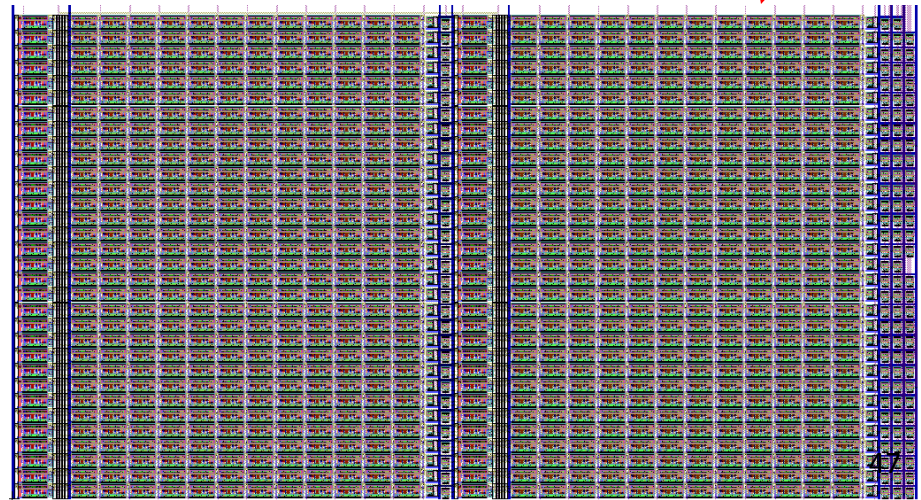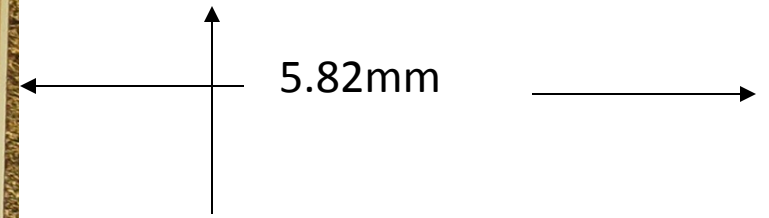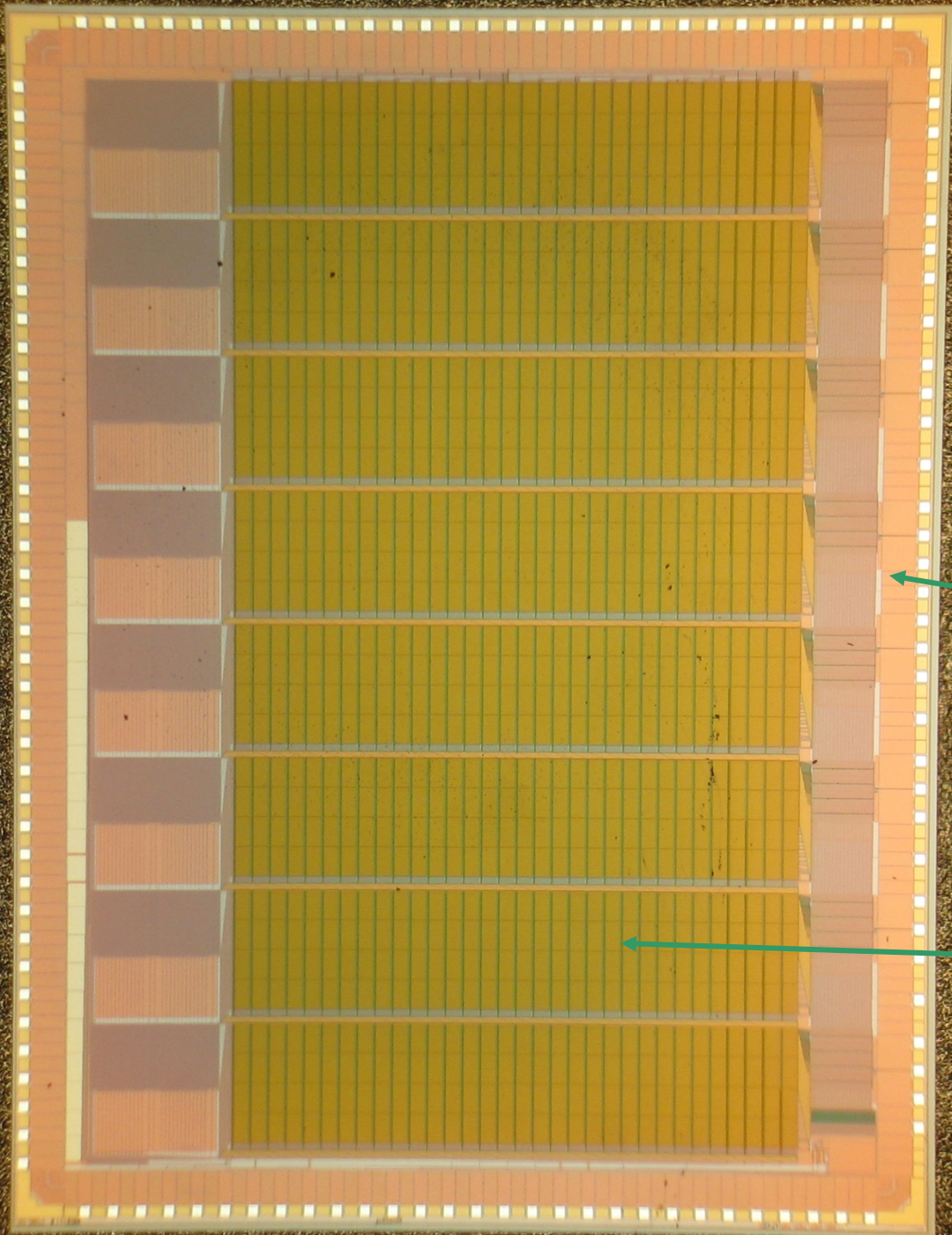
7.62mm

8x RF inputs
(die upside down)

32k storage cells
per channel
(512 groups of 64)

Deeper storage: Buffered LABRADOR (BLAB1) ASIC
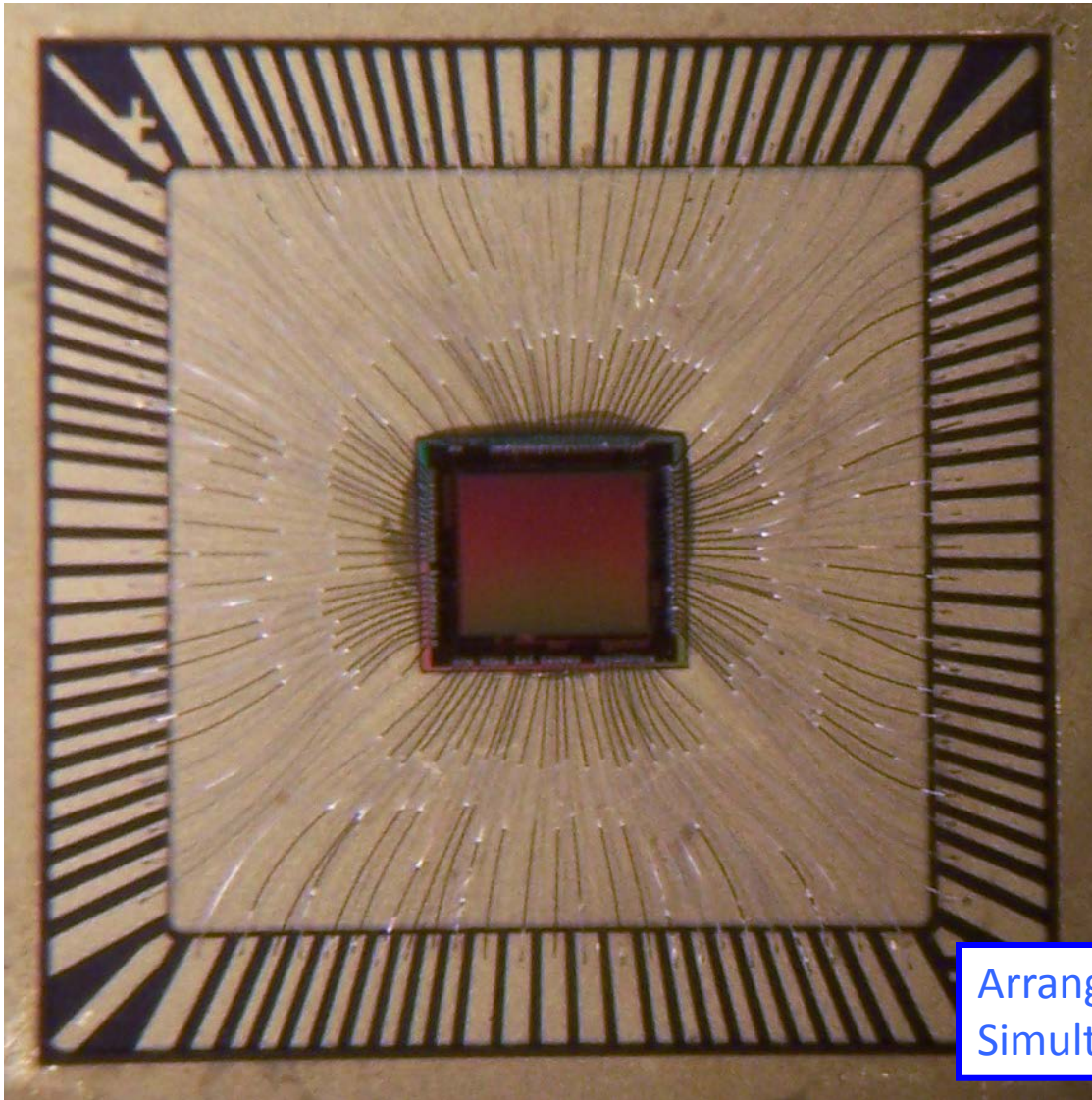
- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

Arranged as 128 x 512 samples
Simultaneous Write/Read

3mm x 2.8mm, TSMC 0.25um

Comparison of readout with CFD + CAMAC readout and UH waveform sampling
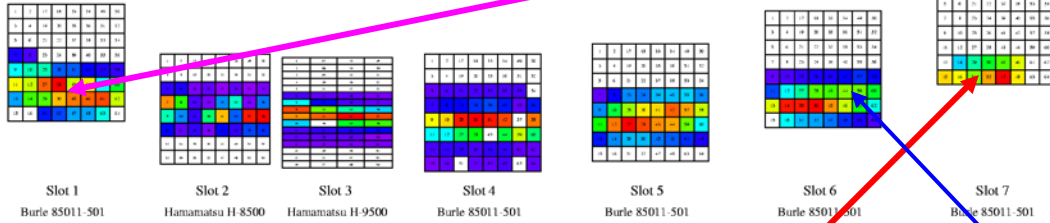
(symmetry partner in hit plane)

deltaT	
Integral	4568
χ² / ndf	225.3 / 82
Narrow Norm	319 ± 6.8
Narrow Mean	−0.08889 ± 0.00439
Narrow Sigma	0.2422 ± 0.0044
Wide Norm	12.44 ± 0.89
Wide Mean	0.9851 ± 0.0748
Wide Sigma	1.118 ± 0.044

slot 1, pad 28

σ≈240ps

Slot 1
Burle 85011-501

Slot 2
Hamamatsu H-8500

Slot 3
Hamamatsu H-9500

Slot 4
Burle 85011-501

Slot 5
Burle 85011-501

Slot 6
Burle 85011-501

Slot 7
Burle 85011-501

New BLAB-based Readout

deltaT	
Integral	5669
χ² / ndf	504.8 / 240
Narrow Norm	171.1 ± 3.7
Narrow Mean	−0.000702 ± 0.003574
Narrow Sigma	0.19 ± 0.00
Wide Norm	11.39 ± 0.56
Wide Mean	0.6778 ± 0.0360
Wide Sigma	1.092 ± 0.027

slot 7, pad 30

σ≈170ps

Timing resolution photodetector limited

140MHz background

Overshoot/ringing

Using external RF Amplifier System (~43dB gain)

(close neighbor in hit plane)

deltaT	
Integral	5960
χ² / ndf	291.7 / 78
Narrow Norm	370.8 ± 6.6
Narrow Mean	0.04636 ± 0.00447
Narrow Sigma	0.2749 ± 0.0037
Wide Norm	17.27 ± 1.02
Wide Mean	1.313 ± 0.061
Wide Sigma	−0.9753 ± 0.0355

slot 6, pad 61

σ≈275ps
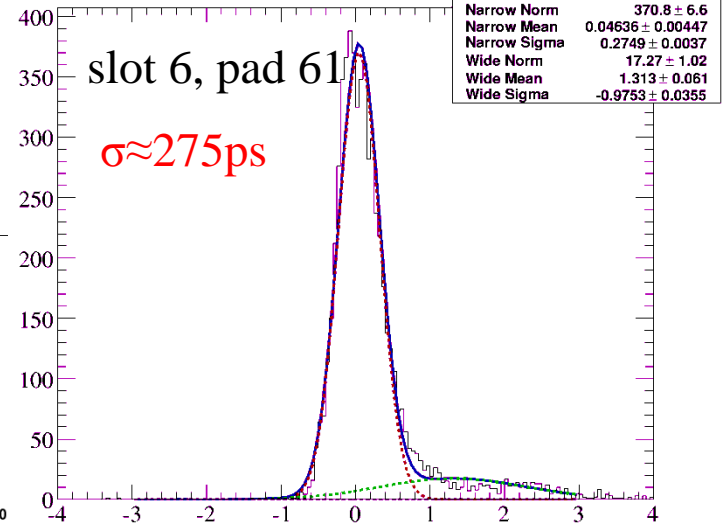
delta(time) (ns)

Simulated Performance vs. SNR

300MHz ABW, 5.9GSa/s

Time Difference Dependence on Signal-Noise Ratio (SNR)

$$\sqrt{kTZ\Delta\nu}$$

G. Varner -- Deeper Fast Waveform Sampling -- picoSecond WS in Krakow
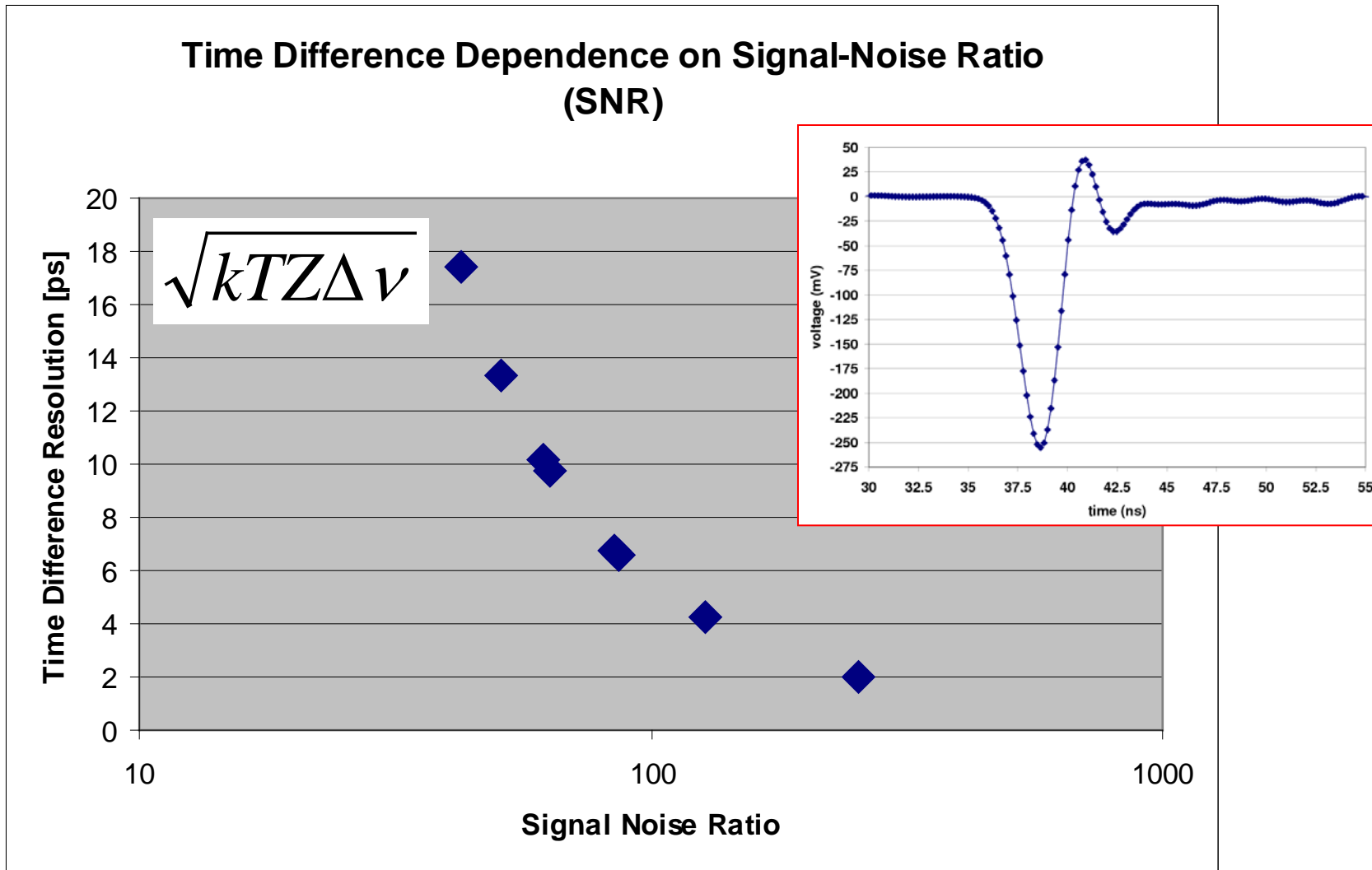
IRS Input Coupling
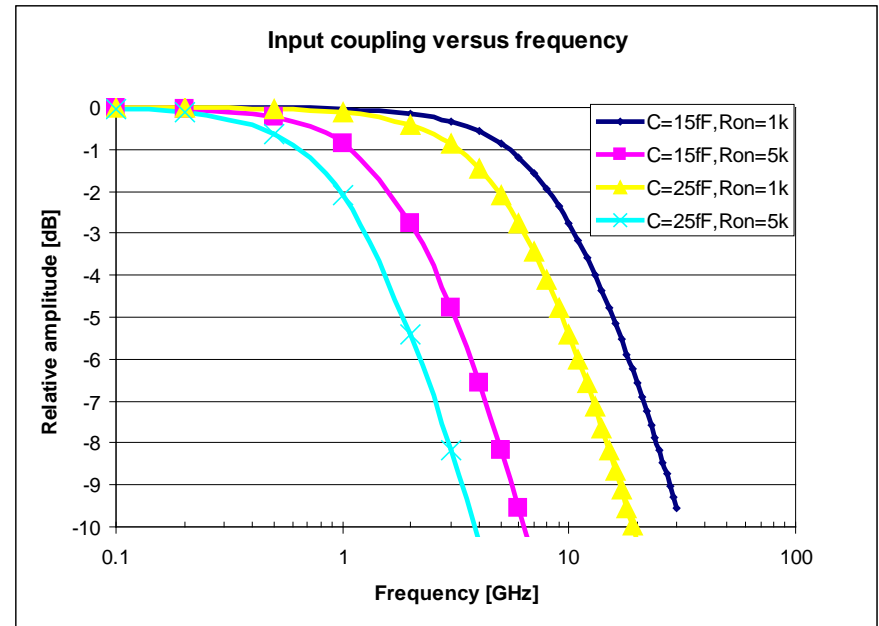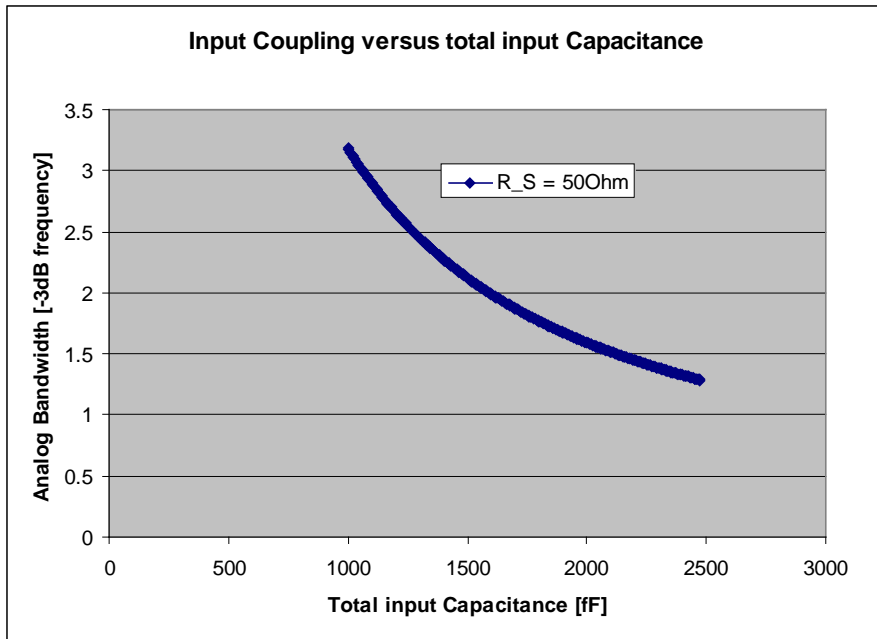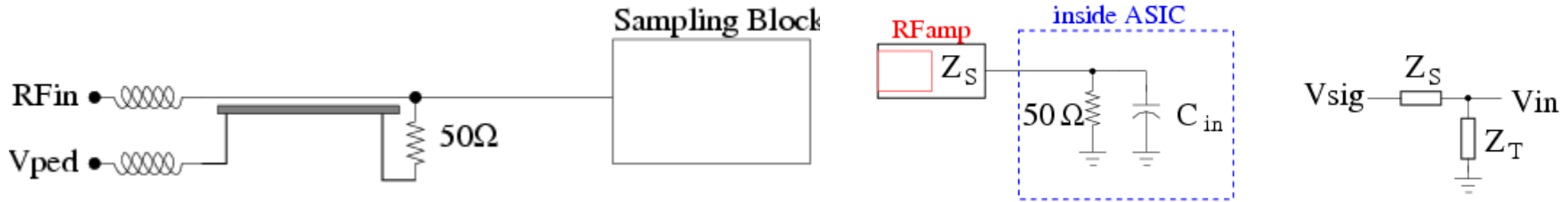
- ## Input bandwidth depends on 2x terms
  - $f3dB[input] = [2*\pi*Z*C_{tot}]^{-1}$

  - $f3dB[storage] = [2*\pi*R_{on}*C_{store}]^{-1}$

Founding WFS ASIC References

- ## PSI activities (DRS)
  - IEEE/NSS 2008, TIPP09
  - http://midas.psi.ch/drs

- ## DAPNIA activities
  - MATDAQ: *IEEE TNS 52-6:2853-2860,2005 / Patent WO022315*
  - SAM; *NIM **A567** (2006) 21-26.*

- ## Hawaii activities
  - STRAW: Proc. SPIE 4858-31, 2003.
  - PRO: JINST, Vol. **3**, P12003 (2008).
  - LABRADOR: NIM **A583** (2007) 447-460.
  - BLAB: NIM **A591** (2008) 534-545; NIM **A602** (2009) 438-445.
  - STURM: EPAC08-TUOCM02, June, 2008.

SAMPIC0: a Waveform based TDC chip

SAMPIC0 : a 16 channel WTDC

- proof of concept chip **already usable with detectors**
- Test of CMOS **AMS0.18µm** (**low cost**, low leakage, 1.8V technology)
- Compatible with buffered architecture (deatime free) => future chips

Each channel Self-Triggerable to catch parameters of fast pulses:

- **Timing :**
  - Coarse = timestamp counter
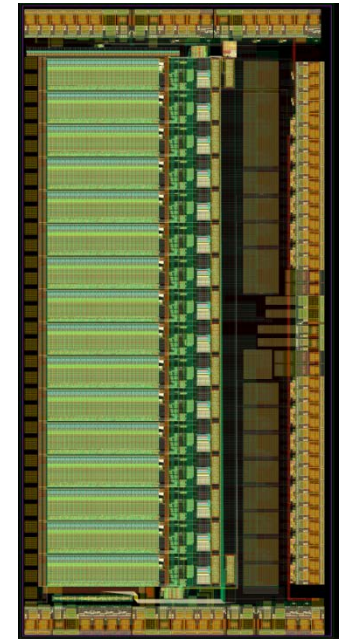 - Middle = DLL based TDC *also defining a Zone of Interest for sampling*
  - Fine = few samples in the ZOI of the sampled waveform
- **Waveform Shape, Charge, Amplitude** available through samples
- **No need for high-end discriminator** => low power, versatility
- **Short SCA** (to accommodate the delay of the discriminator)
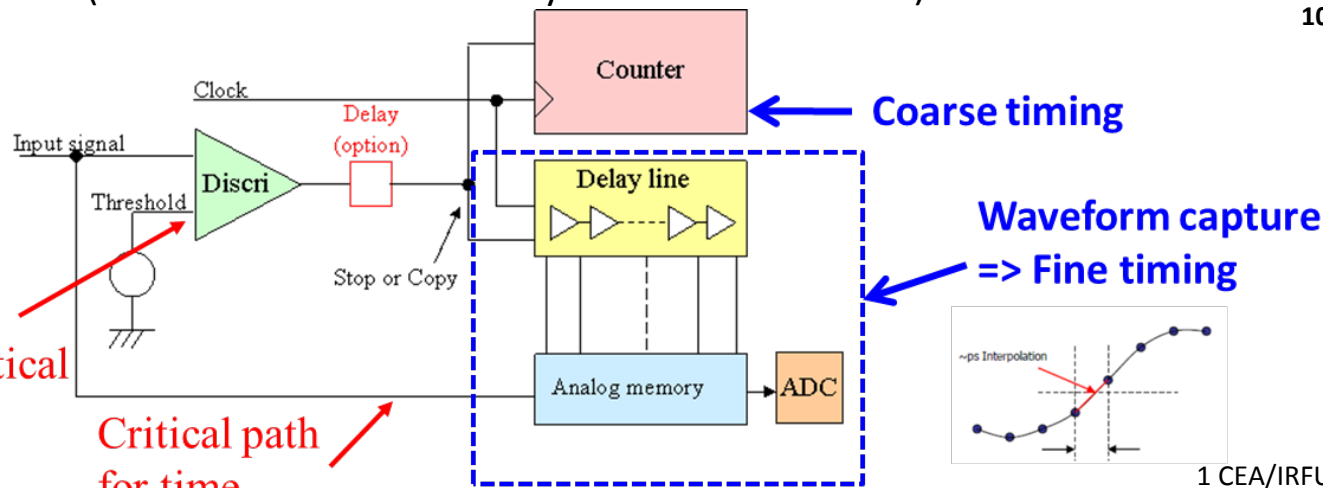
AMS CMOS 0.18µm
10 mm²

- H. Grabas[1]
- E. Delagnes[1]
- D. Breton[2]
- J. Maalmi[2]

Coarse timing

Waveform capture
=> Fine timing

No more critical
For timing

Critical path
for time
measurement
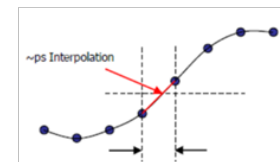
1 CEA/IRFU/SEDI Saclay
2 CNRS/IN2P3/LAL Orsay

SAMPIC0 Architecture

- Common "Slow" (160MHz) 12-bit Gray Counter = **Coarse Timestamping/ch**

- **Common Timing generator**: servo-controlled DLL: (1-10 GHz) used for **middle precision timing** & analog sampling commands

- 16 (short) SCA self-triggerable channels:
  - No analog input buffer
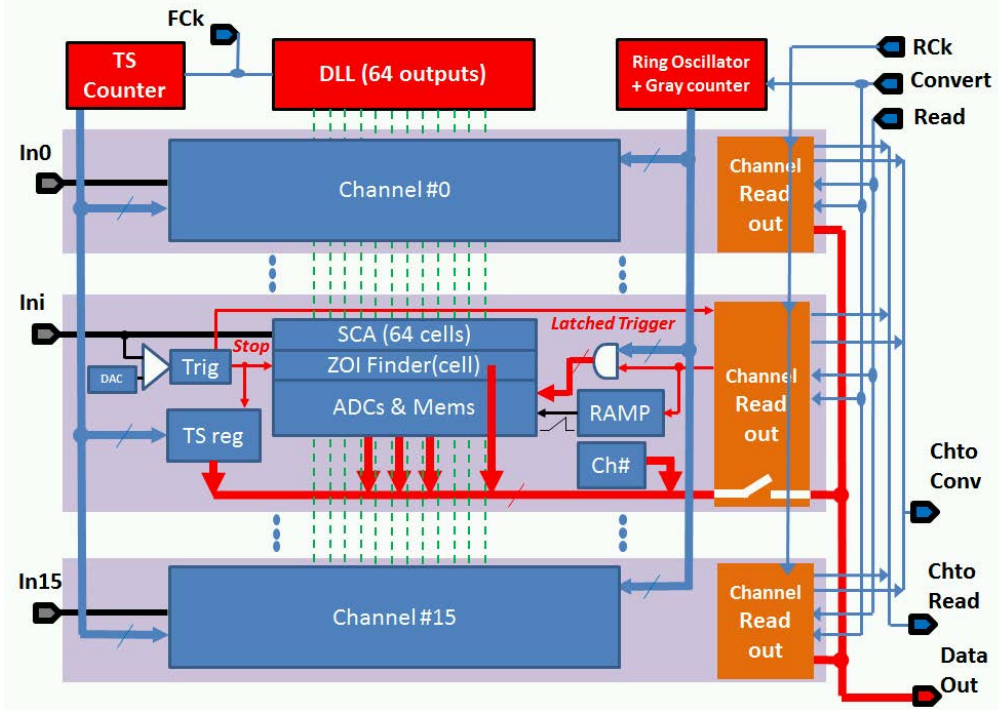 - 64 cells, ~ 50fF capacitor
  - 1.5 GHz Bandwidth

- Several modes of triggering: discri on threshold (+/-), External, Or...

- On-chip fast Wilkinson digitization :
  - 1.3 GHz common gray counter.
  - tunable ramp slope=> trade-off conversion time/precision 1.6μs/11bit to 200ns/8bit
 - Simultaneous conversion of all the SCA cells of the triggered channels

- **Deadtime** = only for triggered channels waiting or in conversion *=> independent DEADTIME* (can be common if required)

- Read-Out through a 12 bit/160 MHz (up to 400) LVDS bus: negligible readout deadtime

- SPI for configuration (Trigger modes, discriminator thresholds (1/ch),...)

55

Cascaded Switched Capacitor Array

- 32 fast sampling cells (10 GSPS)

- 100 ps sample time, 3.1 ns hold time

- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)

- Shift register gets clocked by inverter chain from fast sampling stage

input

shift register

fast sampling stage

secondary sampling stage
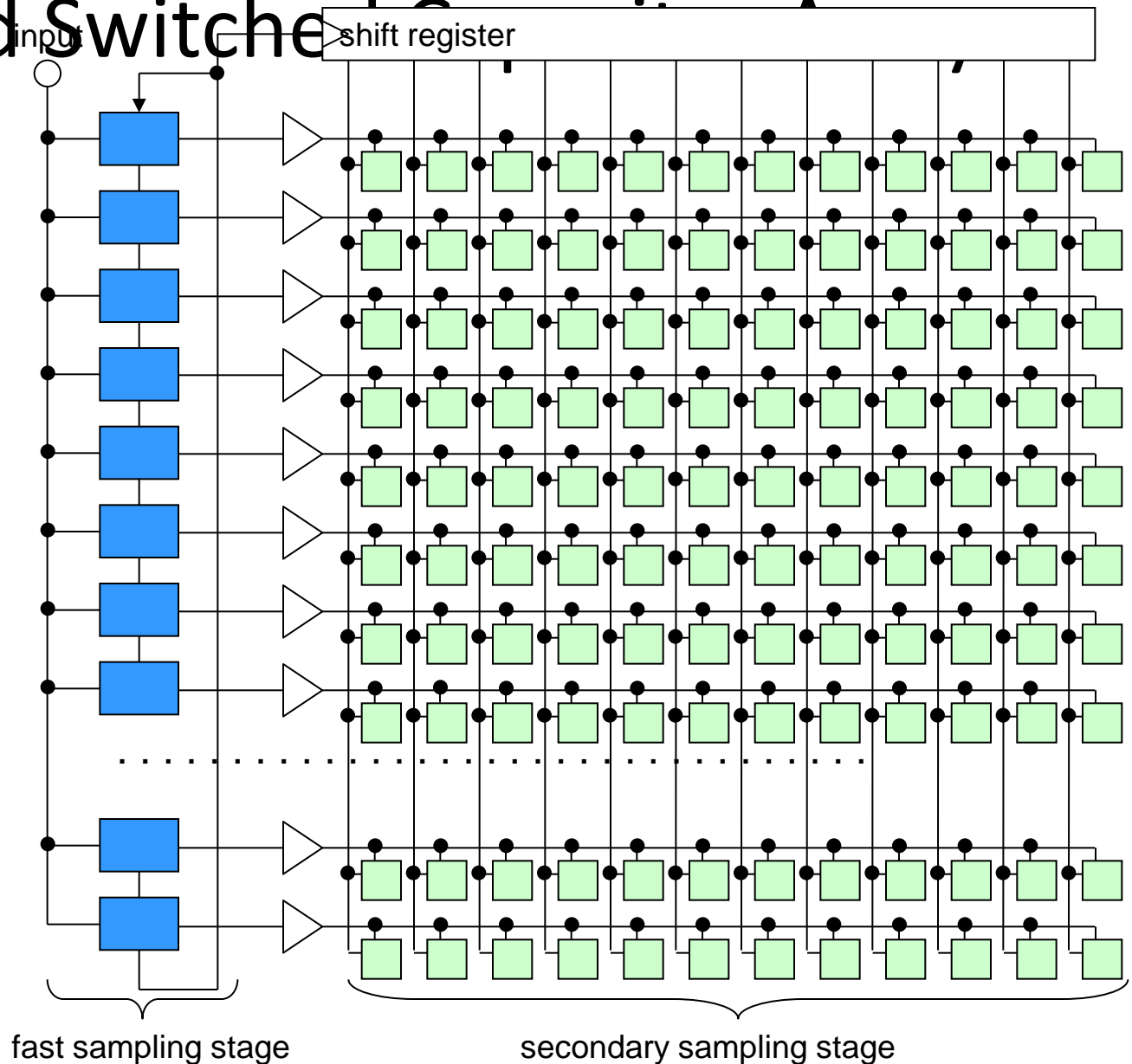
FIFO-type analog sampler

digitization

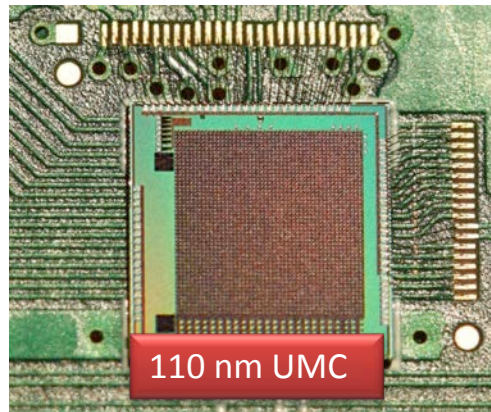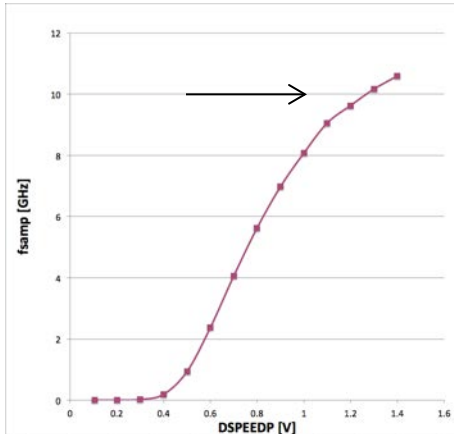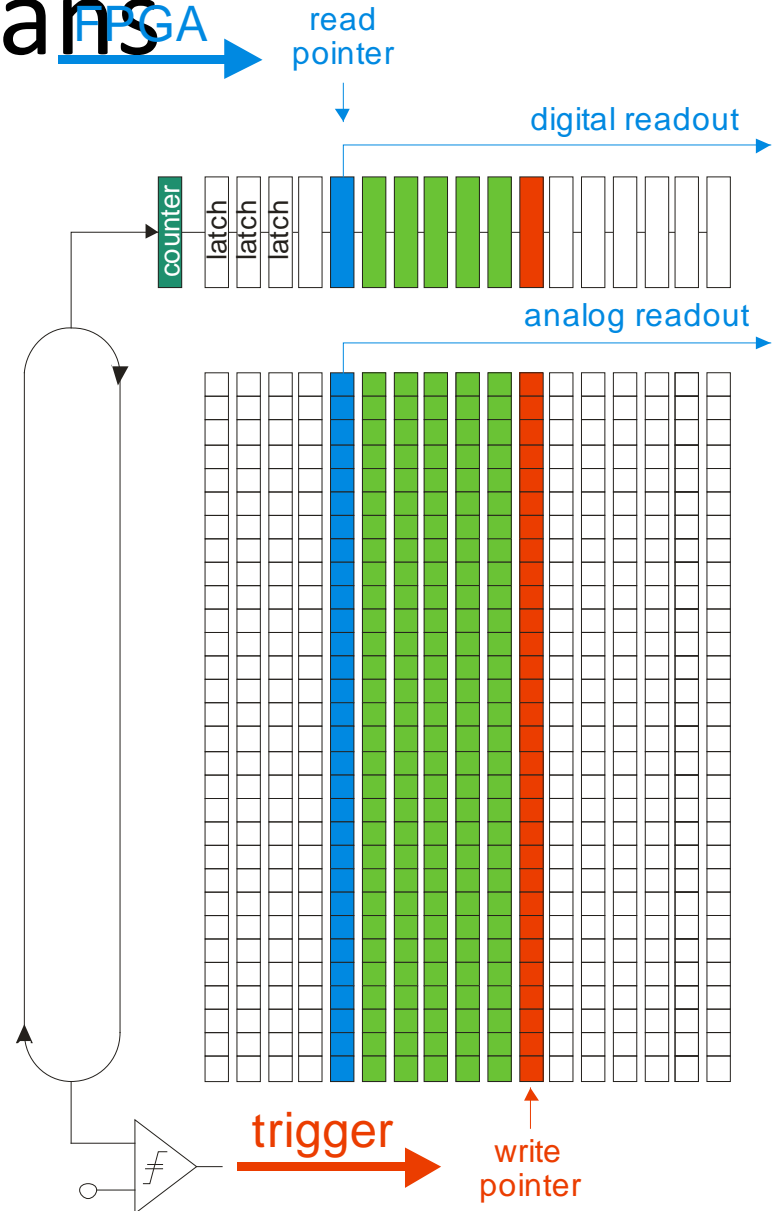**DRS Readout (1.024 GSPS)**

ADC value / Time [ns]
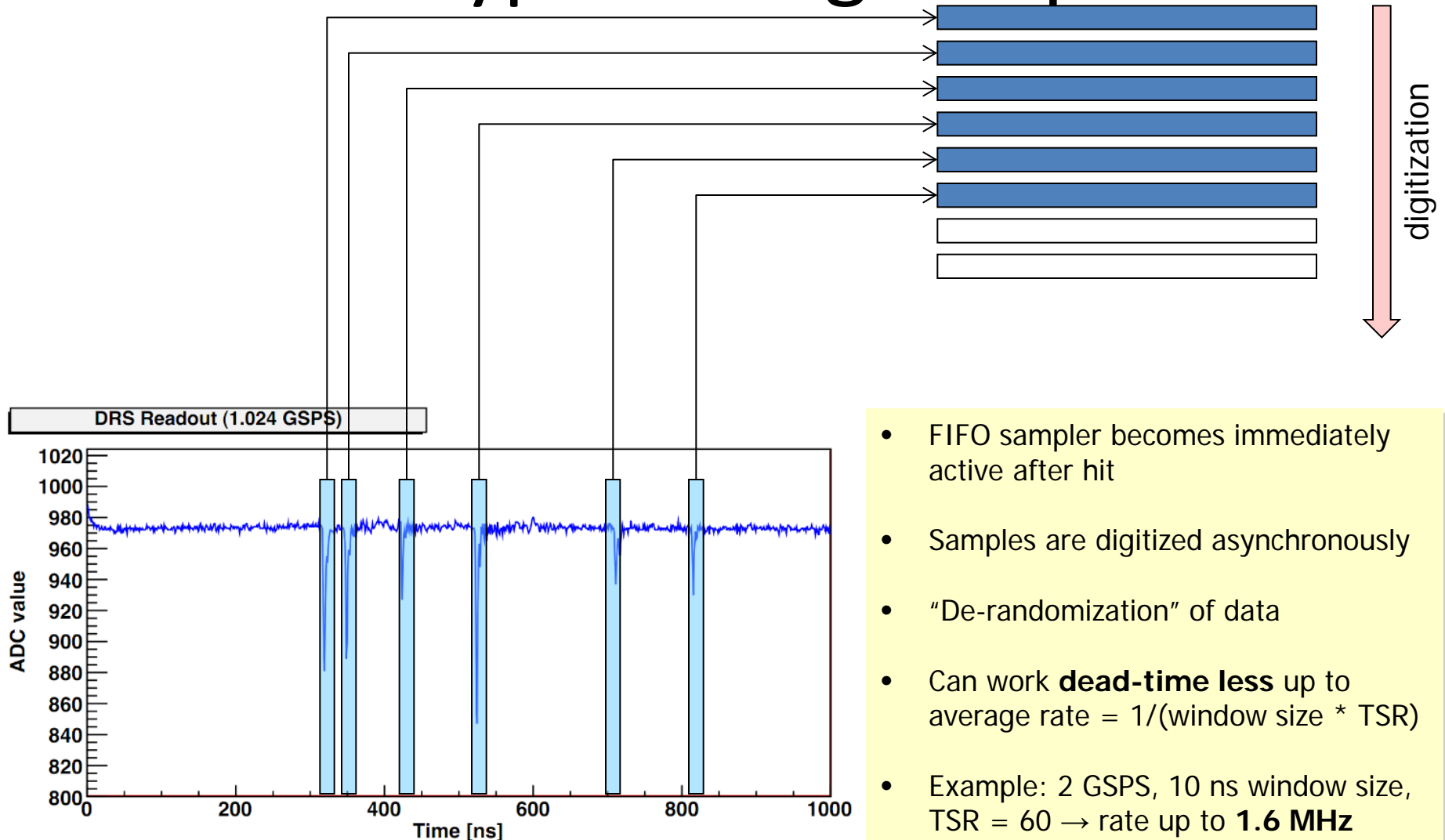
- FIFO sampler becomes immediately active after hit

- Samples are digitized asynchronously

- "De-randomization" of data

- Can work **dead-time less** up to average rate = 1/(window size * TSR)

- Example: 2 GSPS, 10 ns window size, TSR = 60 → rate up to **1.6 MHz**

DRSF Plans

- Self-trigger writing of 128 short 32-bin segments (4096 bins total, 3 GHz analog bandwidth)

- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger

- Attractive replacement for CFG+TDC

- First tests: > 10 GSPS @ 4 mA, first full version planned for 2014

FPGA

read pointer

digital readout

counter | latch | latch | latch

analog readout
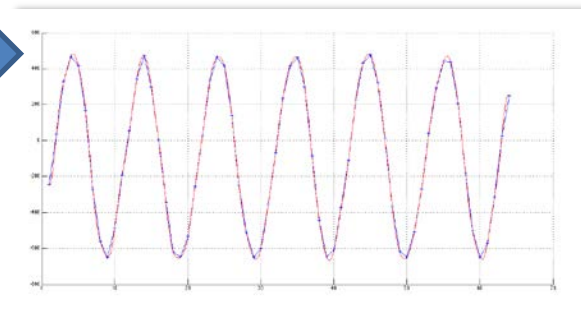
110 nm UMC

trigger

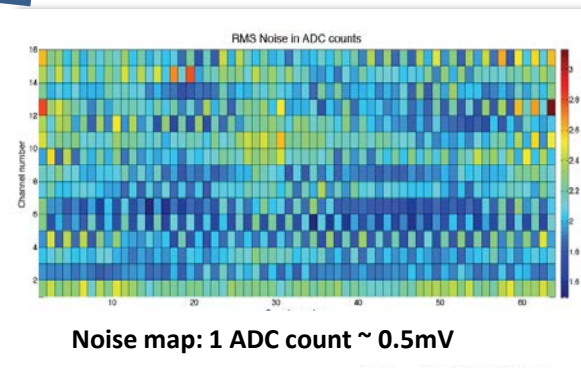write pointer

Very first measurement results

- Performed with a 16-channel mezzanine-board compatible with the system (USB/Eth/optical) previously developed for the SAMLONG chips
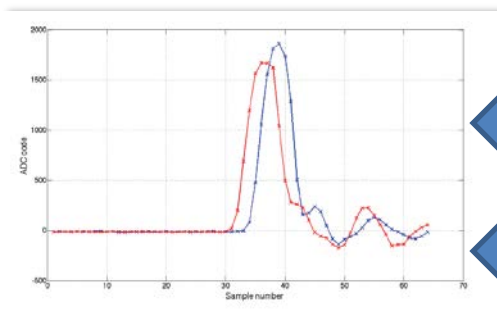- **Already usable for small/experiments or detector tests**

800ps FWHM pulses, self triggered & sampled @ 6.4 GSPS

- 180mW power consumption
- **Sampling 3.2GSPS- 8.4 GSPS OK for the 16 channels, and up to 10.2 GSPS for the 8 first channels**
- **Discriminator able to trigger on pulses with FWHM < 800ps**
- **Discriminator noise < 2mV RMS**
- **SCA noise < 1.3mV RMS in 11-bit mode (1.6mV in 9-bit)**
- **Range = 1V => 9.6 bit RMS**
- **Gain spread between cells = 0.7% RMS, INL = 3% pp.**
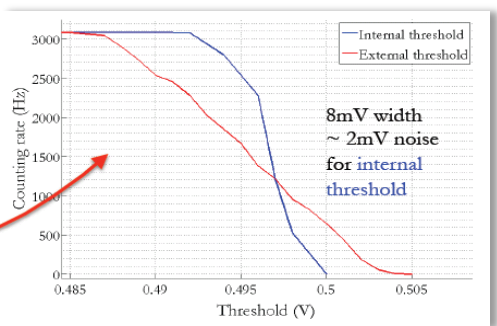- **1.6 GHZ SCA Bandwidth (uniform on all cells/all channels)**

8mV width ~ 2mV noise for internal threshold

Discriminator S-Curve , internal & external threshold, 3kHz rate

1 GHz, 0.5pp sinewave @ 10.2 GSPS (only pedestal corrections). All the 64 samples are usable.
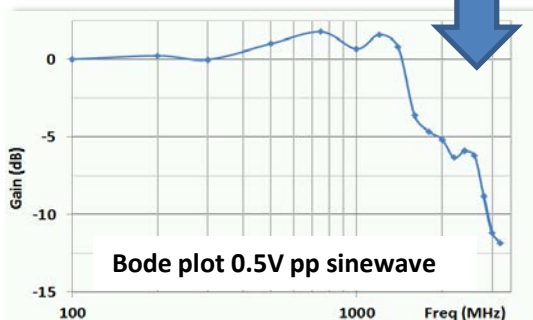
Bode plot 0.5V pp sinewave

Noise map: 1 ADC count ~ 0.5mV

SAMPIC0: Summary
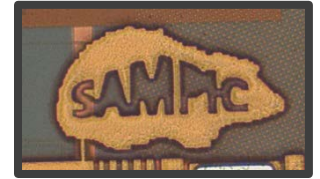
		Unit
Technology	AMS CMOS 0.18μm	
Number of channels	16	
Power consumption	180 (1.8V supply)	mW
Discriminator noise	2	mV RMS
SCA depth	64	Cells
Sampling Speed	<3-8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (Unipolar)	1	V
ADC resolution	8 to 11 (trade-off time/resolution)	bit
SCA noise	<1.3	mV RMS
Dynamic range	9.6	Bit RMS
Conversion time	0.2-1.6 (8bit-11bit)	μs
Readout time (can be probably be doubled)	25 + 6.2/sample	ns
Time precision before correction	15	pS RMS
Time precision after timing INL correction	< 5	pS RMS