Status of the System Test at UZH

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CERN

UZH Lab

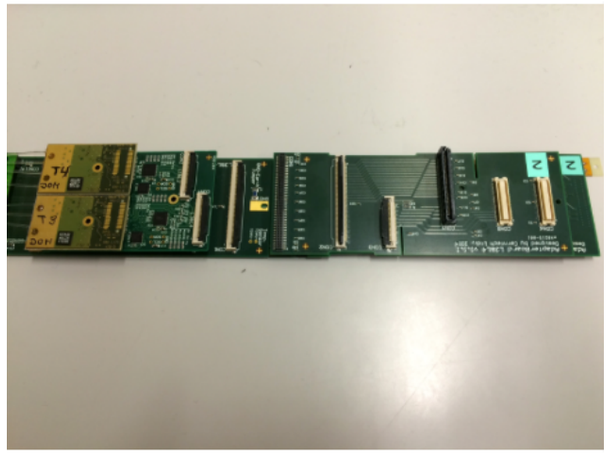
Table-top system including all components of one BPix sector

VME crate

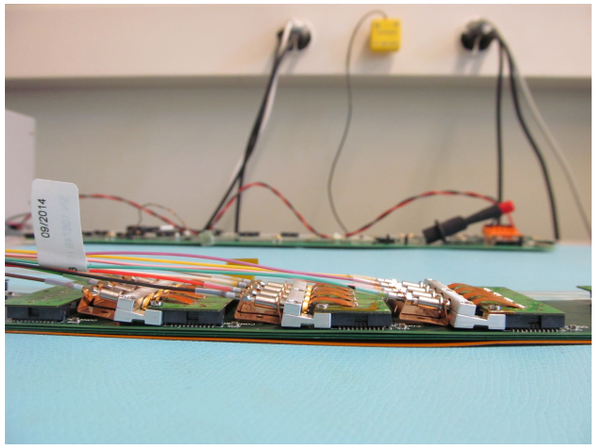
CCU ring

DCDC board

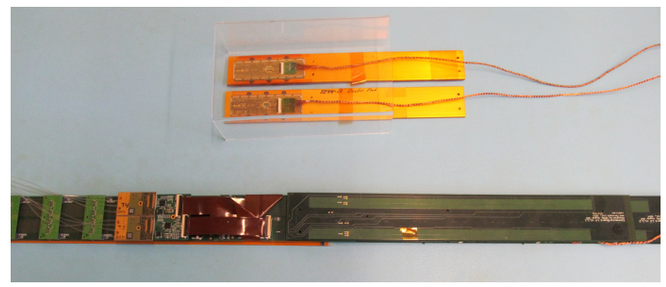
DOH MB



POHs

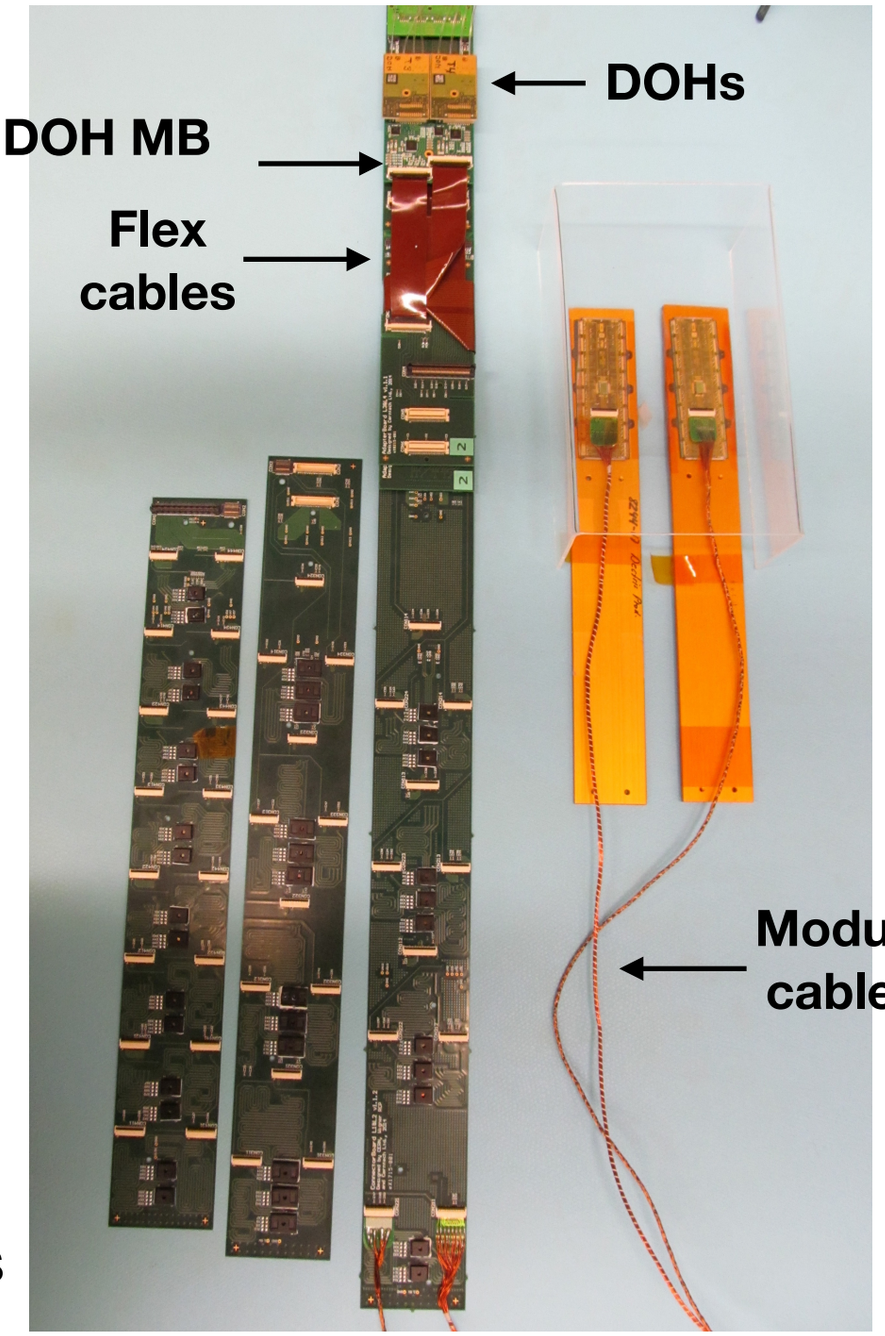


Adapter and connector boards with two modules



System test at UZH

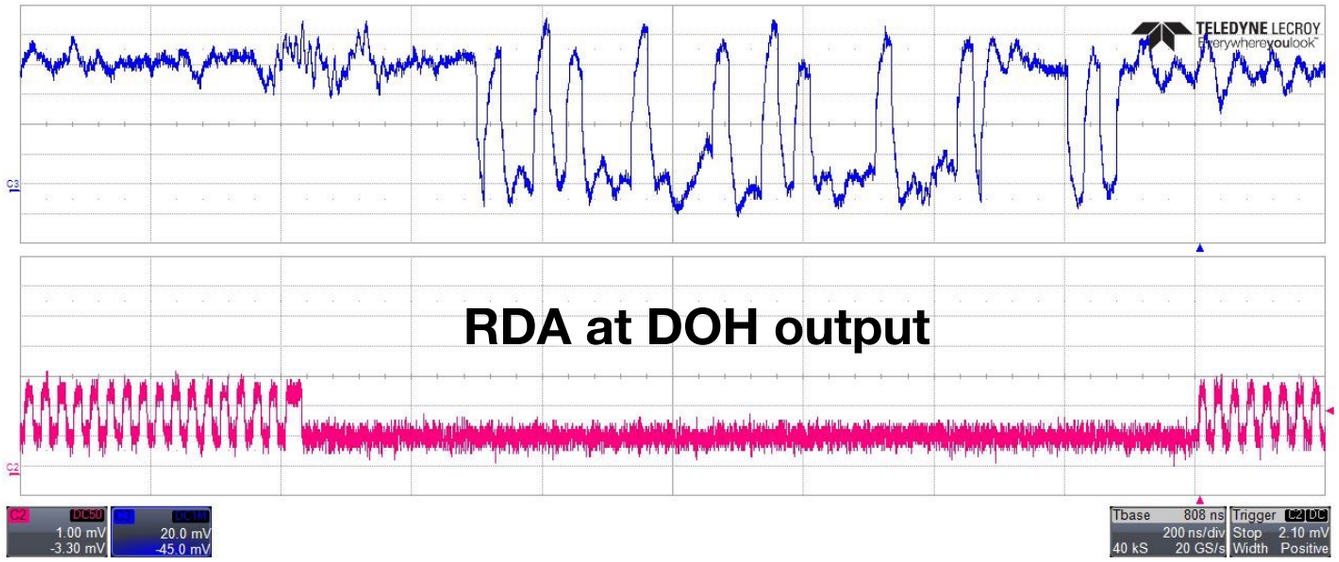
- Latest status report at [Phase I Pixel Upgrade Workshop] in Visegrad
- Verified slow control and measured slow I^2C signal quality on POH connectors
- Verified fast I^2C signal transmission
  - problem with Gatekeeper RESET polarity inverted on DOH MB: Gatekeeper always open
  - fixed by removing soldering connection
- Performed POH bias scan with analog VME FED
- Verified module programming and measured clock, CTR and fast I^2C signals
  - after DOH MB at the end of flex cables
  - after connector boards at the end of module cable
  - on the module HDI test pad
- Verified module readout and measured module signals

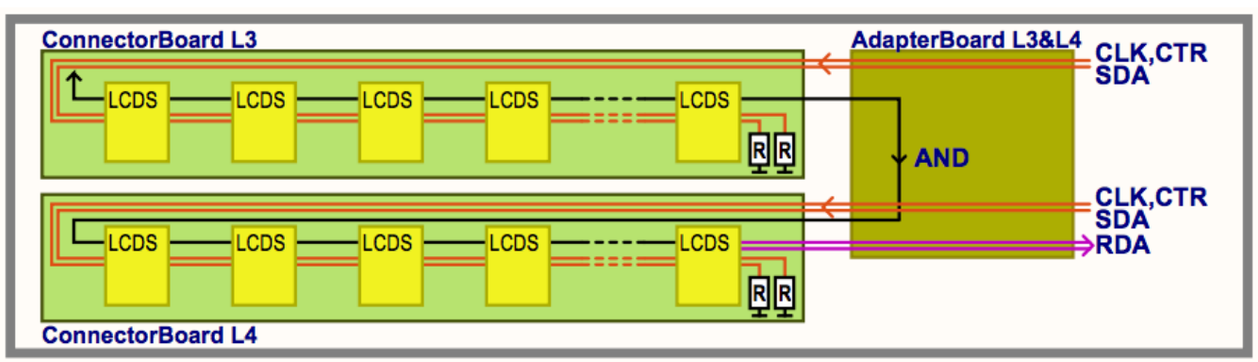


RDA signal

- Investigated issue with the RDA
- When sending programming signals (SDA) the return data signal (RDA) from the module is not visible at the DOH output
  - only idle pattern interrupted when the SDA is sent

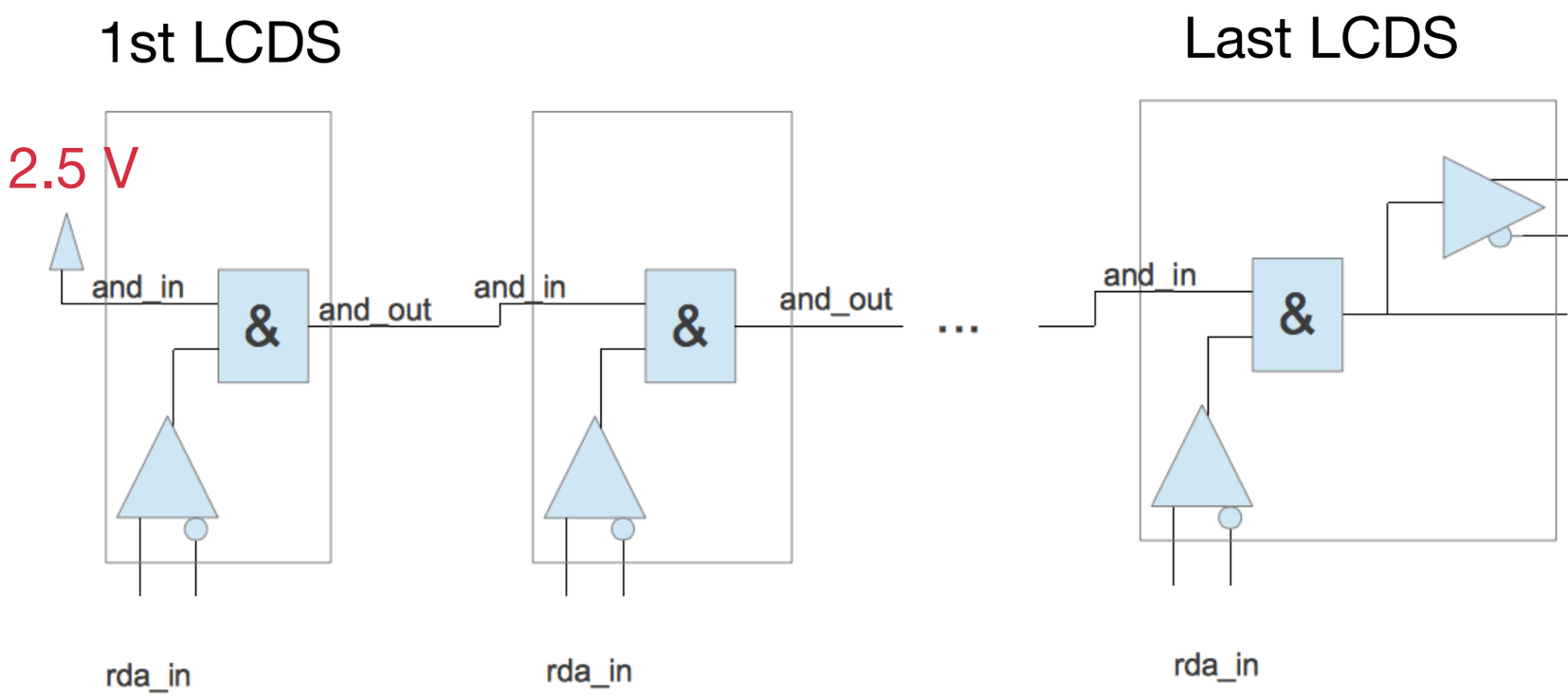
RDA on module connector on module





RDA signal

At each LCDS: and_out = rda_in & and_in

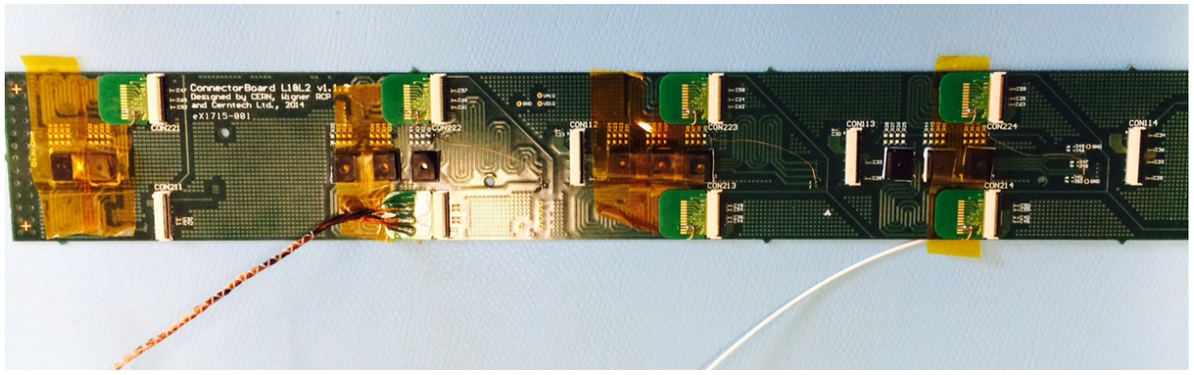


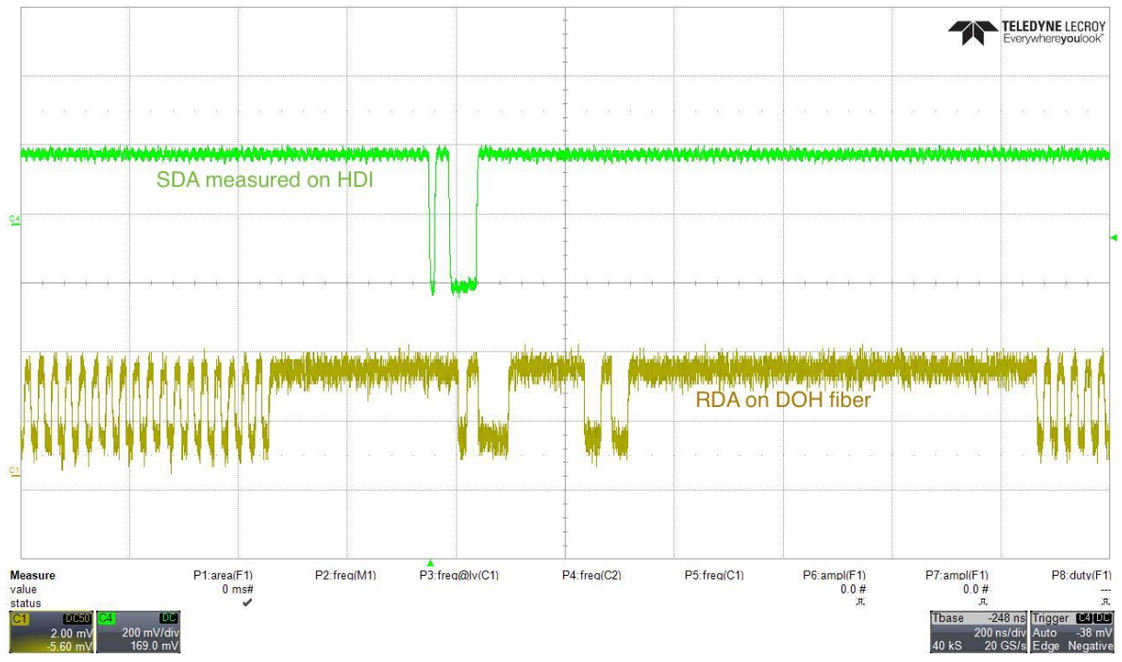
- Measured and_in/out signals at each LCDS of L12 connector board
- Found that some of the connectors have rda_in = 0

  ⇒ and_out = 0 ⇒ rda_out = 0

RDA signal

- Soldered pull-up resistors (1.5 kOhm) on module cable prints to pull up the rda_in line for L2 connectors
- Soldered resistors directly on the board for the L1 connectors (prints not yet available)
- With these modifications, successfully verified the RDA signal at the DOH output





- The connected modules in the final system will automatically pull up the rda_in
  - issues for sectors where not all the module connectors are used

Conclusions and plans

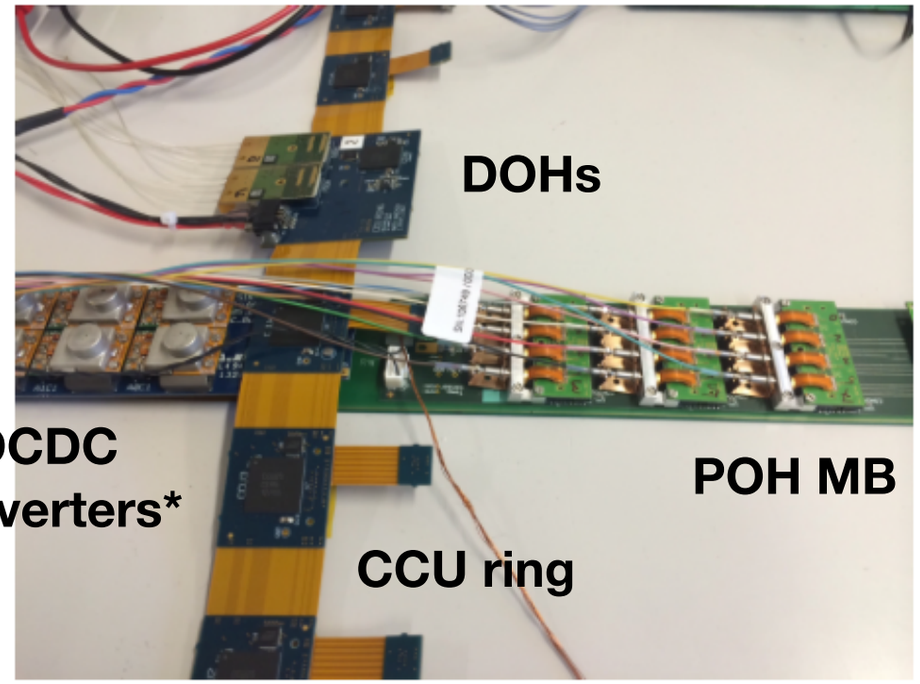
- We integrated a full upgrade BPix sector at UZH and it is ready for testing the complete upgrade system
  - included all electronic boards and two modules
  - all final components included but mechanically different wrt final system
- Achievements:
  - verified slow control, module programming and readout chains
  - measured slow and fast I^2C signals, and module digital signals
  - established routines for module operation
- Plans:
  - complete the testing of module connectors on each connector board
  - develop procedure to measure optical signal quality
  - implement software for digital VME FED operation
  - implement routines to automatize the supply tube testing procedure

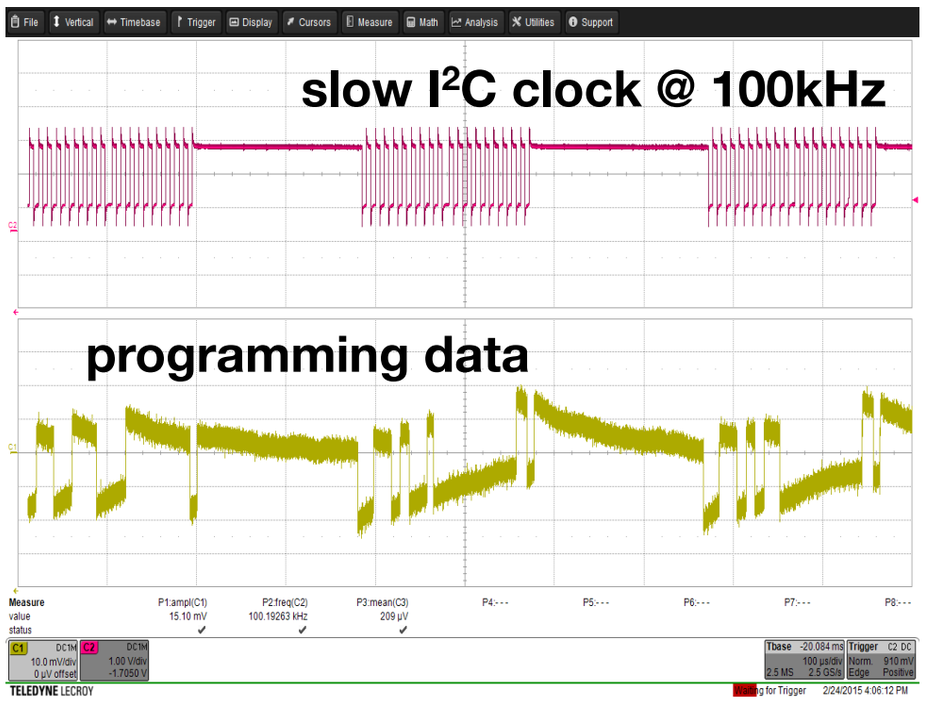
Backup Slides

Slow control

- CCU ring with 8+1 CCUs (Aachen) connected to TrackerFEC through 2 DOHs
  - successfully tested: FEC-CCU ring architecture, redundancy scheme, I^2C communication to DOHs, functionality and control of DCDC converters
- One CCU connected to POH MB
  - measured slow I^2C signal quality on different POH connectors
  - successfully tested slow I^2C speed and POHs programming
- DOH MB mounted on POH MB and equipped with two DOHs (L12 and L34) connected to pxFEC
- Successfully tested DOHs, Delay25 and PLL chips programming through slow I^2C

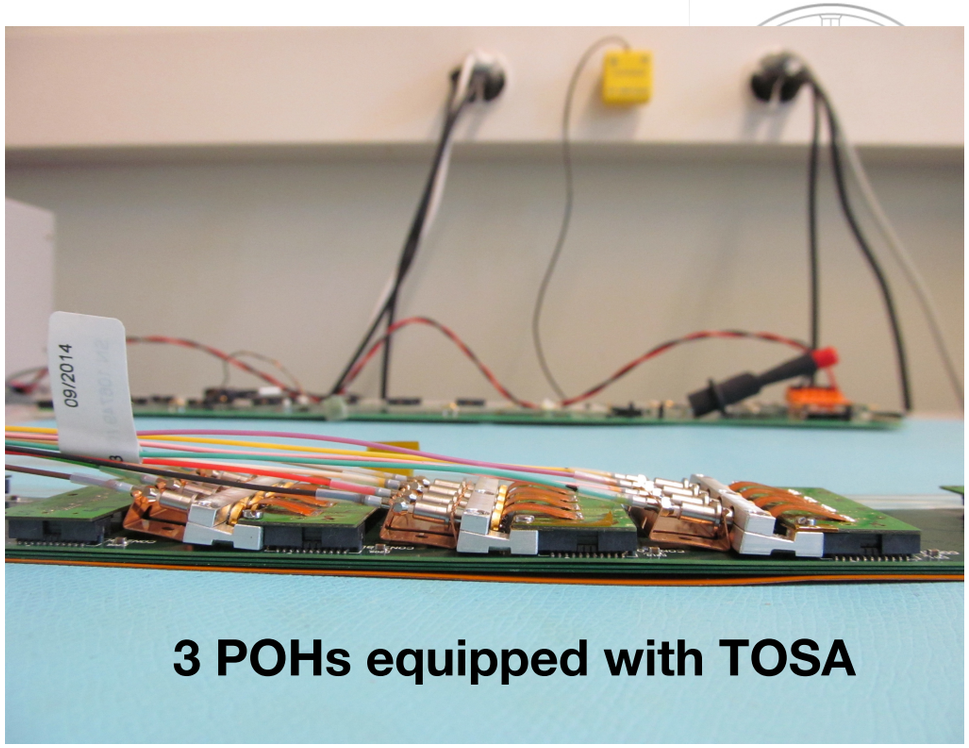
* DCDC converters → Deborah's talk

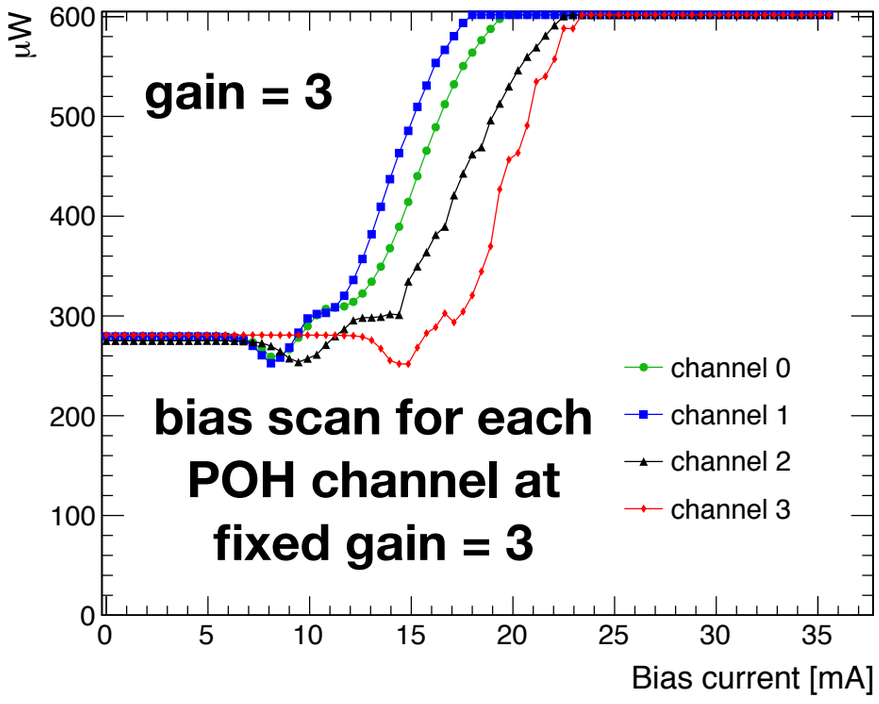


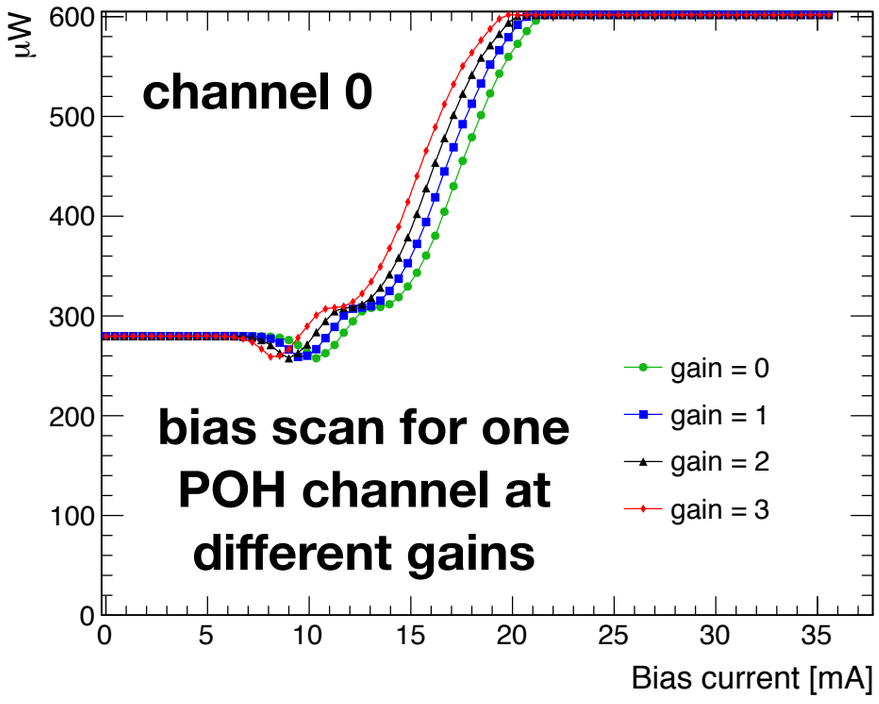


Optical readout

- Module digital signals transmitted through flex cables to POH MB and readout as optical signals at the POH fibers
- POHs gain and bias registers have to be initialized to proper values for module readout
- Used analog VME FED to perform the bias scan of each POH channel





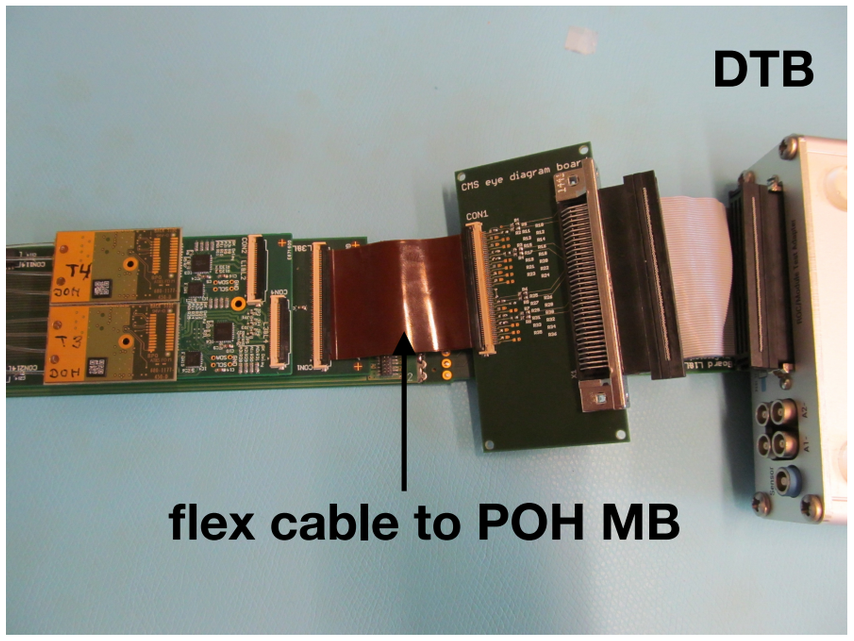


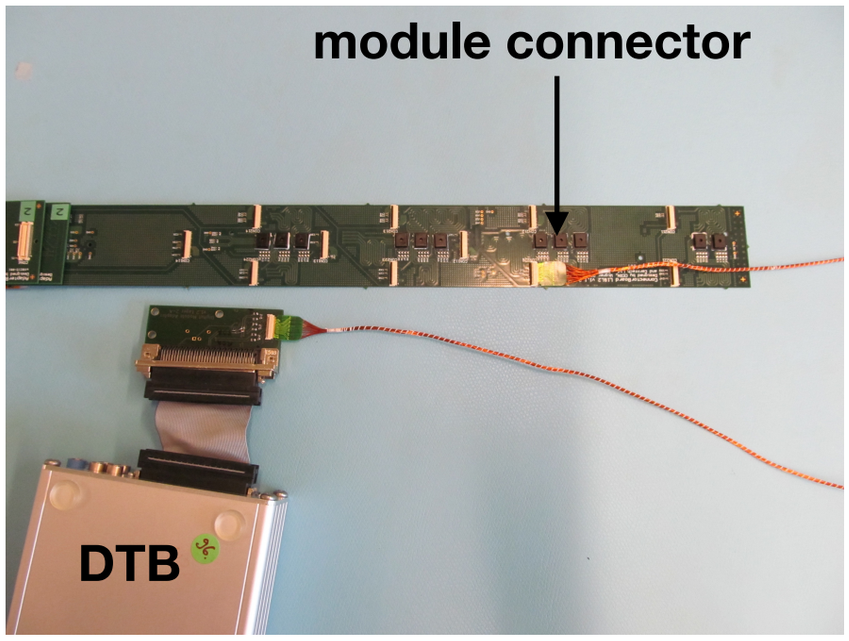
FED receiver conversion:
1.7uW/ADC
4.5 mA/10 bias units

Module readout (I)

- Verified readout chain injecting random data with Digital Test Board directly into POH MB and into connector boards
- verified complete connector to POH channel mapping for all 4 layers
  - module assignment in the readout does not match the I^2C addressing
- transmitted signal not visible for some of the connectors on L4 connector board → still need to investigate
- Plans to use this setup to measure the quality of the transmission line (eye diagrams)

POH	module readout	i2c addressing	POH	module readout	i2c addressing
1	L1		8	L4	
2	L2		9	L1	
3	L4		10	L3	
4	L1	0x11	11	L4	0x13
5	L4		12	L2	
6	L2		13	L3	
7	L2		14	L3	

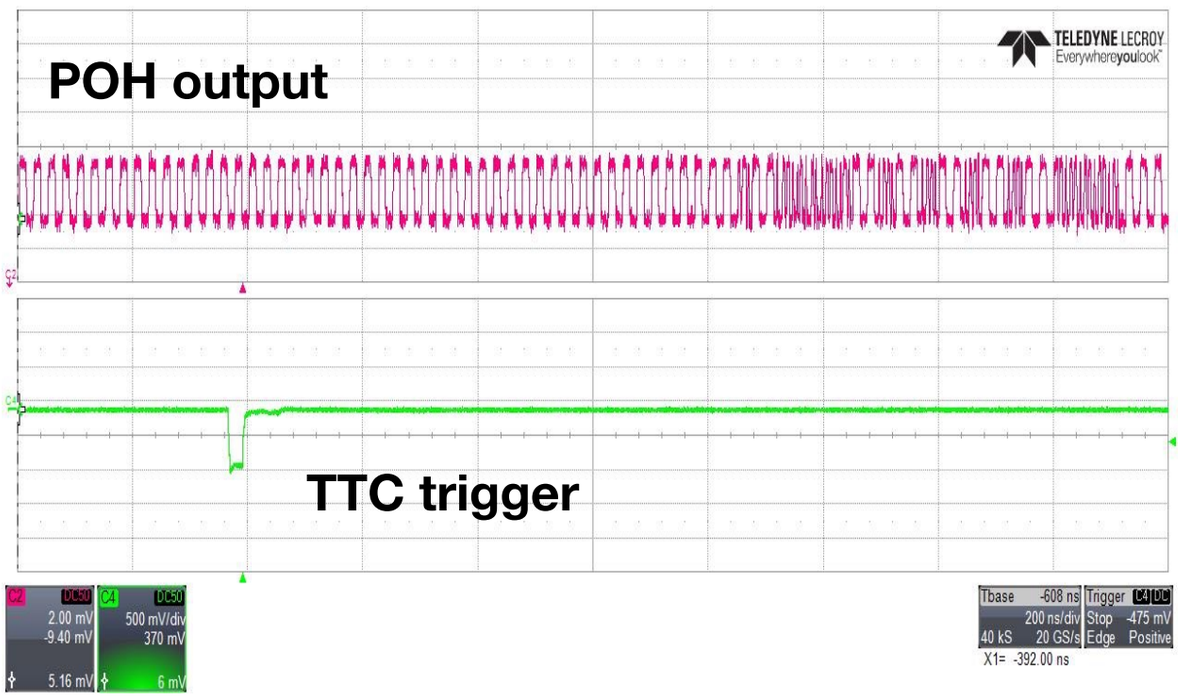




Module readout (II)

- Verified module digital output signals for different connectors of different layers
  - 40MHz idle pattern without trigger
  - TBM trailer and header + ROC headers when sending triggers

TBM trailer and header + ROC headers



TBM trailer (ROCs disabled)