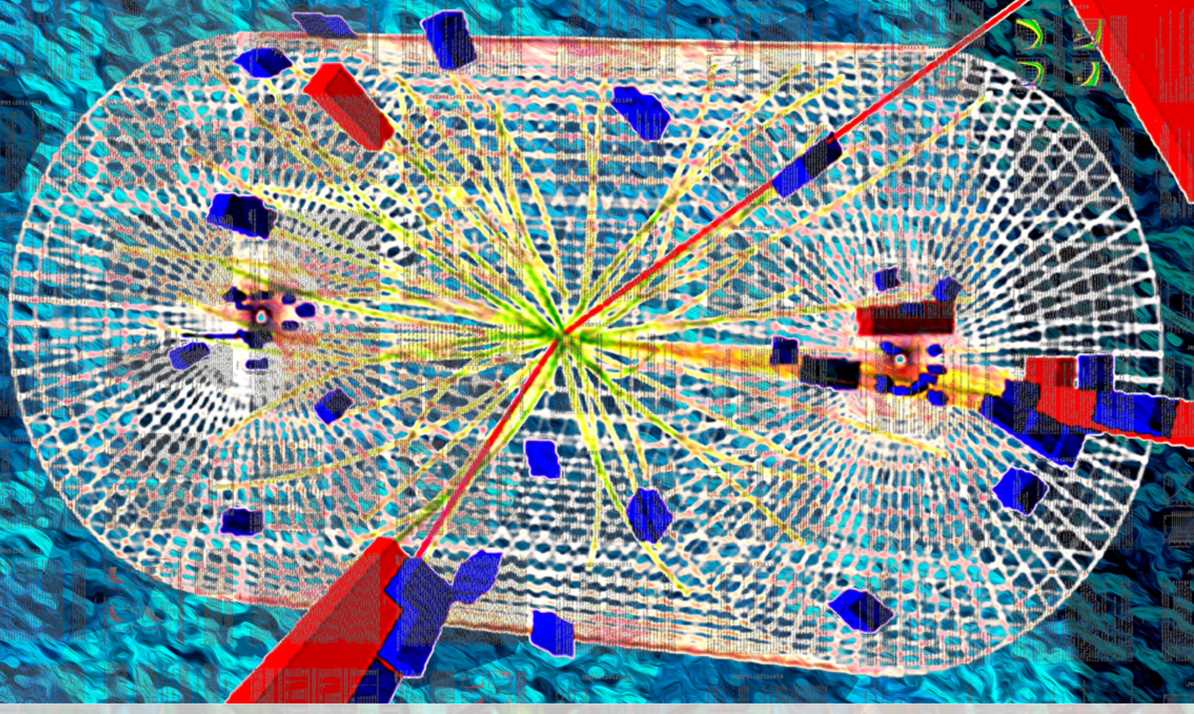

Hardware Demonstrator of a L1 Track Finding Algorithm with FPGAs for the Phase II CMS Experiment

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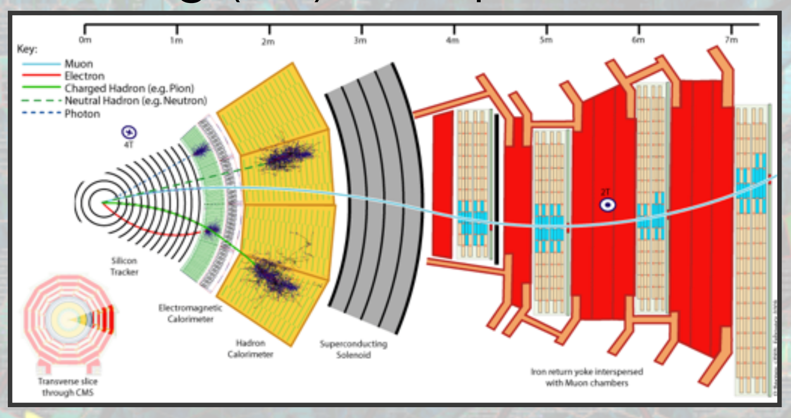
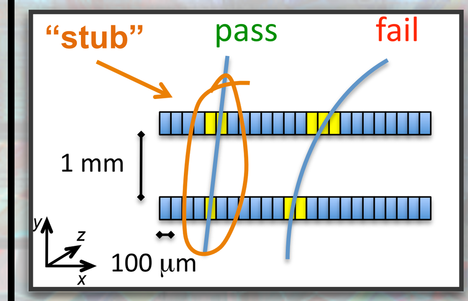
The CMS Phase II Upgrade

In the next decade the Large Hadron Collider (LHC) will undergo a series of upgrade in order to increase the instantaneous luminosity up to 5~7 times the nominal value (**High Luminosity LHC**) [1]. At the HL-LHC proton bunches will cross each other every 25 ns, producing up to an average of 200 pile-up collisions per bunch crossing (BX). To operate in such an environment the CMS detector [2] will be upgraded (**CMS Phase II Upgrade**).

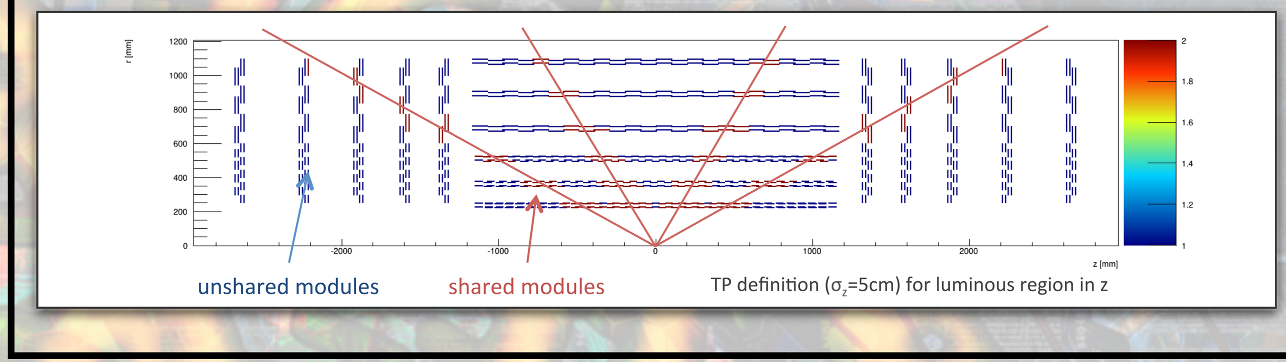


In particular for the first time the silicon tracker will be part used in the L1 Trigger (**Track Trigger**) [3].

The Track Trigger



The new CMS tracker will be composed of **double sensor modules** [4]. Each module will be able to reject low p_T tracks, measuring hit correlations in the two sensors. A pair of hits in a sensor doublet consistent with a high-p_T track is called **stub**. A possible architecture to handle tracker data makes use of **FPGA** boards, read out in a time multiplexed way [5].

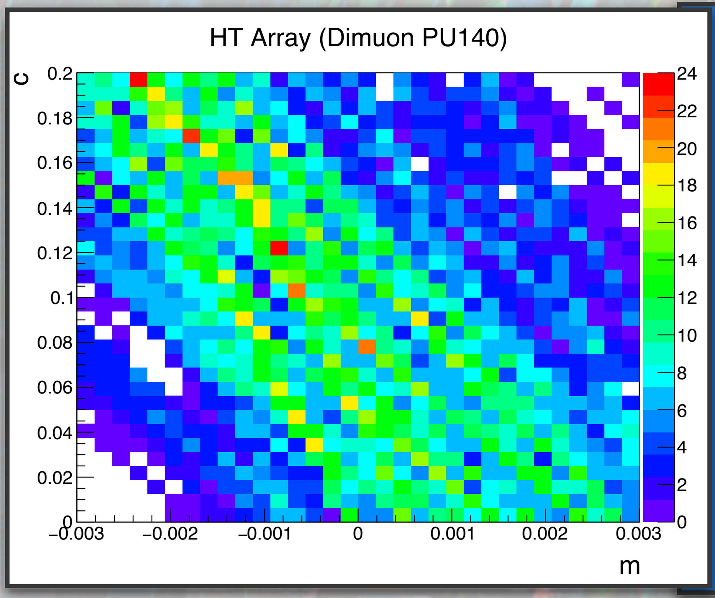


HT Basics

Straight lines considered in terms of slope-intercept parameters (m,c)

Point (x, y) –> Line (m,c)
Line (x, y) –> Point (m,c)

L1 Track Finding with Hough Transform

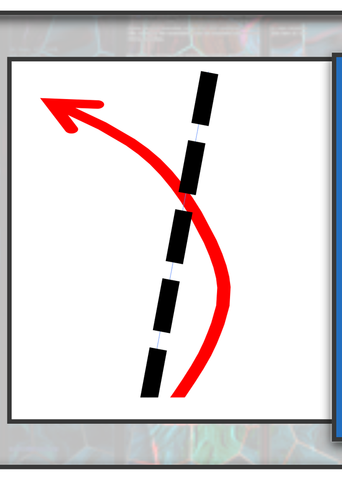


HT Parameters

Stub Parameter from detector
Φ, r (better resolution)
Track Parameters in HT
$m = q/p_T$, $c = \phi_0$
Hough Transform Equation
$$\phi(r) = \frac{cBr}{2} \cdot \frac{q}{p_T} + \phi_0$$
Valid for p_T > 3 GeV/c
Single ϕ_0 segment Array Content
~ 100 stubs & 90% occupied cells

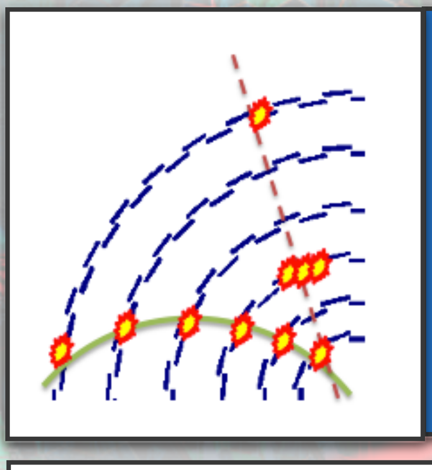
R-ϕ Hough Transform

The **Hough Transform** (HT) [6] is the method chosen to build track candidates. For ease of processing, the tracker has been divided into 5 trigger regions in pseudo-rapidity (Δη~1.0) and 36 regions along the estimated azimutal angle at the production point ϕ_0. **r,ϕ coordinates** of stubs are transformed into **slope m** and **intercept c** of lines from the vertex to the stub, and these filled into a 2-d histogram of m and c (see example on the left) A track is found when stubs cluster in the 2-d histogram.



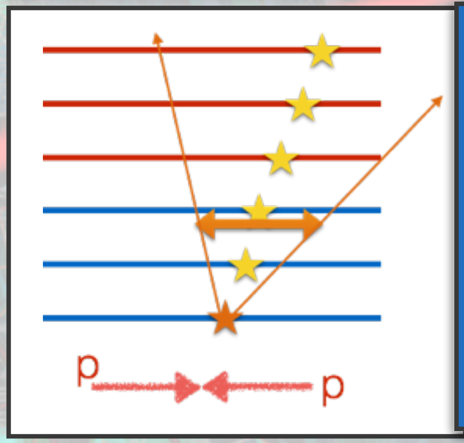
Bend Filter

Stubs are kept in a HT cell only if stub bend is consistent with predicted bend based on q/p_T of cell & (r,z) coords. of stub.



R Filter

- High p_T tracks should leave hits in all tracker layers
- Only cells with 5+ stubs belonging to 5+ tracker layers/ disks are marked for readout

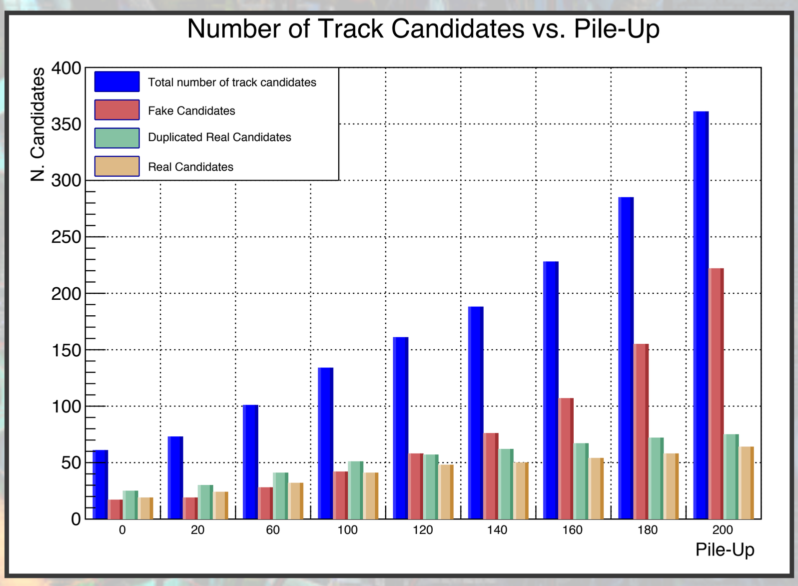


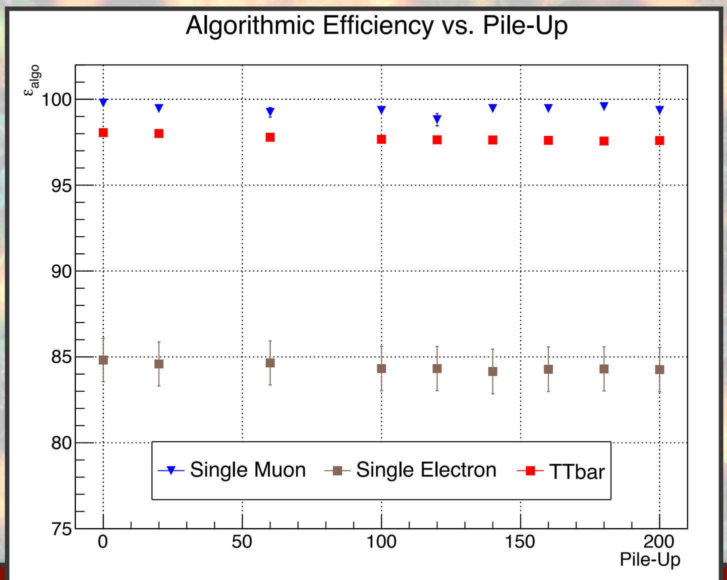
Z Filter

- Stubs in a HT cells should have the same value of Z_R (estimated value of Z at a radius of R)
- Stubs with a Z_R value far away from the cell average are discarded

Track Filtering

In most cases the stubs present in a HT cell are not consistent with real tracks. Indeed they are usually due to **random combinations** of hits belonging to pile-up tracks. In order to remove those fakes, several **filtering stages** are applied to each cell in the array.



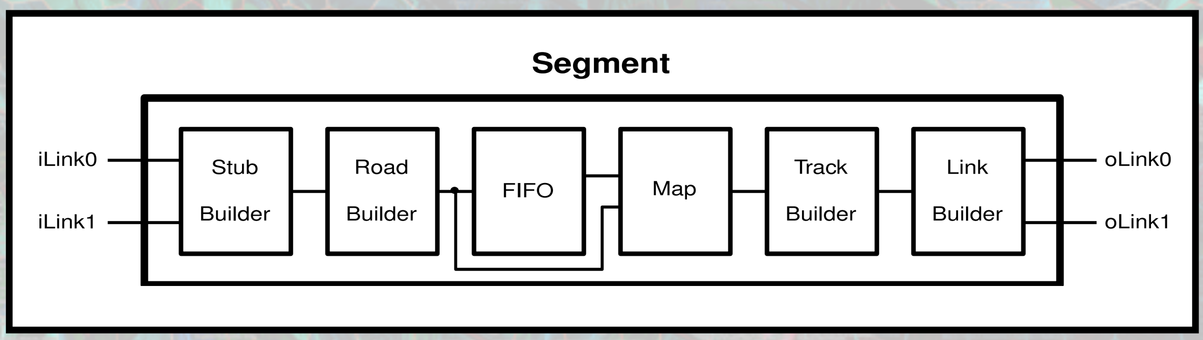


$$\varepsilon_{algo} = \frac{\text{charged signal tracks found by HT}}{\text{generated charged signal tracks passing filtering}}$$

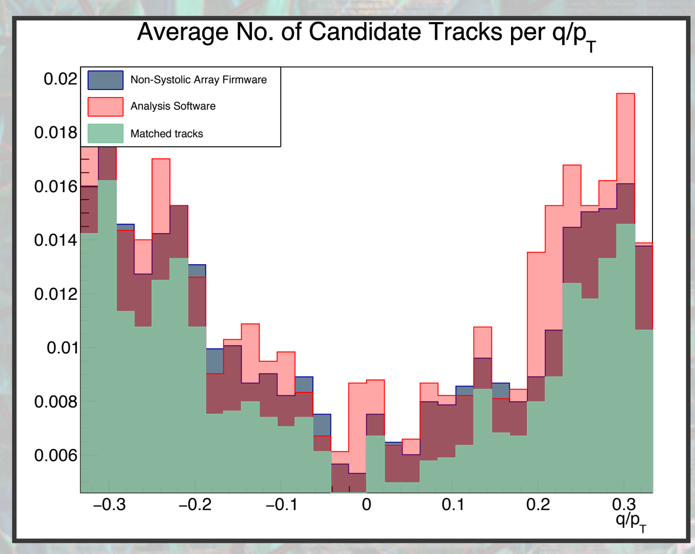
Results

Results show a generally good **algorithm efficiency (>97%)**, except that for electrons. This loss is mainly due to the Bremsstrahlung effect, which deviates the electron's trajectory.
The track filtering stages significantly reduce the number of candidate cells, with a **maximum fake rate of 60%** in the worst scenario of ttbar+PU200 events.

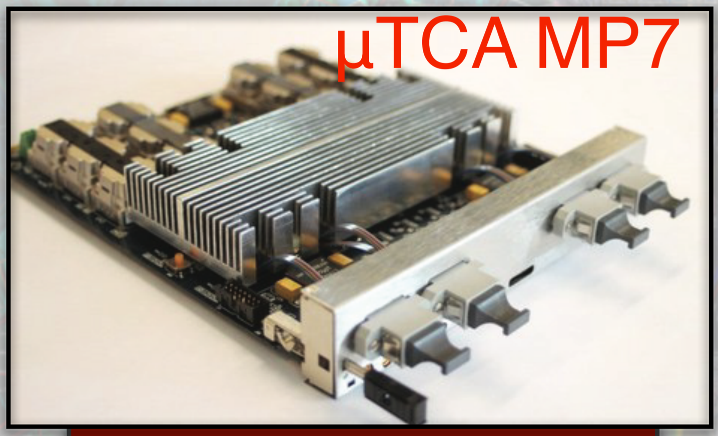
Hardware Implementation



A hardware demonstrator has been built using two **MP7** boards [7]. The Hough Transform algorithm has been implemented with a pipelined firmware. Each pair of links in the MP7 is assigned to a single ϕ_0 segment, so that the HT is performed independently for each of them. Every board processes data from 1 region in η and 9 segments in ϕ_0.



Preliminary **hardware results** show a **good agreement** with the floating point simulation. Firmware found ~92% of candidate tracks with an exact matching rate with the simulation software of 83%.



- FPGA Virtex 7
- 72 I/O Optical Links (12.5 Gbps)
- Tot. bandwidth ~1 Tbps

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Acknowledgment

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