The impact of Moore's Law and loss of Dennard scaling on chip architecture and software

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Moore's law, the doubling of transistors per unit area for each CMOS technology generation, is expected to continue throughout the decade, while Dennard scaling, threshold voltage scaling to maintain constant power per unit area, stopped about a decade ago resulting in an inability to fully utilize the increased transistor density and for increased performance due to power constraints. The limitations on power dissipation has led to efforts to find alternate chip architectures with significantly more energy efficient cores for targeted application domains with chips potentially incorporating several types of such cores to cover well a range of applications. DSP's are examples of chip architectures that already have adopted this design approach for energy efficiency. Heterogeneous architectures are likely to significantly impact the software systems not only through the heterogeneity of architectures, but also through increasingly refined and dynamic management of power. The presentation will discuss these issues and experiences with assessing the energy efficiency of a Texas Instruments DSP for some HPC benchmarks.