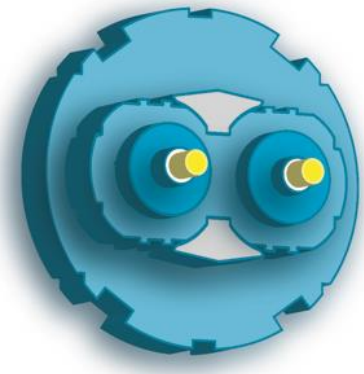

High Luminosity LHC

Joint session of WP3, WP6, WP7, WP11 on **Circuit protection** - Introduction

D. Wollmann

The HiLumi LHC Design Study is included in the High Luminosity LHC project and is partly funded by the European Commission within the Framework Programme 7 Capacities Specific Programme, Grant Agreement 284404.

Session overview versus HL circuit table

Introduction *Daniel WOLLMANN*

Kjell Johnsen Auditorium, CERN

Nb-Ti circuit protection (20+5) *Ezio TODESCO*

SC Link protection (20+5) *Amalia BALLARINO*

Kjell Johnsen Auditorium, CERN

Protection of Nb-Ti Magnets/Circuits and SC Link

MQXF protection & HQ-program experience (20+10) *Giorgio AMBROSIO*

Triplet circuit protection with heaters and CLIQ (20+10)

30-7-018 Kjell Johnsen Auditorium, CERN

11 T protection (20+10)

30-7-018 Kjell Johnsen Auditorium, CERN

Protection of Nb3Sn Magnets/Circuits

	Circuits for HiLumi	Magnet Type	Number of circuits per IP side	I_nominal [kA]	I_ultimate [kA]	I_rated [kA]	L per circuit [mH]	Quench Heaters	CLIQ	EE	Collaborations
Inner Triplet[3]	Triplet Q1, Q3	MQXFA	1	16.5	17.8	18.0	138	Baseline (inner/outer layer)	Baseline	Baseline	US-HiLumi
	Triplet Q2a,Q2b	MQXFB	1	16.5	17.8	18.0	117	Baseline (inner/outer layer)	Baseline	Baseline	CERN
	Trim Q1			2							
	Trim Q2a,Q2b			0.12							
	Orbit correctors Q2a/b vertical	MCBXFBV	2	1.6	1.73	2.00	18	Baseline	no	Option	Ciemat
	Orbit correctors Q2a/b horizontal	MCBXFBH	2	1.47	1.59	2.00	29	Baseline	no	Option	Ciemat
	Orbit correctors Q3 vertical	MCBXFAV	1	1.6	1.73	2.00	33	Baseline	no	Option	Ciemat
	Orbit correctors Q3 horizontal	MCBXFAH	1	1.47	1.59	2.00	53	Baseline	no	Option	Ciemat
	Superferric, order 2	MQSXF	1	0.18	0.20	0.20	1247	no	no	Baseline	INFN
	Superferric, order 3, normal and skew	MCSXF / MCSSXF	2	0.13	0.14	0.20	118	no	no	PC crowbar?	INFN
	Superferric, order 4, normal and skew	MCOXF / MCOSXF	2	0.12	0.13	0.20	152	no	no	PC crowbar?	INFN
	Superferric, order 5, normal and skew	MCDXF / MCDSXF	2	0.14	0.15	0.20	107	no	no	PC crowbar?	INFN
	Superferric, order 6	MCTXF	1	0.17	0.18	0.20	229	no	no	PC crowbar?	INFN
	Superferric, order 6, skew	MCTSXF	1	0.16	0.17	0.20	52	no	no	PC crowbar?	INFN
D1[2]	Separation dipole D1; MBXF	MBXF	1	12	13.0	13.0[3]	25	Baseline	Option	no	KEK
D2[2]	Separation dipole D2; MBRD	MBRD	1	12	13.0	13.0[3]	27	Baseline	Option	no	INFN
	Orbit correctors D2	MCBRD	4	1.5	1.62	2	47	Baseline	no	Option	CERN
Q4	Large aperture 2-in-1 Quad; Q4	MQYY	2	4.50	4.9	6.0	74.0	Baseline	Option	no	CEA
	Orbit correctors Q4	MCBYY	4	1.5	1.62	2	47	Baseline	no	Option	CERN
Q5[1]	Present LHC Q4 magnet	MQY	2	3.61	3.9	4.0	148.0	Baseline	no	no	CERN
	Orbit correctors present Q4	MCBY	6	0.072	0.08	0.12	5270	Baseline	no	no	CERN
Q6	Insertion Quad, 2-in-1 aperture; Q6	MQML	2	4.31	4.7	6.0	21.0	Baseline	no	no	CERN
	Orbit correctors Q6	MCBC	2	0.08	0.09	0.12	2840	Baseline	no	no	CERN
11T	11T dipole, MBH	11T dipole, MBH		11.85	12.798	13	63.5	Baseline	Option	existing RB EE	CERN / FNAL
	Trim circuit			0.2							

Goals and time line for circuit protection

Recommendation from Cost and Schedule Review 03.2015

"Reduce the number of redundant systems for quench protection to a safe level and explore the possibility of replacing the costly and risky energy extraction systems by less expensive solutions."

Questions to each speaker

- Project scope
- State protection simulations
- V-taps, routing of instrumentation cables, required thresholds and allowed evaluation times
- ELQA compatibility (voltage levels)

Time line for circuit protection

- HL- LHC Circuit Review – early spring 2016
- Technical Design Report V1 – spring / summer 2016
- Cost & Schedule Review – autumn 2016

Deliverables and Actors - for each circuit type

- **Detection specification** (Mr. Circuit, WPs 3, 6, 7, 11)
  - Magnet (symmetric/asymmetric), busbar and joints, leads, SC link.
    - V-tap definition
    - Thresholds voltage and evaluation time,
      - documentation of flux-jump voltage spikes,
      - peak temperature vs. threshold parameters.
    - Documentation of measured propagation velocities
      (long. & transv. in high and low field region).
- **Heater design documentation** (WPs 3, 7, 11)
  - Documentation of heater-efficiency experiments and simulations.
- **Active-protection specification** (Mr. Circuit, WPs 3, 6, 7, 11)
  - Crowbar
  - EE (max. current, max. load, switch delay)
  - CLIQ (capacitance, leads dimensions)
  - Heater power-supplies (capacitance, switch delay, leads dimensions)
- **Specification of ELQA tests voltages** (Mr. Circuit and WPs 3, 6, 7, 11)
  - During manufacture, at reception, and in tunnel.
- **PIC interface documentation** (Mr. Circuit, WP 7)
- **Busbar specification** (Mr. Circuit, WPs 3, 6, 7, 11)
- **CLIQ, EE: reliability studies** (Mr. Circuit, WP 7)
- **Electric circuit diagram incl. instrumentation** (Mr. Circuit, WPs 3, 11, 15)
- **Definition of instrumentation routing** (Mr. Circuit and WPs 3, 6, 11, 15)

B. Auchmann, plenary talk 27.10.2015

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