

JRA1 - Data Acquisition Status Report

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DPNC Genève

Extended SC Meeting

1 Sep 2008

Draft version, incomplete

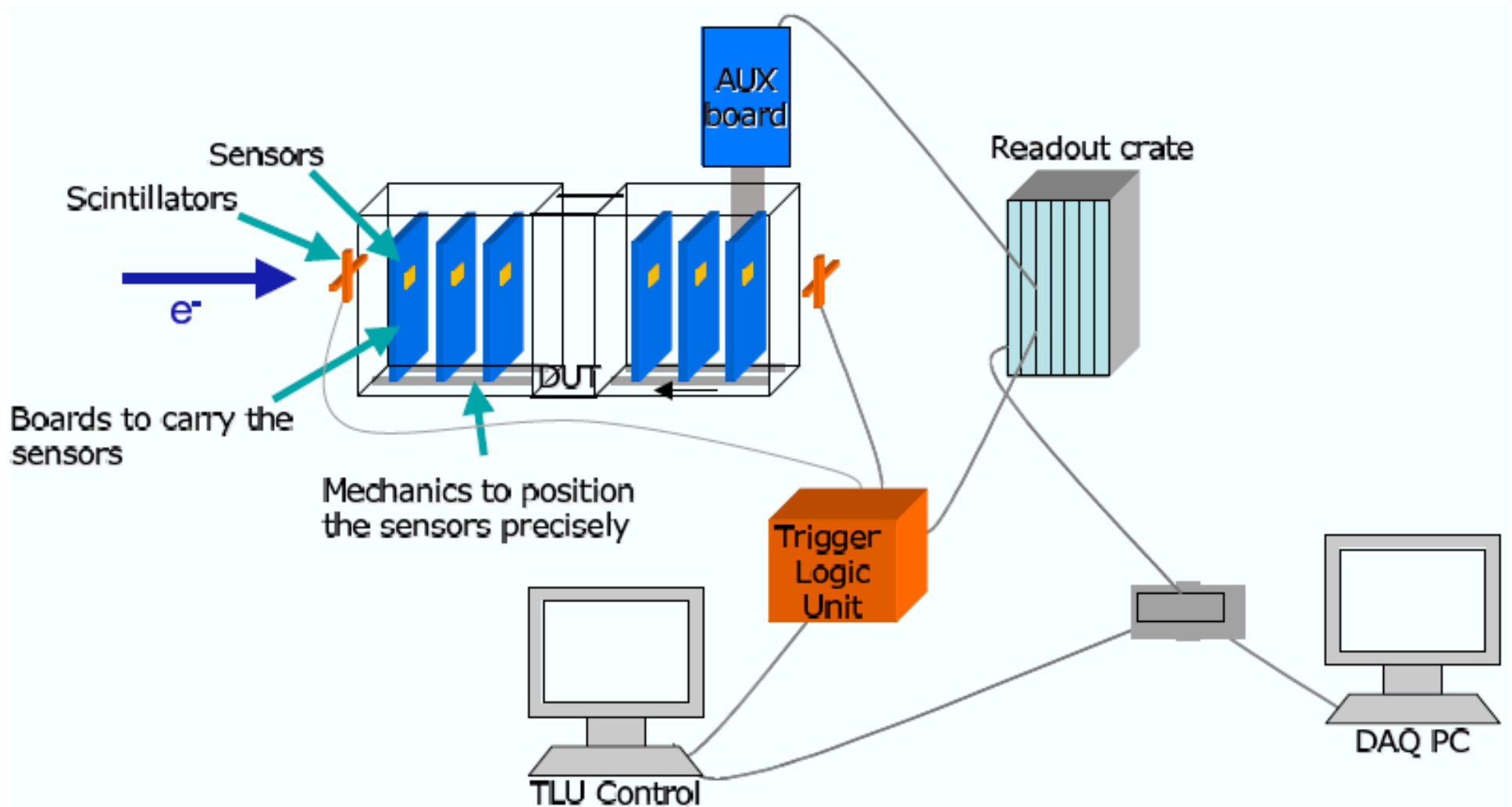


Outline

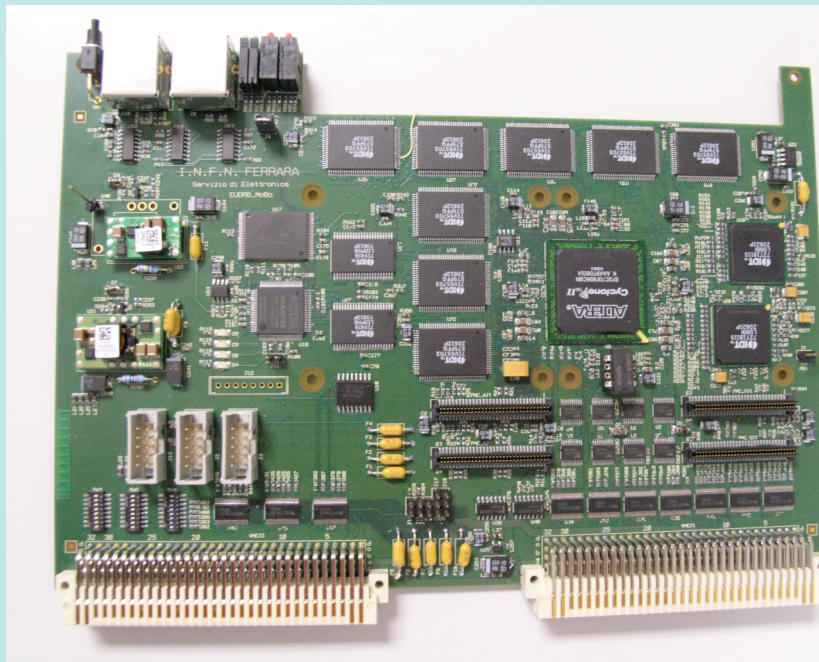
- System Level Overview
- Hardware
 - EUDRB
 - TLU
- Software-Architecture
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- Documentation
 - on eudet
 - on hepforge
- Milestones
- Highlights
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- Open Questions
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System Level Overview



EUDRB by INFN Ferrara



mother board built around an ALTERA Cyclone II FPGA (clock rate: 80MHz) and hosting the core resources and Interfaces (VME64X slave, USB2.0, EUDET trigger bus)

NIOS II, 32 bit “soft” microcontroller (clock rate: 40Mz) implemented in the FPGA for

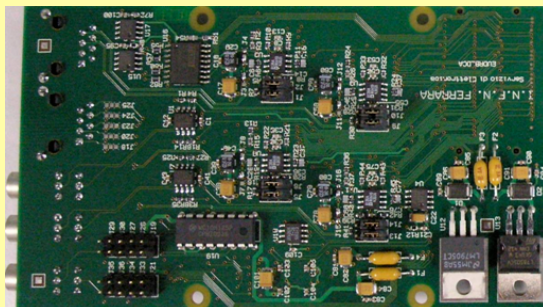
- on board diagnostics
- on-line calculation of pixel pedestal and noise
- remote configuration of the FPGA via RS-232, VME, USB2.0

Two readout modes:

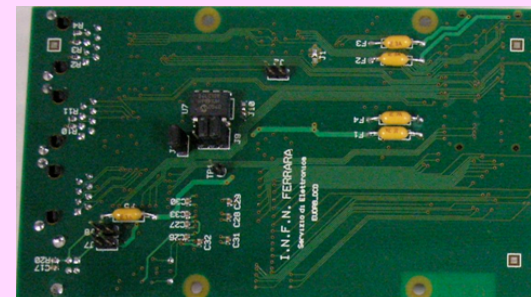
Zero Suppressed readout to minimize the readout dead-time while in normal data taking.

Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations

analog daughter card based on the successful LEPSI and SUCIMA designs clock rate up to 20 MHz



digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link



Trigger Logic Unit

- Simple Handshake via Trigger/Busy/Reset on RJ45 LVDS lines (or TTL-Lemo)
- Timestamp and event-number via USB

Eventnumber via advanced data handshake on RJ45 available

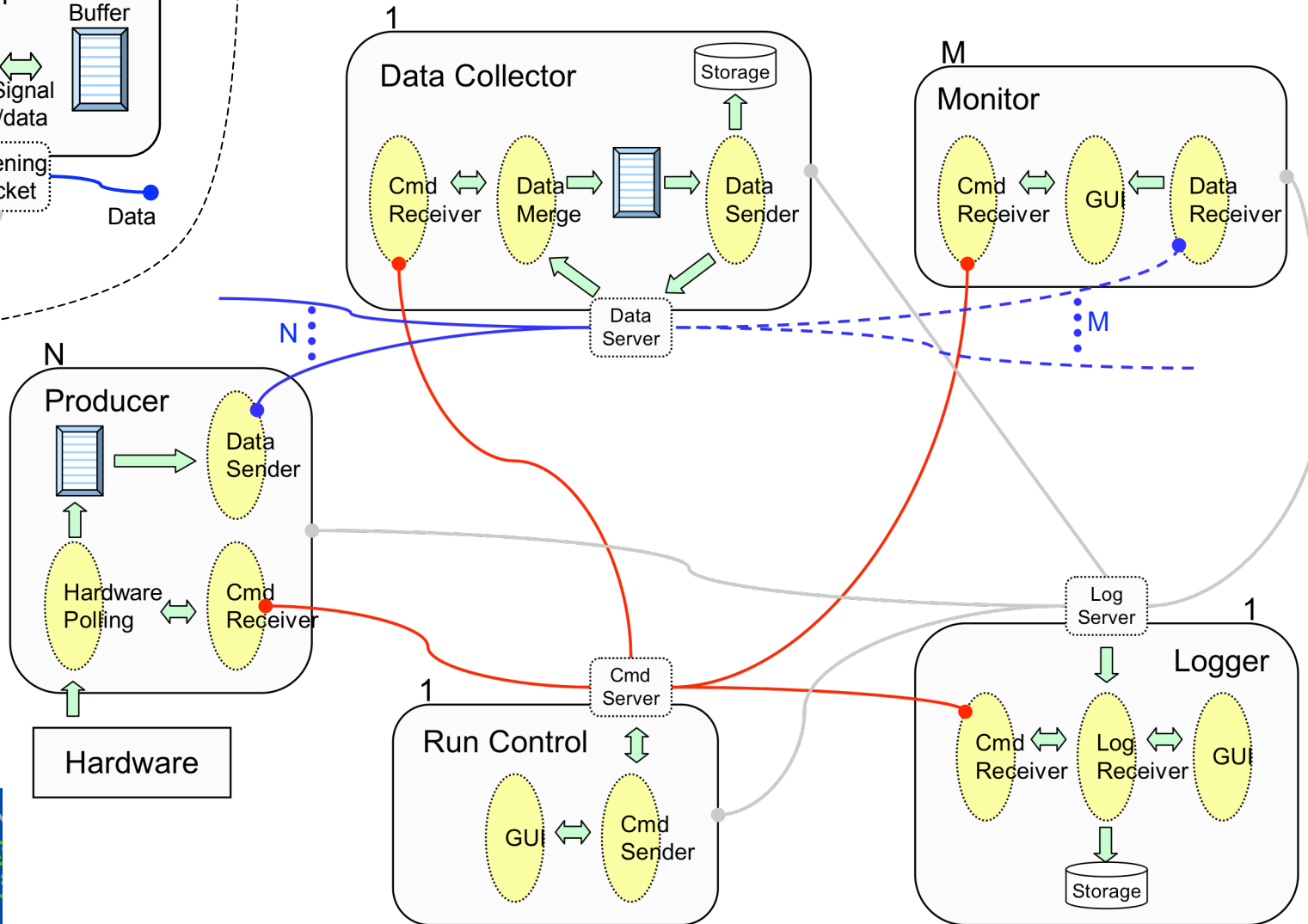
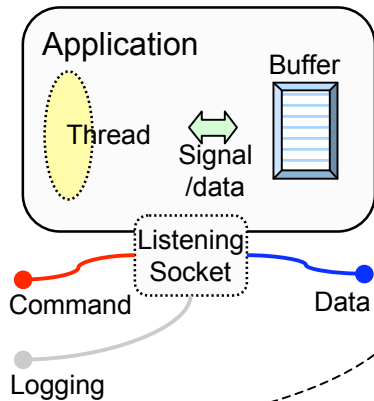
- Version 0.2 now available, more IO etc.

- In collaboration with Bristol



DAQ-Architecture JRA1

Key:



JRA1 DAQ Key Features

- Platform independent (Linux, MacOS X, Windows under Cygwin) and highly modular
- current suite of ILC software (LCIO/Marlin etc) also runs under MacOS, but no official support yet
- DUTs can **(and should)** be easily integrated in our DAQ, simple examples and help is provided
- SVN Repository and Documentation at:

<http://projects.hepforge.org/eudaq/>



eudaq Run Control

Control

Config: isis_and_tel_zs Config

Run: Start

Log: Log

Reset Stop

Status

Run Number: 4581 Rate: 0 Hz

Triggers: 747 Mean Rate: 0.242153 Hz

Events Built: 747 File Bytes: 33028971

Connections

type	name	state	connection
DataCollector		OK	127.0.0.
LogCollector		OK	127.0.0.
Monitor	Root	OK	127.0.0.
Producer	TLU	OK: Started	129.194
Producer	EUDRB	OK: Started	129.194

Level: 4-INFO From: All Search:

Time	Level	Text
09:05:24.488	4-INFO	Run 4579, EORE = 1
09:06:13.298	4-INFO	Starting Run 4580:
09:06:13.800	4-INFO	Preparing for run 4580, file=...
09:06:13.901	4-INFO	Starting run 4580, file=../data
09:15:22.216	4-INFO	End of run 4580
09:15:22.216	4-INFO	Stopping Run 4580
09:15:24.084	4-INFO	Run 4580, EORE = 2
09:15:28.008	4-INFO	Starting Run 4581:
09:15:28.509	4-INFO	Preparing for run 4581, file=...
09:15:28.610	4-INFO	Starting run 4581, file=../data
09:41:39.061	4-INFO	Board 0 pedestals loading from
09:41:42.336	4-INFO	Board 1 pedestals loading from
09:41:45.611	4-INFO	Board 2 pedestals loading from
09:41:48.887	4-INFO	Board 3 pedestals loading from
09:41:52.165	4-INFO	Board 4 pedestals loading from
09:41:55.442	4-INFO	Board 5 pedestals loading from
09:41:55.444	4-INFO	Configured (isis_and_tel_zs)
09:42:10.980	4-INFO	Board 0 pedestals loading from
09:42:14.258	4-INFO	Board 1 pedestals loading from
09:42:17.536	4-INFO	Board 2 pedestals loading from
09:42:20.812	4-INFO	Board 3 pedestals loading from
09:42:24.090	4-INFO	Board 4 pedestals loading from fil...
09:42:27.367	4-INFO	Board 5 pedestals loading from fil...
09:42:27.369	4-INFO	Configured (isis_and_tel_zs)

EUDAQ Root Monitor

File name: ../data/run004581.raw Run #: 4581 Event #: 747 Reduce by: 1 Update every: 10.0 Colours: Board 0 Board 1 Board 2 Board 3 Board 4 Board 5

Conf | Board 0 | Board 1 | Board 2 | Board 3 | Board 4 | Board 5 | CDSLego | Main

Cluster X Profile

Entries: 879
Integral: 1.948e+05

Cluster Y Profile

Entries: 879
Integral: 1.948e+05

CDS Profile

Cluster Profile

Entries: 879
Integral: 1.948e+05

Cluster Charge

Entries: 879
Integral: 862

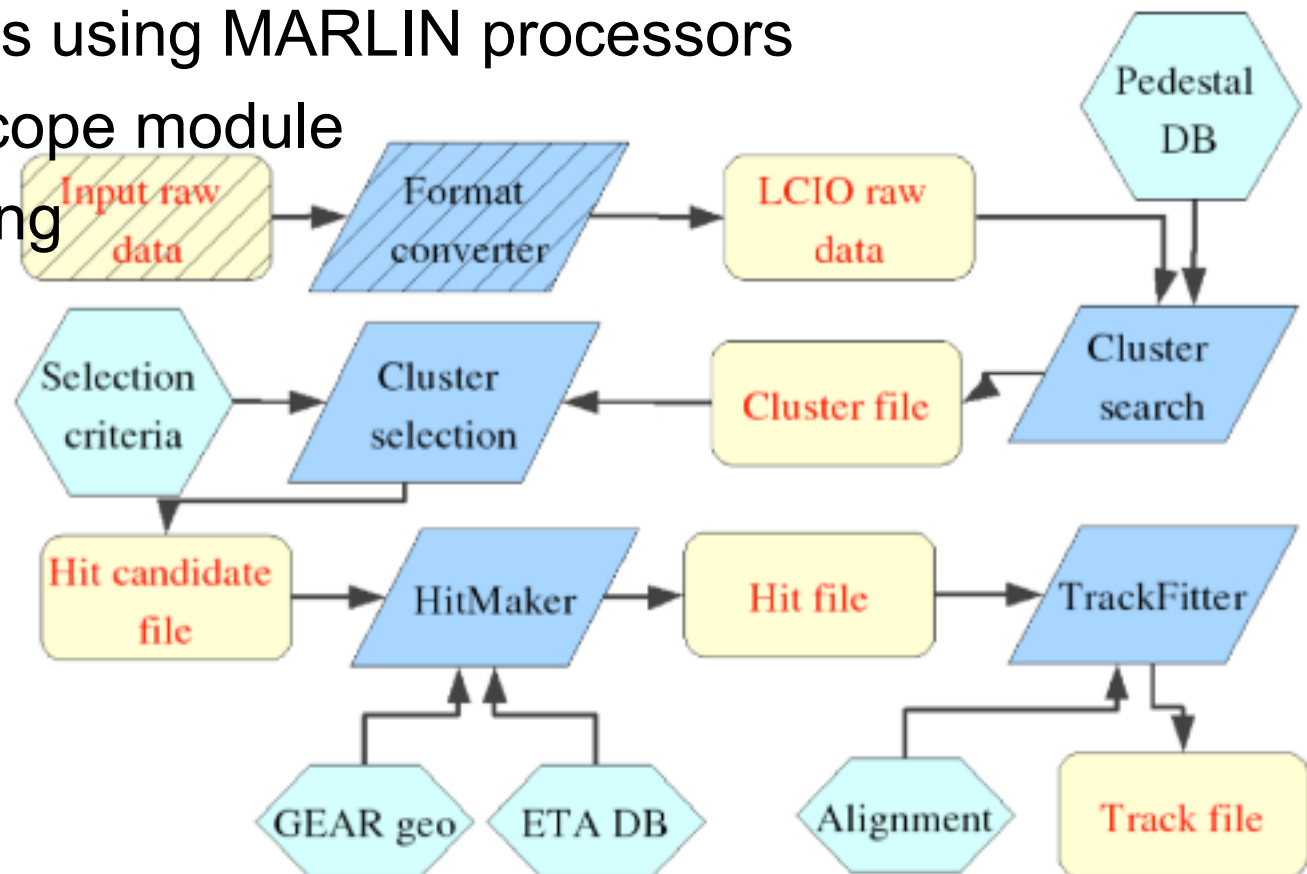
Num Clusters

Producer.EU... EUDRBProd... OnConfigure(const eudaq::Configuration&)
Producer.EU... EUDRBProd... OnConfigure(const eudaq::Configuration&)
Producer.EU... EUDRBProd... OnConfigure(const eudaq::Configuration&)

Wed 8/27/2008 11:07 Wed 8/27/2008 11:07 mmm.cern.ch

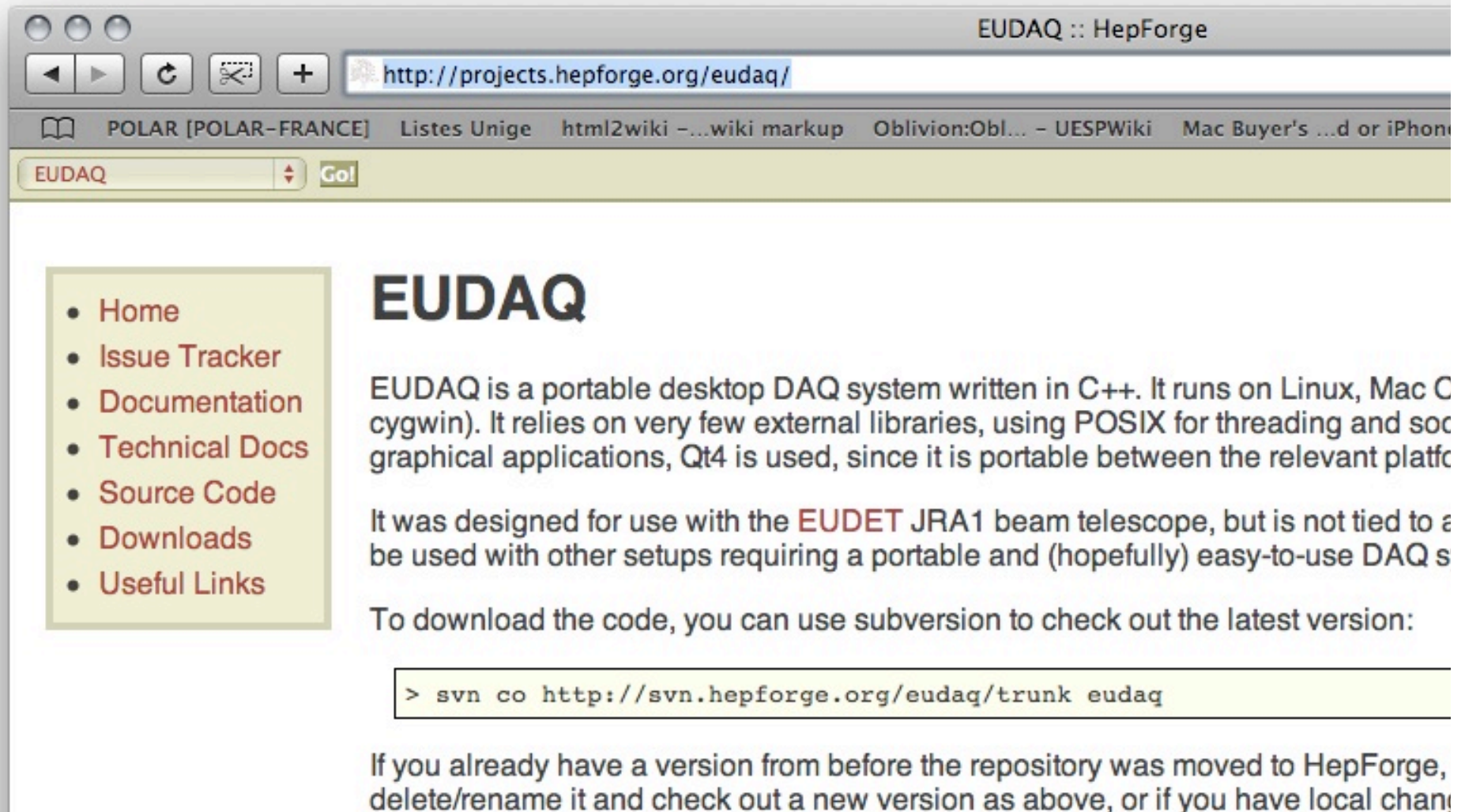
Analysis chain

- Proprietary raw format on DAQ-PC
- RAW data processed to LCIO on the GRID
- Data analysis using MARLIN processors
 - EUTelescope module
 - Track fitting



Documentation...

- SVN, Doxygen and Bugtracking on hepforge:



The screenshot shows a web browser window titled "EUDAQ :: HepForge". The address bar contains the URL "http://projects.hepforge.org/eudaq/". The browser's tab bar shows several tabs, including "POLAR [POLAR-FRANCE]", "Listes Unige", "html2wiki - ...wiki markup", "Oblivion:Obl...", "UESPWiki", and "Mac Buyer's ...d or iPhone". The main content area features a navigation menu on the left with the following items:

- Home
- Issue Tracker
- Documentation
- Technical Docs
- Source Code
- Downloads
- Useful Links

EUDAQ

EUDAQ is a portable desktop DAQ system written in C++. It runs on Linux, Mac C (cygwin). It relies on very few external libraries, using POSIX for threading and some graphical applications, Qt4 is used, since it is portable between the relevant platforms.

It was designed for use with the **EUDET** JRA1 beam telescope, but is not tied to a specific setup and can be used with other setups requiring a portable and (hopefully) easy-to-use DAQ system.

To download the code, you can use subversion to check out the latest version:

```
> svn co http://svn.hepforge.org/eudaq/trunk eudaq
```

If you already have a version from before the repository was moved to HepForge, delete/rename it and check out a new version as above, or if you have local changes

...Documentation...

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	Wiki	Timeline	Roadmap	Browse Source	View Tickets	Search	Doxygen
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[Last Change](#) | [Revision L](#)

root / trunk

 View revision:

Name ▲	Size	Rev	Age	Last Change
../				
bin		394	2 months	corrin: tlnoroot program to replace script
conf		423	1 week	corrin: Config files from CERN 2008-08 test beams
depfet		424	1 week	corrin: DEPFET tweaks from before (nothing significant)
doc		267	10 months	corrin: More rearranging - moverd Makefile.common up a directory
eudrb		407	1 month	corrin: Fix typo
extern		358	3 months	corrin: Fixed includes in ZestSC1
gui		307	7 months	corrin: Increased spacing in euRun gui
images		193	1 year	corrin: Rearranged directories for trunk / tags
main		425	1 week	corrin: DataCollector? allows offset of 1 in event numbers
ports		193	1 year	corrin: Rearranged directories for trunk / tags
root		411	1 month	corrin: New correlation plots in RootMonitor
tlu		427	1 week	corrin: CERN 2008-08 tlu producer fixes
vme		316	6 months	corrin: Added scaler control program, cleaned up VME interface

...Documentation...

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Welcome to the EUDAQ Wiki

- **GettingStarted** with EUDAQ
 - **Downloading**
 - **Building**
 - **Configuring?**
 - **Running**
- Using the EUDET JRA1 **BeamTelescope**:
 - Using the Trigger Logic Unit (TLU)
 - Using the **EUDRB** readout board
 - The **MimoTEL** sensor chips
- The EUDAQ software **Applications**:
 - **STARTRUN** EUDAQ startup script
 - **euRun** GUI Run Control
 - **euLog** GUI Log Collector
 - **RootMonitor** A monitor process for displaying Root histograms

...Documentation

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{1} Active Tickets (9 matches)

- List all active tickets by priority.
- Color each row based on priority.
- If a ticket has been accepted, a '*' is appended after the owner's name

Ticket	Summary	Component	Version	Milestone	Type	Owner	Created
#10	DAQ hangs on start of run	any			defect	corrin	19/02/08
#12	Log file messages should be escaped	libeudaq			defect	corrin *	22/02/08
#6	Improve VME access speed	eudrb			enhancement	corrin *	17/12/07
#7	Clean up Monitor code	any			enhancement	corrin	17/12/07
#8	Write Grid submitter	any			enhancement	corrin	17/12/07
#11	Add received time to log messages	libeudaq			enhancement	corrin *	22/02/08
#3	Set up Doxygen	any			task	corrin *	19/10/07
#4	Comment code	any			task	corrin *	19/10/07
#5	Improve thread safety	any			task	corrin	17/12/07



Milestones

- Achieved:
 - Readout for prototype ready July 2007
 - current software is robust and easy-to-use
- Still open:
 - Readout for final telescope, Dec 2008 (full integration by March 2009)
 - Software needs improved speed
 - Hardware must adapt to new sensor



Open Questions...

- VME-Speed
 - Readout speed via VME currently limited at ~70 Hz for 6 sensor planes, aim is 1 kHz
 - single sensor readout in ~25 μ s, but change of sensor board takes ~2 ms
 - driver issue, will be investigated in the coming months



...Open Questions...

- EUDRB Firmware validation
 - improved firmware with new features ('rolling' raw frames, synchronized readout)
 - needs validation and careful bug checking
 - some timing/noise issues under investigation



...Open Questions

- Code documentation
 - automatic documentation generation in place via Doxygen
 - needs more comments in the code
 - target date: March 2009



Readout of Mimosa26

- Mimosa26 needs a binary readout
- Baseline: current EUDRB with new digital I/O daughter board
- As an alternative, INFN is investigating a commercial digital I/O board from CAEN (V1495) for some of their sensors



Conclusions...

- Multiplatform DAQ, easy to use
- DUT integration at different levels possible
 - Trigger level, with separate DAQs
 - Full integration, with combined file-writing
- Full integration of DUTs in our DAQ:
 - DEPFET
 - Mimoroma
- Integration at trigger level:
 - SiLC
 - ISIS
 - CALICE

• Full analysis chain from Raw data via LCIO to the GRID, DUTs can profit as well (DEPFET)



...and Outlook

- Readout for Mimosa26 will start soon
 - EUDRB with new digital daughterboard (baseline)
 - commercial digital board from CAEN V1495 (under evaluation)
- Still to address:
 - VME readout speed
 - some more debugging
 - code documentation
- (Nearly) ready for running through 2009/2010, already 2008 successful 'servicing' for users

