RELIABILITY ANALYSIS OF QUENCH LOOP AND INTERFACE ARCHITECTURES: VERIFICATION THROUGH MONTECARLO SIMULATIONS

ANDREA APOLLONIO
BE-OP-LHC

Sigrid Wagner

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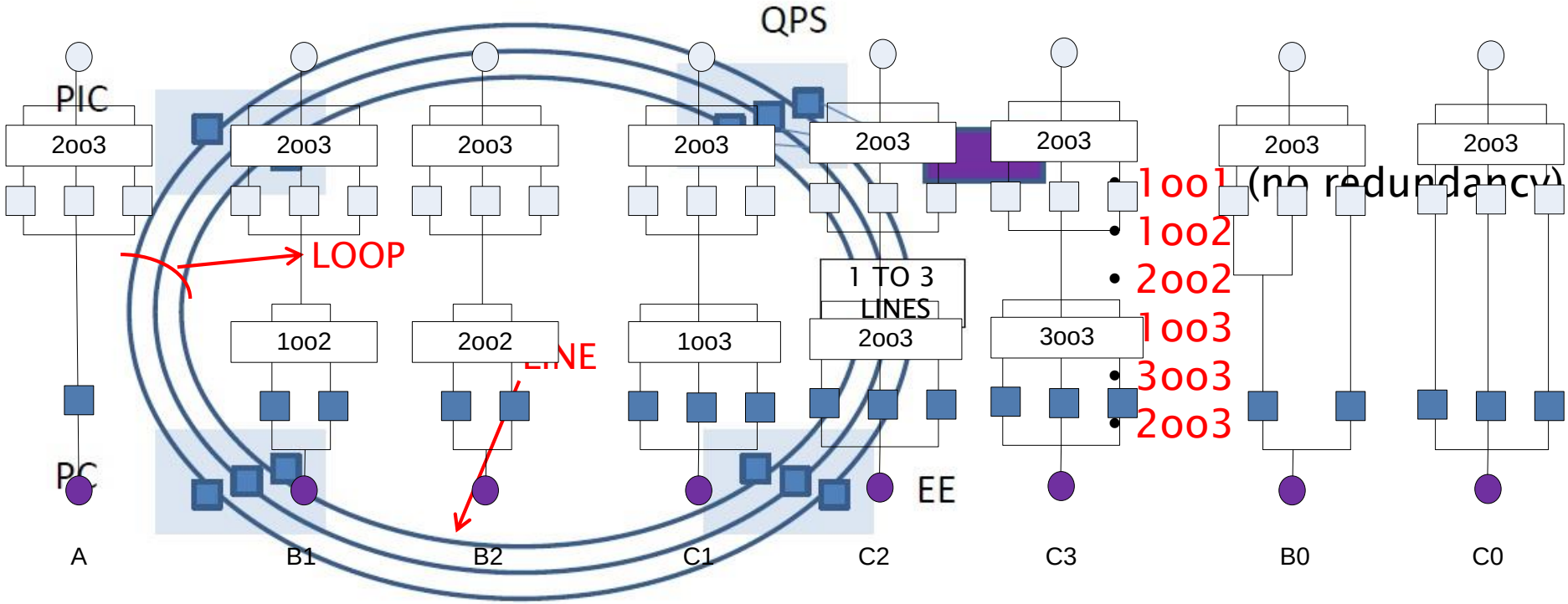
QUENCH LOOP AND INTERFACE MODELS



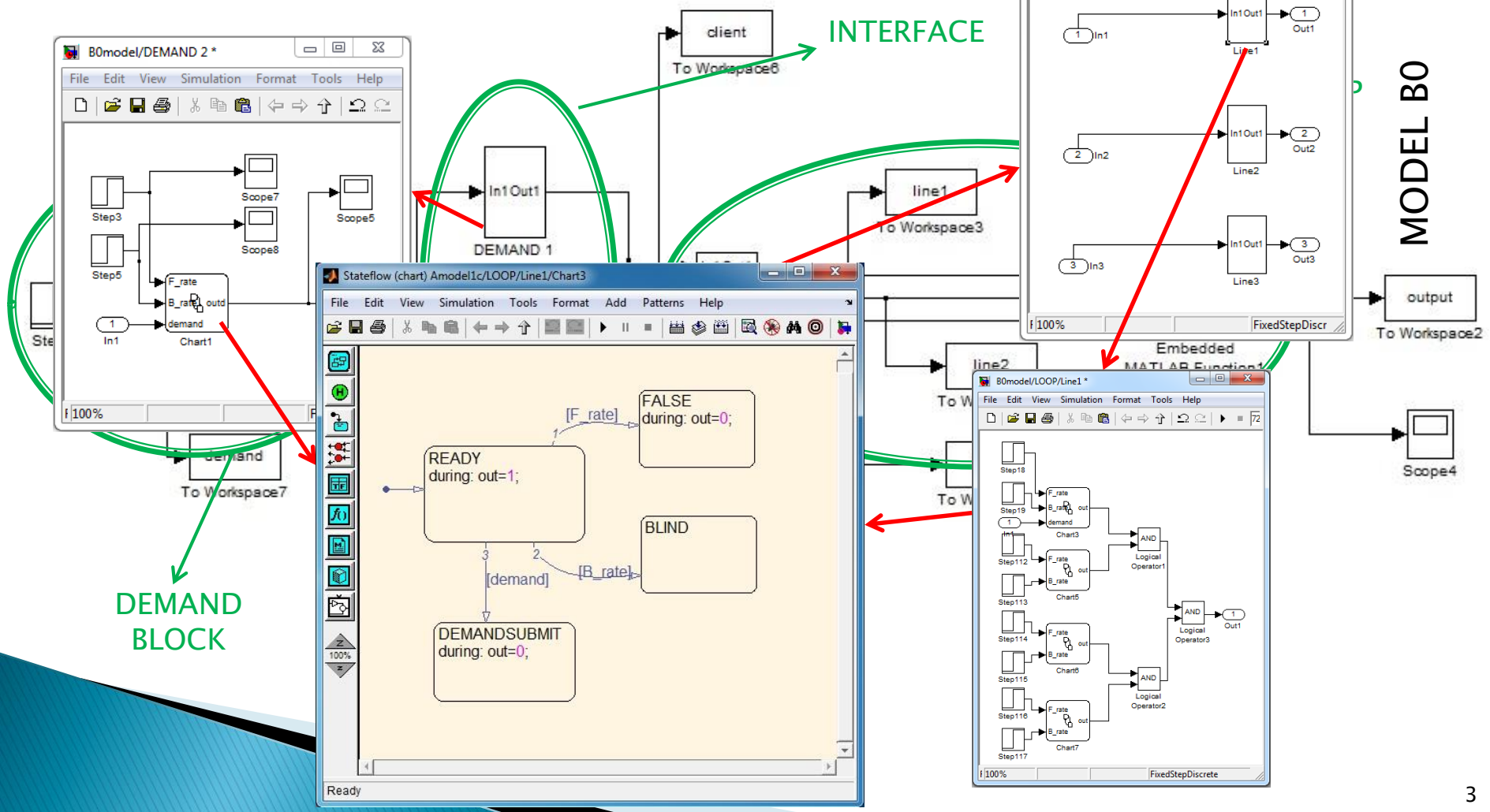
INTERFACE MODELS

Approaches:

- *EXPLICIT APPROACH* (Simulink)
- *IMPLICIT APPROACH*

EXPLICIT APPROACH: MODELS IMPLEMENTATION

- *EXPLICIT APPROACH* (Simulink): a block diagram describes the behavior of the different architectures; signals are used to determine[illegible]n a certain (randomly generated) configuration of the inp[illegible]



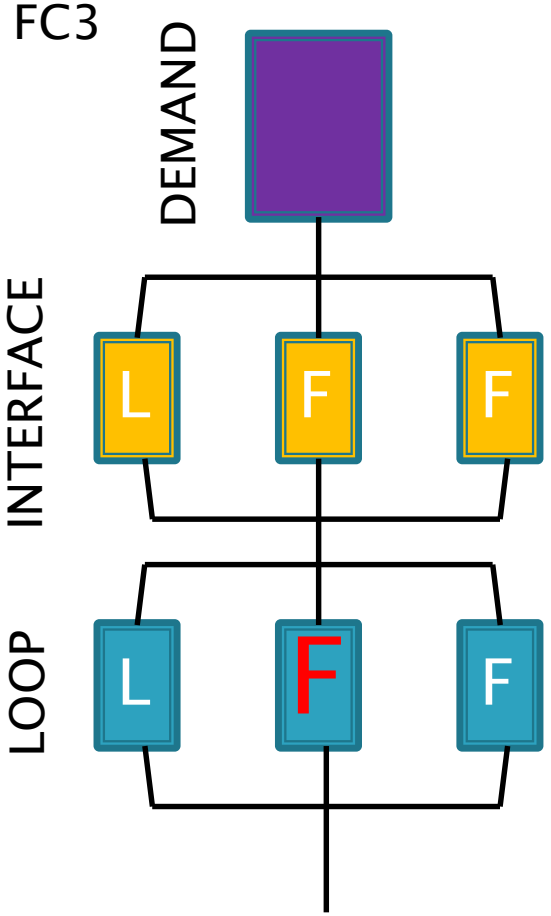
INTERFACE IMPLICIT APPROACH: ALGORITHM

- For each iteration step (IS) of the algorithm a new event of the sequence is added to the loop state table; THERE CAN BE 'INDUCED' EVENTS
- L: at the given iteration of the algorithm one element (ELXY or ELCX) is blind
- F: at the given iteration of the algorithm one element spuriously opens
- D : at the given iteration of the algorithm there's a demand

TEST SEQUENCE (C2 architecture): F13, LC1, FC2, L11, FC3

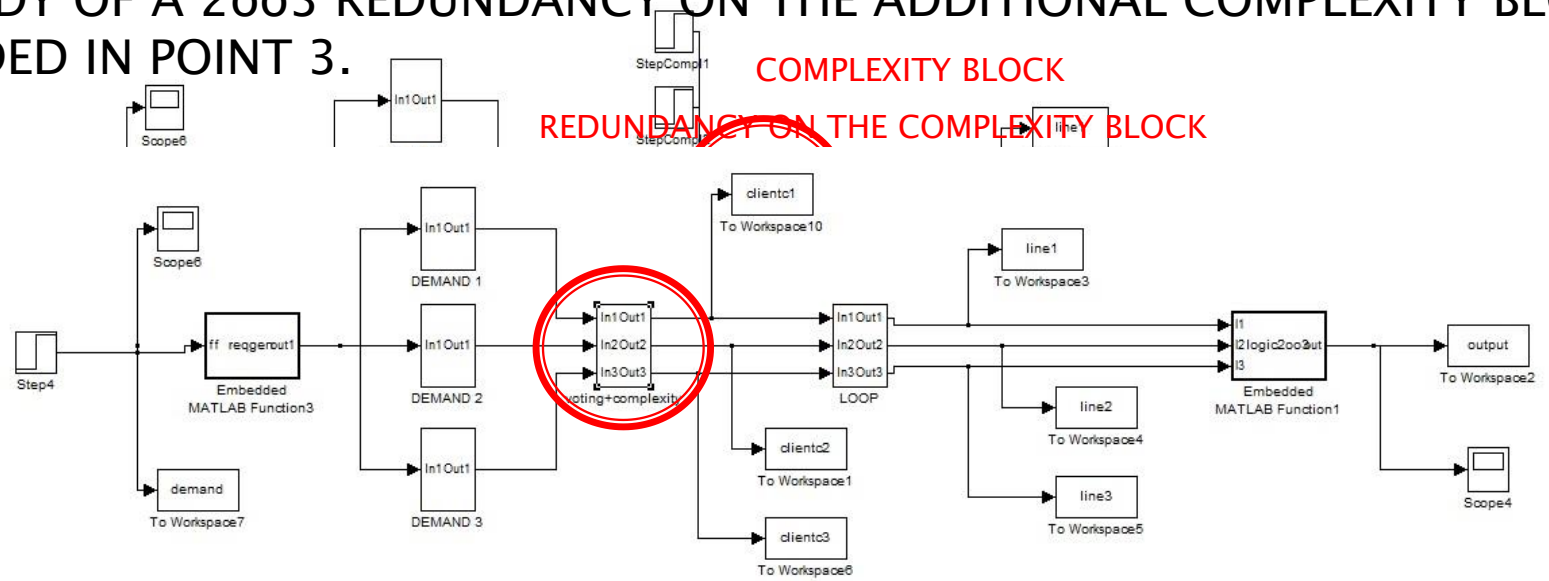
	IS1	IS2	IS3	IS4	IS5
EL11				L11	L11
EL12					F12
EL13	F13	F13	F13	F13	F13
ELC1		LC1	LC1	LC1	LC1
ELC2			FC2	FC2	FC2
ELC3					FC3
ELDM					

False Success



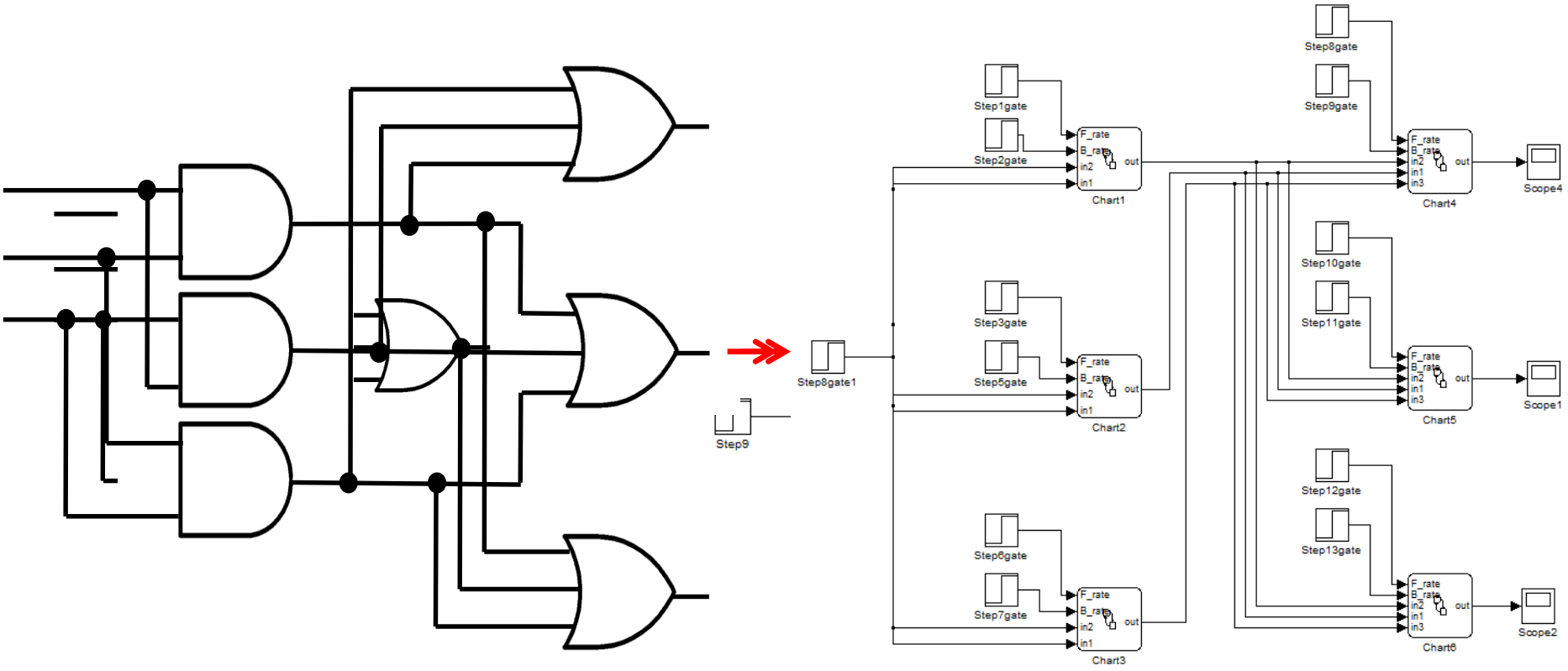
FURTHER DEVELOPMENTS (1/3)

1. INPUT VERIFICATION: to verify the correct behavior of the developed model input parameters (in particular lf) have been changed by two orders of magnitude and the results have been compared again with the theoretical ones (10^7).
2. INCLUDING THE COMPLETE MODEL (4 COMPONENTS) FOR THE LOOP WITH THE EXPLICIT APPROACH
3. STUDY OF THE IMPACT OF THE HIGHER HARDWARE COMPLEXITY OF C2 WITH RESPECT TO C0 ON THE CALCULATED SCENARIO PROBABILITIES
4. STUDY OF A 2oo3 REDUNDANCY ON THE ADDITIONAL COMPLEXITY BLOCK ADDED IN POINT 3.



FURTHER DEVELOPMENTS (2/3)

5. STUDY OF THE IMPLEMENTATION OF THE 2oo3 ARCHITECTURE AT THE GATE LEVEL



FURTHER DEVELOPMENTS: PRELIMINARY RESULTS (3/3)

1. INPUT VERIFICATION: GOOD AGREEMENT WITH THEORETICAL RESULTS (PRESENTED BY SIGRID)
2. COMPLETE MODEL WITH 4 COMPONENTS IN THE LOOP (ONLY EXPLICIT, 10^4 ITERATIONS)
3. 4. STUDY OF THE IMPACT OF THE HIGHER HARDWARE COMPLEXITY OF C2 WITH RESPECT TO C0 ON THE CALCULATED SCENARIO PROBABILITIES
5. 2oo3 ARCHITECTURE GATE LEVEL ANALYSIS – FAILURE RATES: FAILURE MODES DEPEND ON THE ADOPTED TECHNOLOGY FOR THE GATES, A PROPER MODEL STILL NEEDS TO BE DEVELOPED (CMOS: 3 FAILURE RATES?)

	MC (1 COMP)	MC (4 COMP)	DS (1 COMP)	DS (4 COMP)	FS (1 COMP)	FS (4 COMP)	DM (1 COMP)	DM (4 COMP)
C0	0.82							0.0005
C1	0.68							0.0005
C2	0.84							0
C3	0.85							0.0017

	MISSION COMPLETED SUCCESS	DEMAND SUCCESS	FAILURE SUCCESS	DEMAND MISSED
C0 (1,3*10^8)	0.82	0.1276	0.1	0.02
C2 (1,3*10^8)	0.84723404	0.12682978	0.028414893	3.191489362e-005
C2+COMPL (10^7)	0.78	0.1277	0.0875	4.57e-004
C2+COMPL+ RED (3*10^4)	0.8175	0.124	0.058466666 67	3.333333333 e-005

THANK YOU FOR YOUR ATTENTION