Low Mass

Rui de Oliveira (CERN)

Outline

- Aluminum circuits
  - Material budget /General possibilities
  - Micro-via
  - Finishing possibilities
  - Different examples
- Wire bonding alternatives
  - Embedded active devices

Material budget

Material	Radiation length [cm]	Density [gr/cc]	Resistivity [uohms*cm]
Gold	0.3	19.3	2.4
Copper	1.4	9.0	1.7
Aluminum	8.9	2.7	2.7
Glass epoxy	19.4		
Polyimide	29.0		
Beryllium	35.3	1.9	3.3

Copper is close to 6.5 times less transparent than aluminum
And aluminum has only 1.6 times the resistivity of copper
Polyimide is 1.5 times better than glass epoxy.

Possibilities

- Aluminum
  - Laminated:
    - Foils of 15 , 30 or 50 um (crystalline)
  - Vacuum deposited:
    - From 5 to 30um (Amorphous)
  - Pattern size:
    - Minimum line width : 4 time the thickness (3 times for copper)

- Dielectrics
  - Polyimide :
    - 12um , 25um, 50um, 75um
    - Liquid polyimide from 1 to 10um
  - Photoimageable coverlay (modified epoxy):
    - 25um, 50um , 64um
  - Epoxy glue:
    - 5um (liquid), 12um , 25um

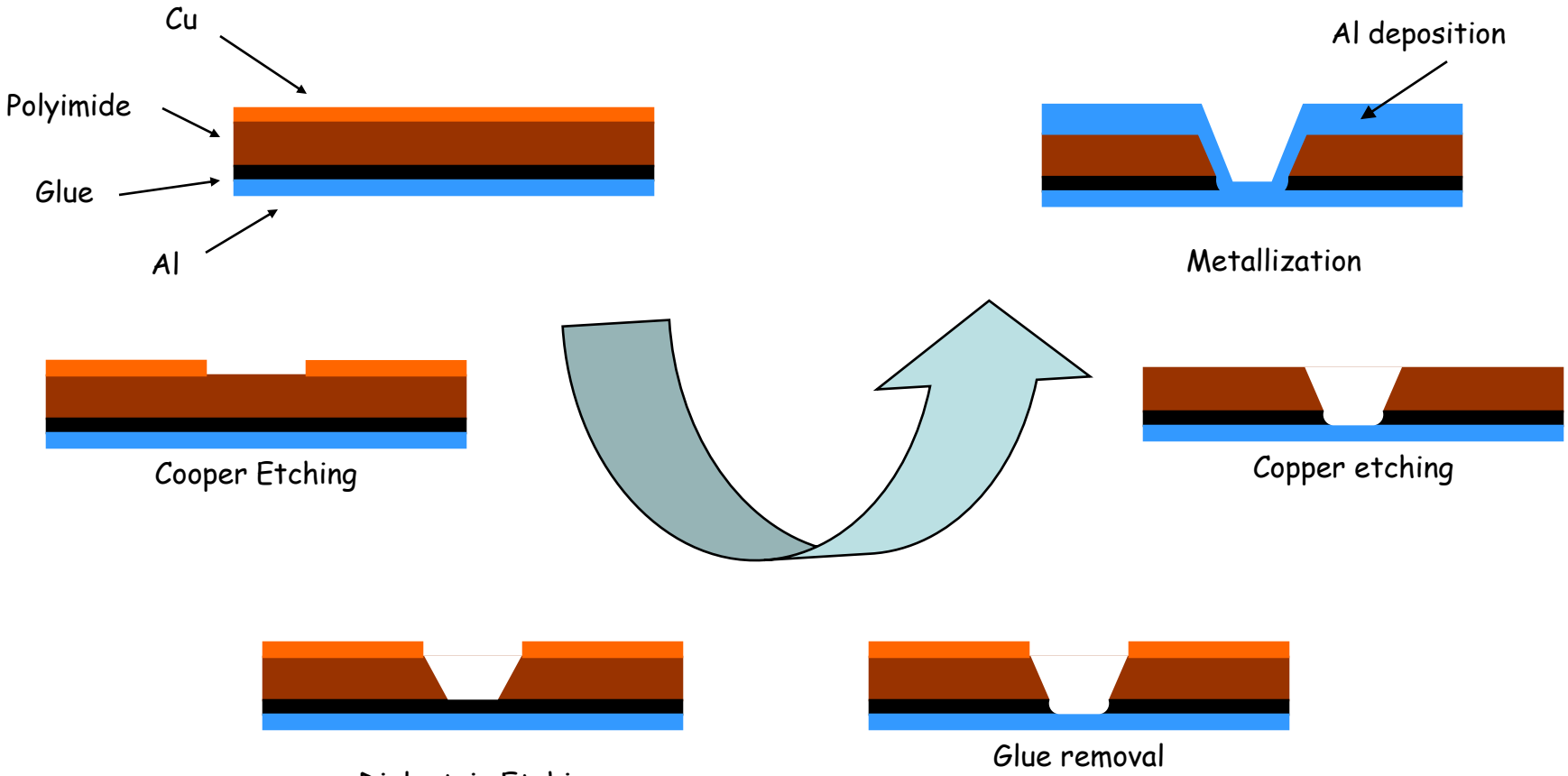
- Hole or vias
  - Minimum 0.05mm diameter

- Sizes
  - Up to 2m x 50cm for single sided flex
  - Up to 1m x 30cm for double sided flex with plated through holes
  - Up to 60cm x 10 cm for multilayer structures

Outline

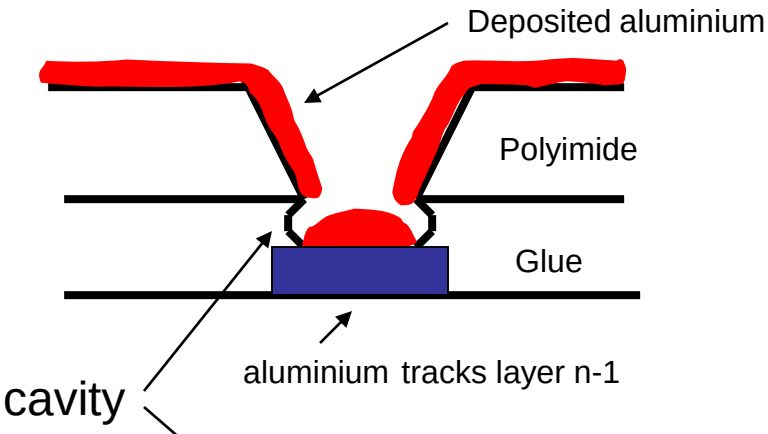
- Aluminium circuits
  - Material budget /General possibilities
  - Vias/Microvias
  - Finishing possibilities
  - Different examples
- Wire bonding alternatives
  - Embedded active devices

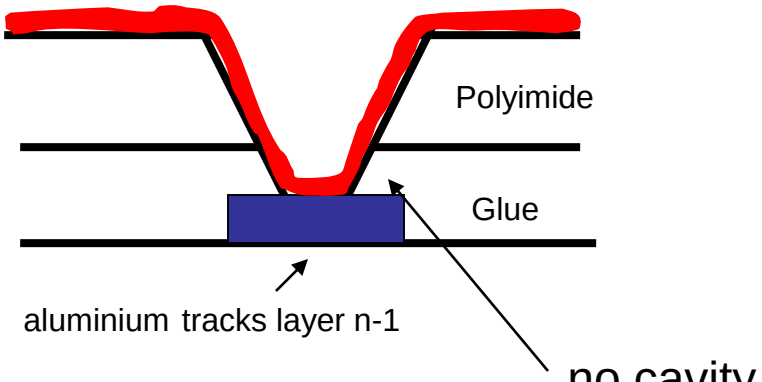
Micro-via , Process with Laminated PI

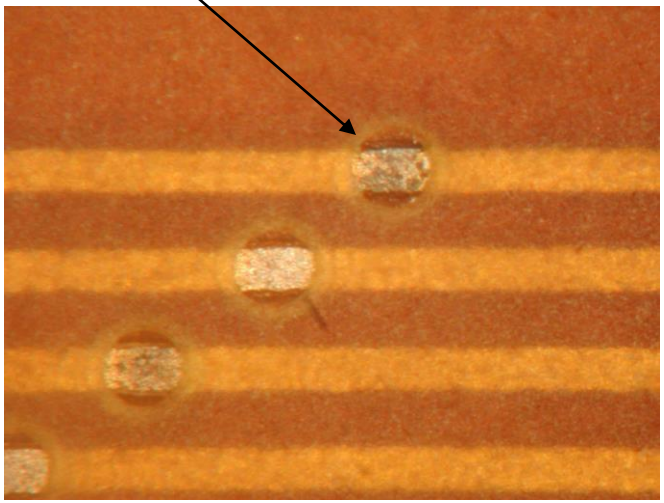


Minimum Via : 50um
Processing temp : 170 deg
Processing temp in study: 20deg

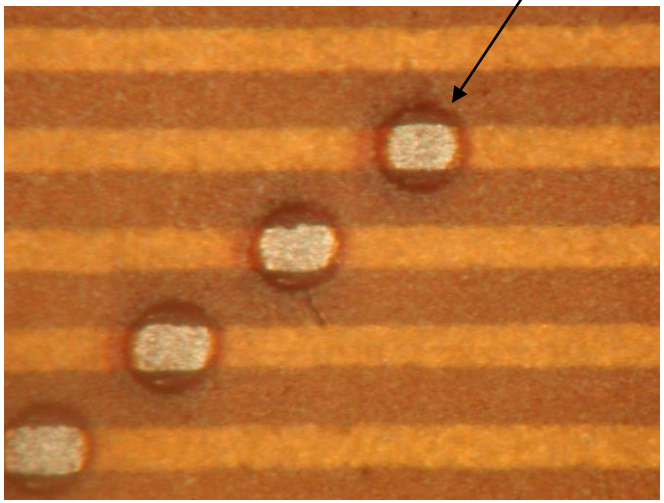
Glue removal





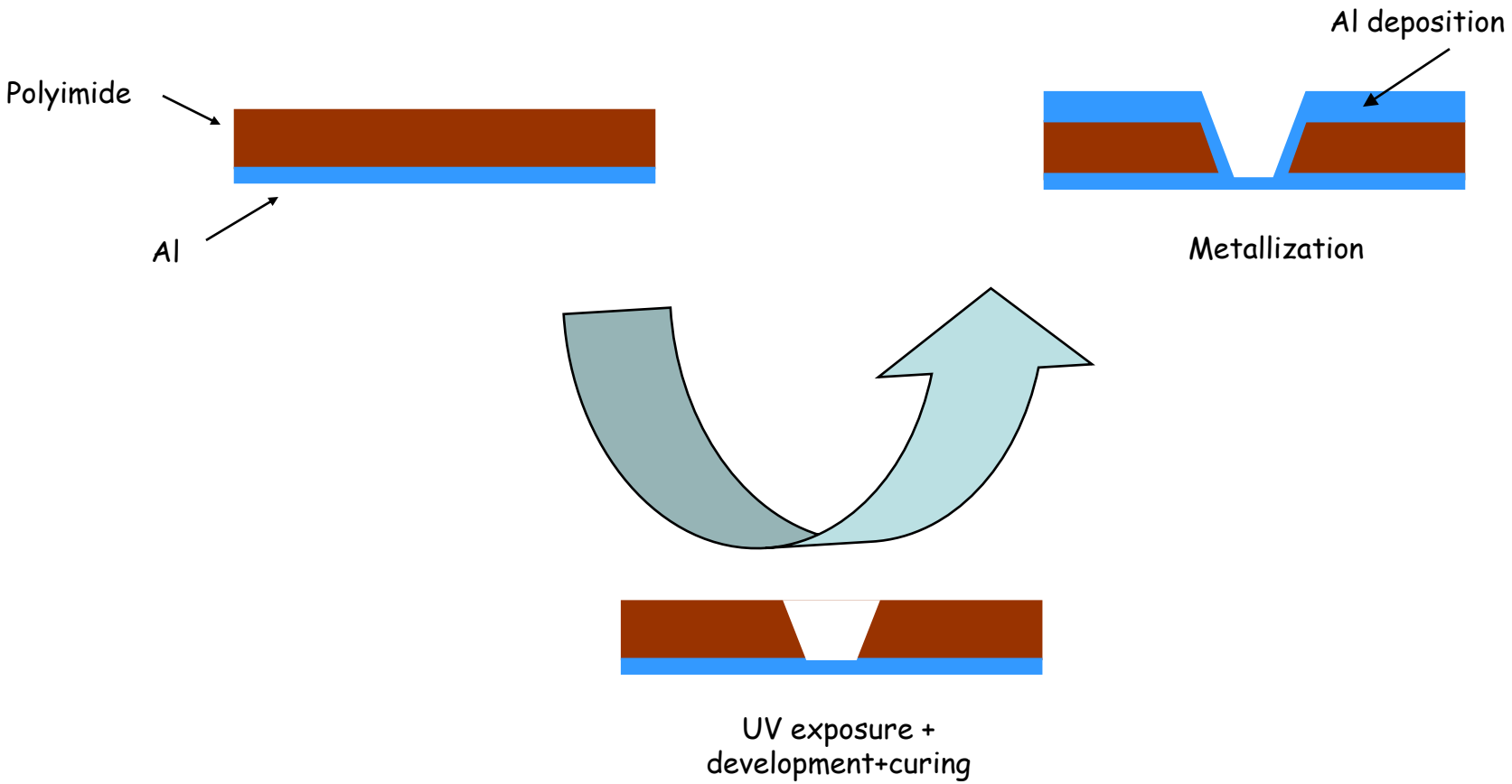


Glue removed chemically



Glue removed by Micro-sand blasting

Process with liquid Polyimide



Minimum Via : 20um
High temp process : 300 deg

Outline

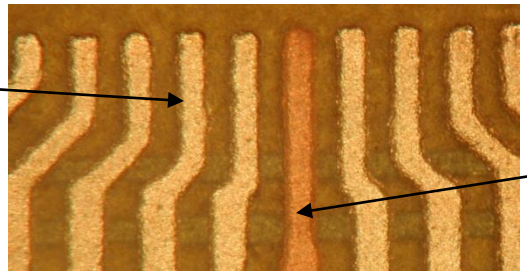
- Aluminum circuits
  - Material budget /General possibilities
  - Vias/Micro-vias
  - Finishing possibilities
  - Different examples
- Wire bonding alternatives
  - Embedded active devices

Finishing possibilities

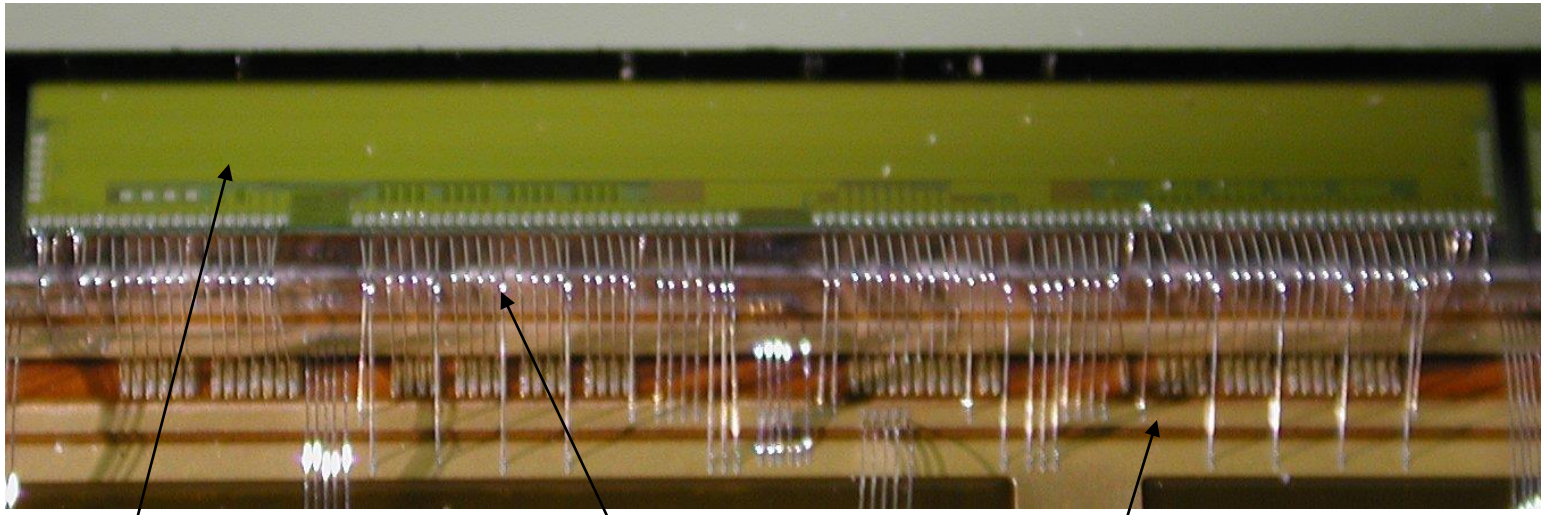
- For wedge aluminum bonding
  - No treatment in case of Crystalline Aluminum
  - Chemical NI/Au Plating on Amorphous deposited Aluminum
- For Au Bonding
  - No treatment in case of Crystalline Aluminum
  - Chemical NI/Thick Au Plating on Amorphous deposited Aluminum
- For soldering
  - Chemical NI/Au Plating

Bonding Close up view example

10umAl + 0.1umZinc + 10umNi + 0.1umAu
With sand blast pre-treatment



Plating defect



Ladder

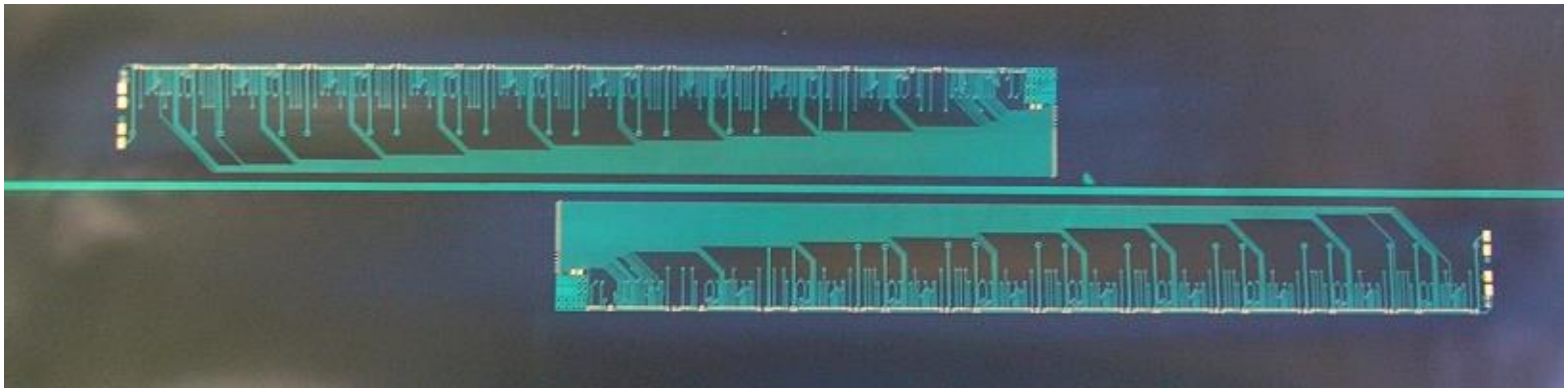
Bonding

AL bus

Outline

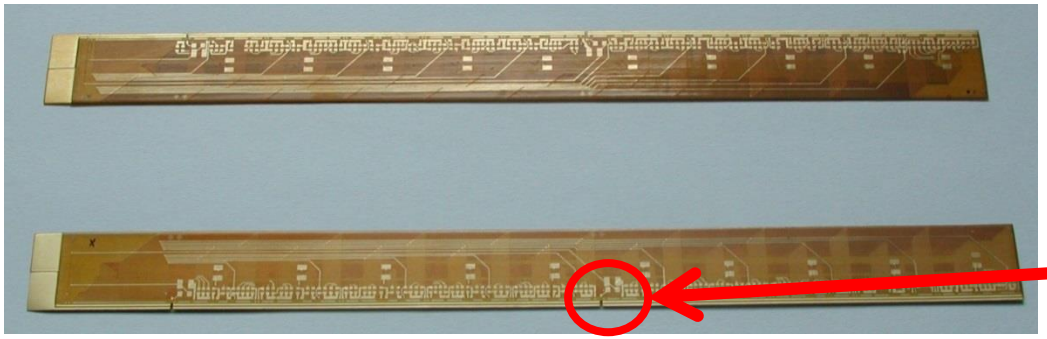
- Aluminum circuits
  - Material budget /General possibilities
  - Vias/Micro-vias
  - Finishing possibilities
  - Different examples
- Wire bonding alternatives
  - Embedded active devices

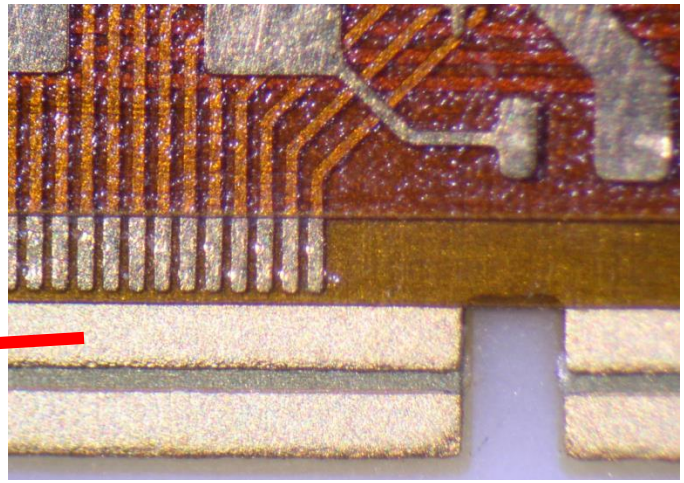
Al double Sided flex with plated through Holes



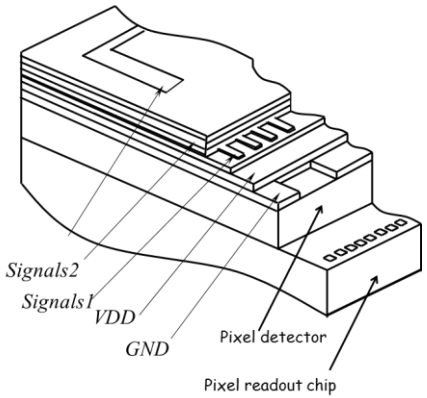
Via : 300um
Double sided
2x 30um Vacuum deposited aluminum
200um line and space
25um Kapton support
Size 300mm x 20mm
NI/AU finishing

5 layers ALICE Pixel Bus





Via : 100um
5 Aluminum layers
3x10um Vacuum deposited aluminum
2x50um laminated aluminum layer
100um line and 50 space
12um Kapton layers
Size 160mm x 16mm
Staircase shape on one side
170 buses produced
NI/AU finishing



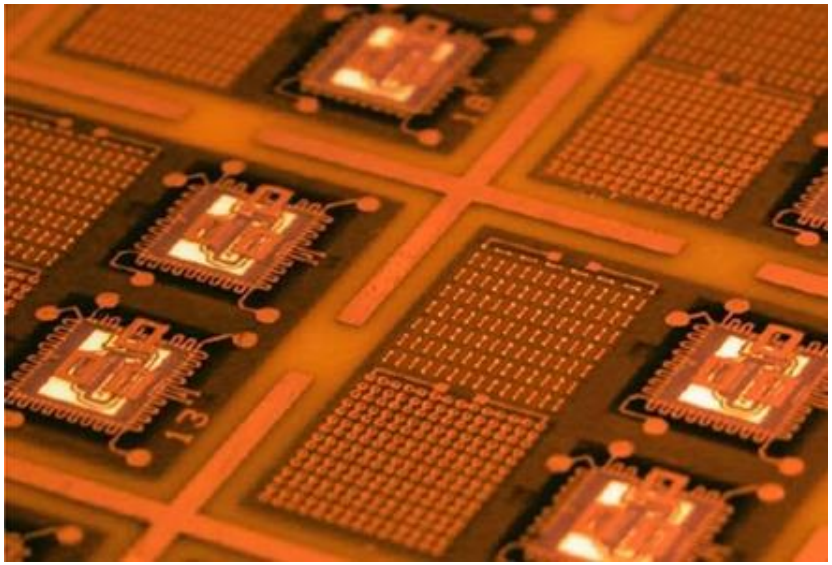
8 layer ATLAS IBL Al/Cu mixed multilayer

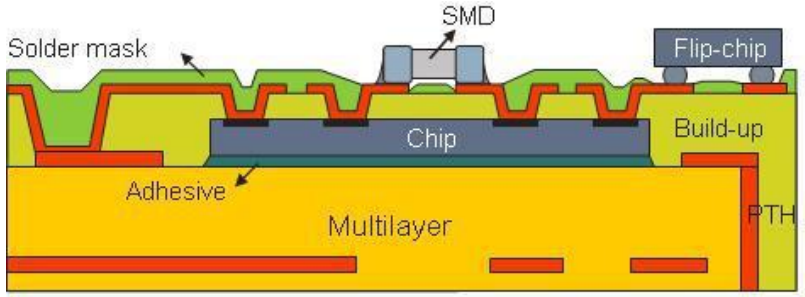
Via min : 300um
5 Copper layers
2x50um laminated aluminum layer
70um line and 50um space
25um Kapton layers
Size 400mm x 20mm
Semi flex rigid structure
Rigidizers near connectors
100 buses produced
Milli-ohms level resistivity check
200 to 300 Mrad compatible
NI/AU finishing

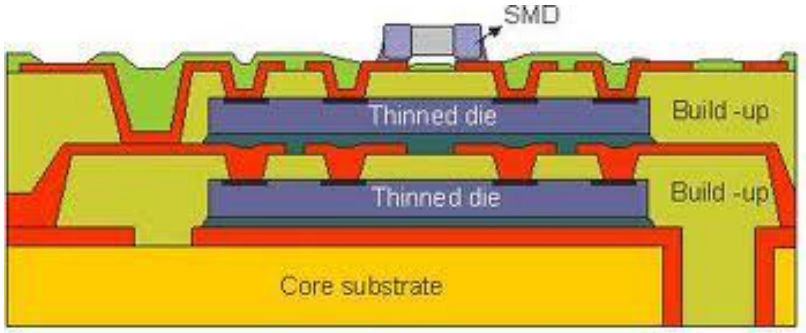
outline

- Aluminum circuits
  - Material budget /General possibilities
  - Vias/Micro-vias
  - Finishing possibilities
  - Different examples
- Wire bonding alternatives
  - Embedded active devices

Embedded Chip situation in industry

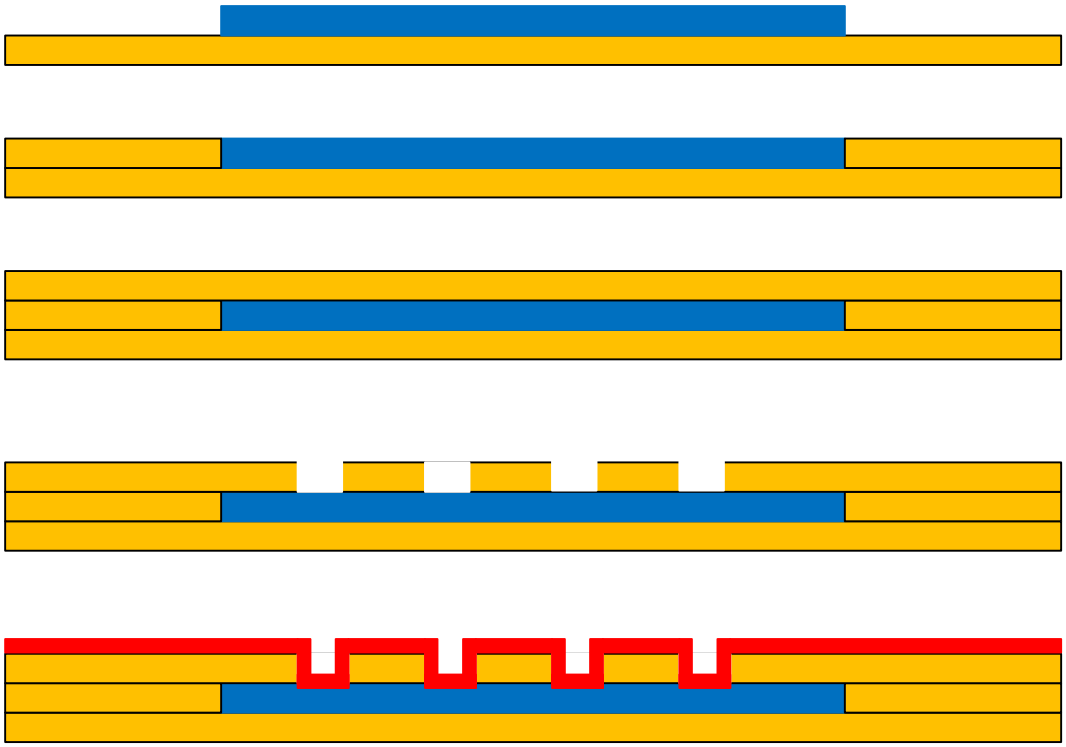






Laser micro-vias
Thick copper pads on chip (15um)
100um vias
100%compatible with PCB production line
RCC glues
Thick or thin chip

Embedded Chip situation at CERN



Glue the chip on 25um kapton
180deg, 1h ,20 bars under vacuum

Compensate the Chip thickness
180deg, 1h ,20 bars under vacuum

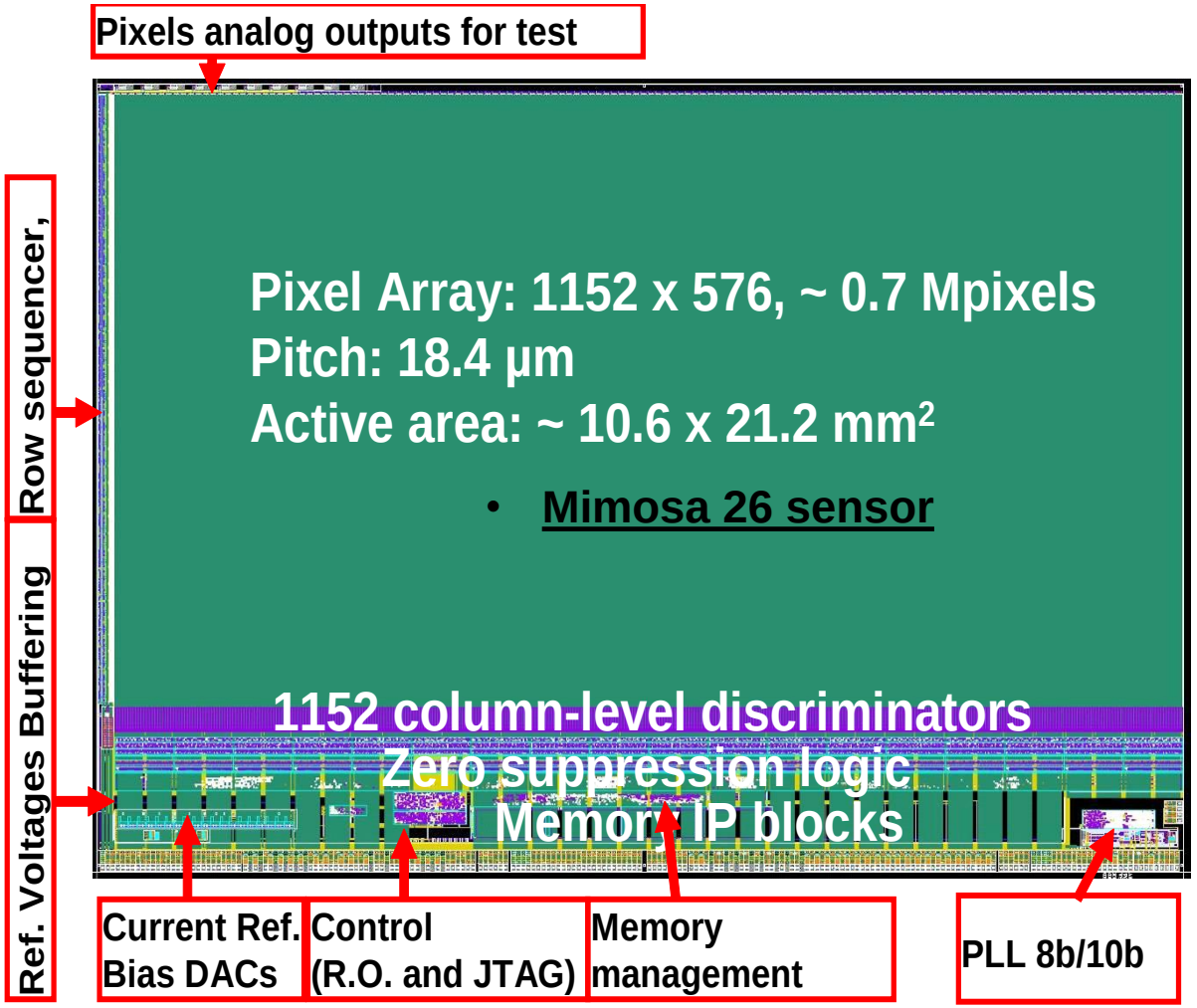
Glue a new layer of 25um
180deg, 1h ,20 bars under vacuum

Chemical hole etching

Vacuum Aluminium plating

The 3 last steps can be repeated for multilayer AL interconnection

Embedded Chip at CERN

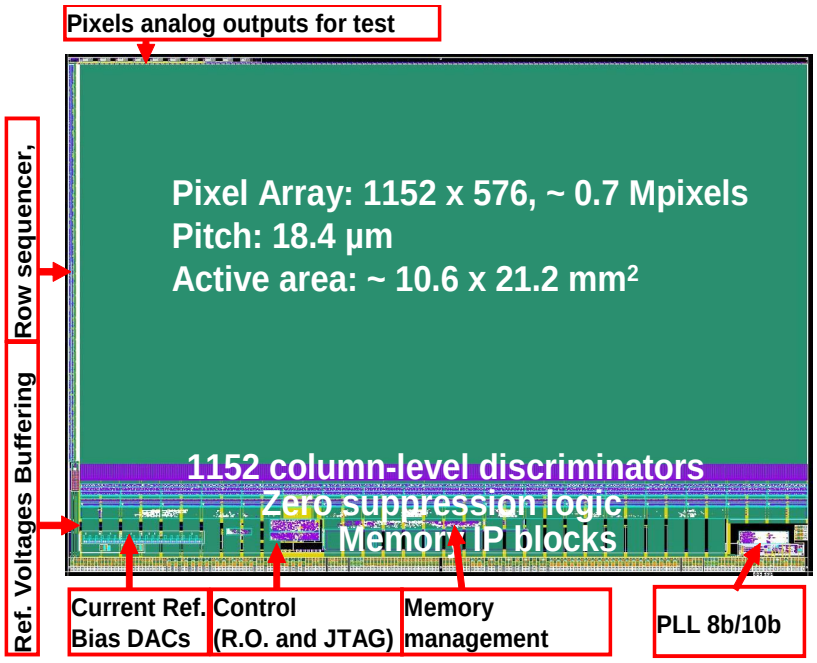


Bonding pads:
Shape : square 80um
Pitch : 100um
Position : peripheral
Pad metal: Al

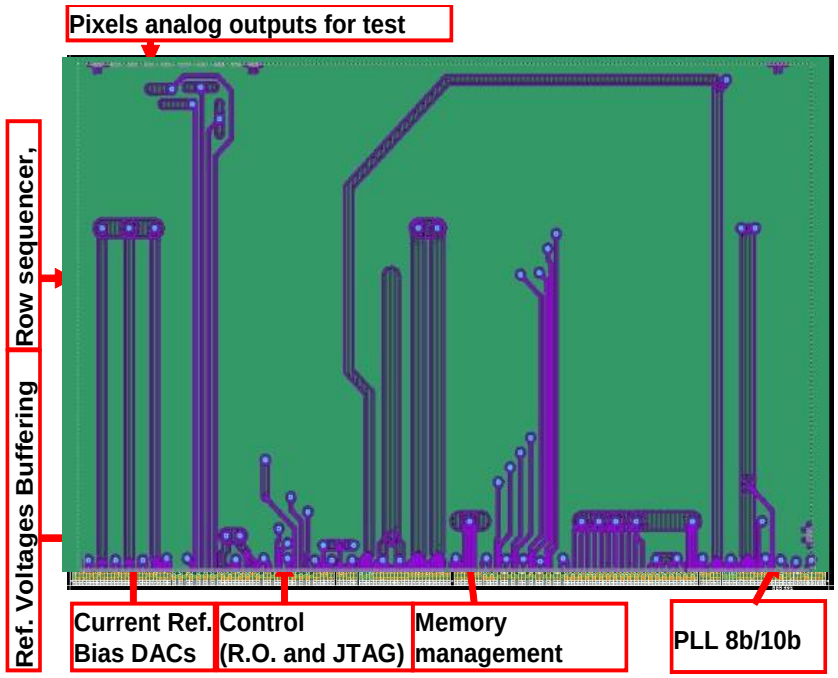
Chip thickness: 50um

Chip not flat

Mimosa 26 sensor

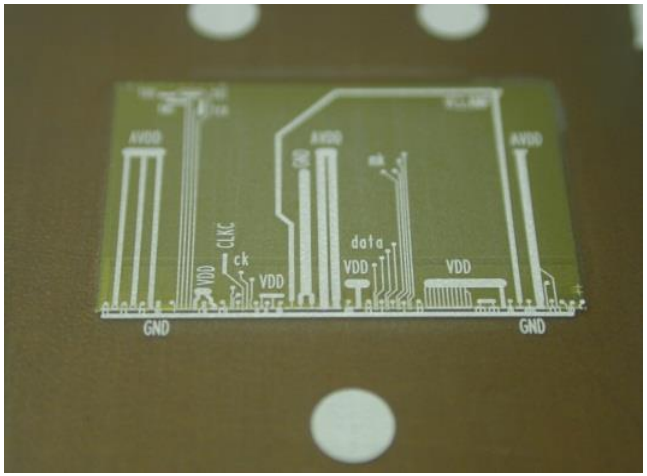


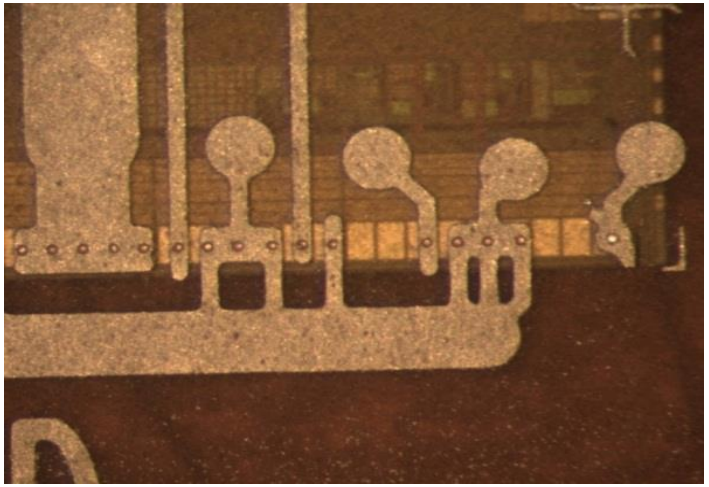
Layout & block diagram



redistribution layer

Embedded Chip at CERN





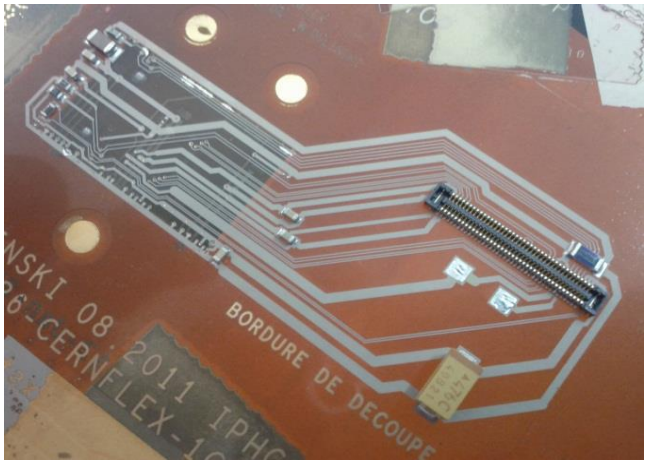
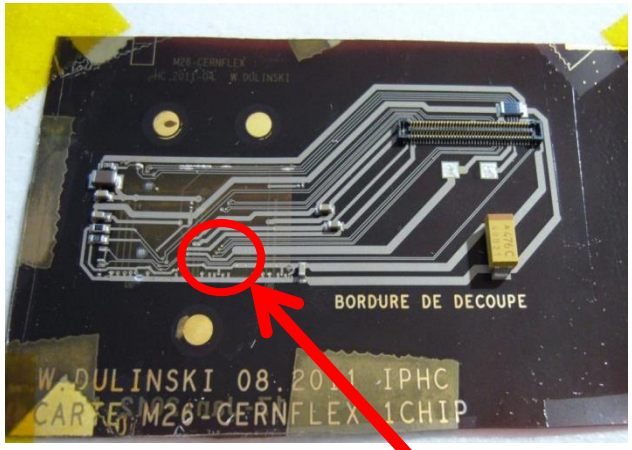
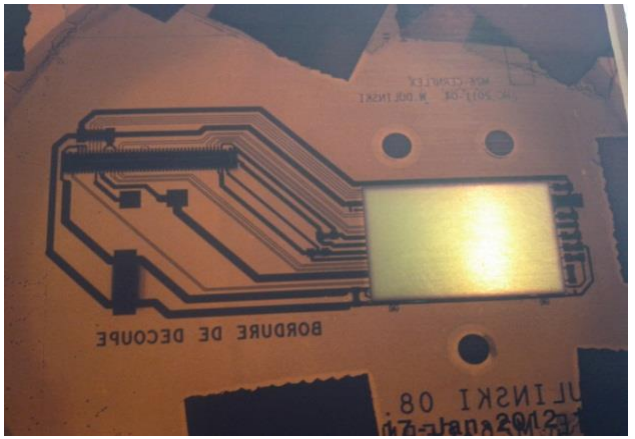
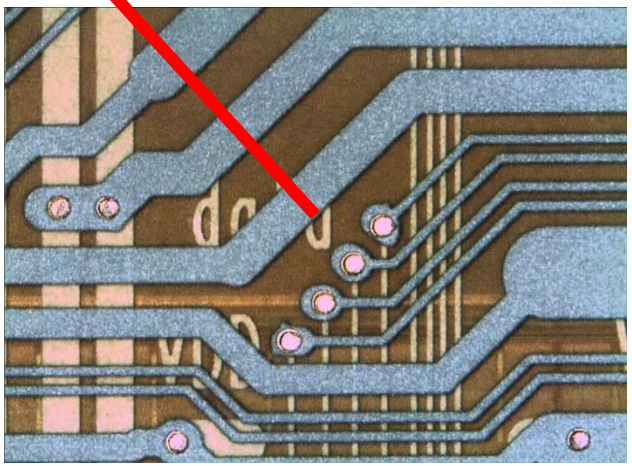


Photo imaged micro-vias
Std aluminum pads on chip (no post process)
40um micro-vias
2 Aluminium layers
No copper
Thinned chip 50 um
Ni/Au plating on the connectors
Mimosa chip
Made in collaboration with Mr Dulinski

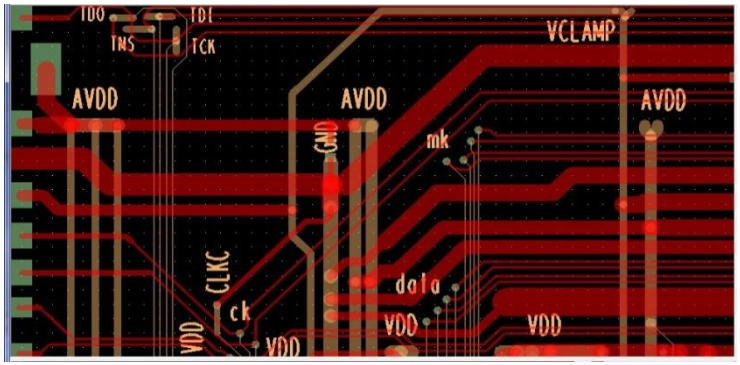
Embedded Chip at CERN



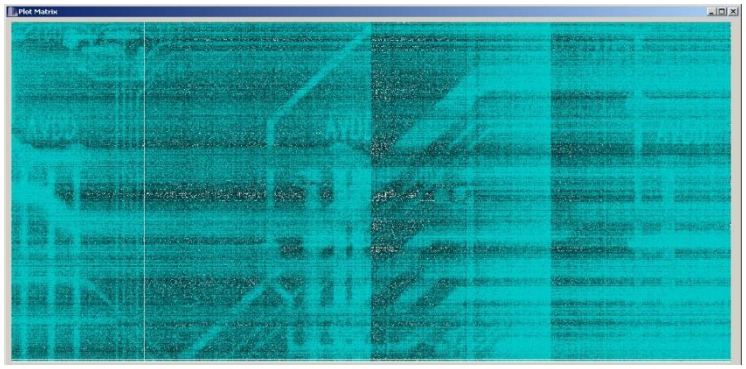




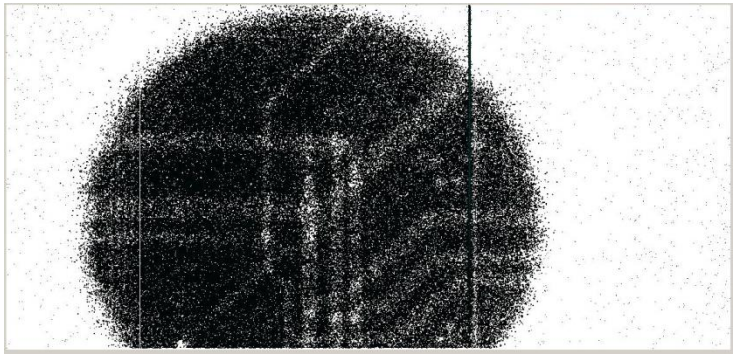
Results



Lithography details of interconnecting metal (two layers of ~10 µm thick Al) deposited on top of the pixel sensor

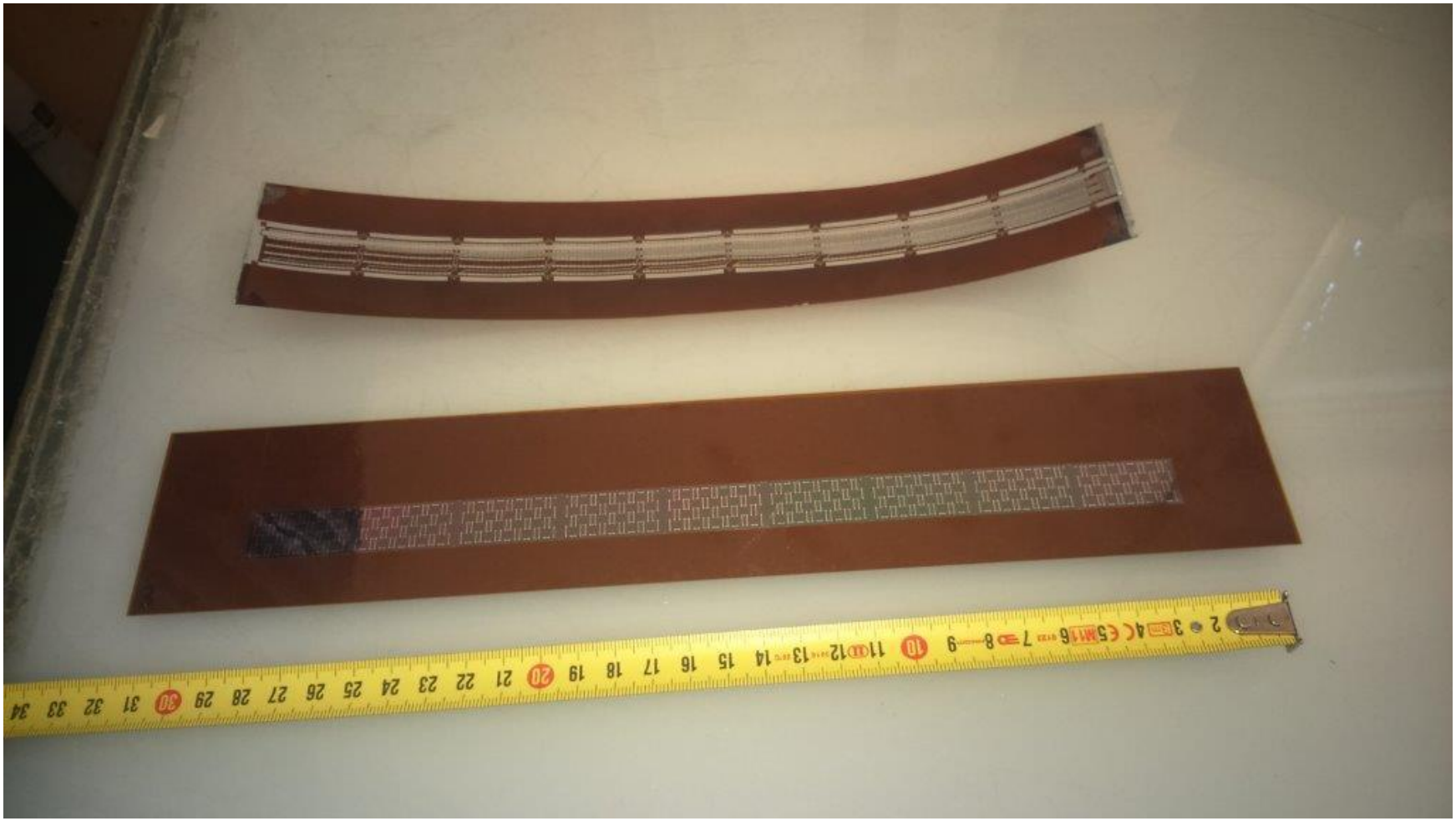


"Shadow" of metal measured by pixel sensor in visible light

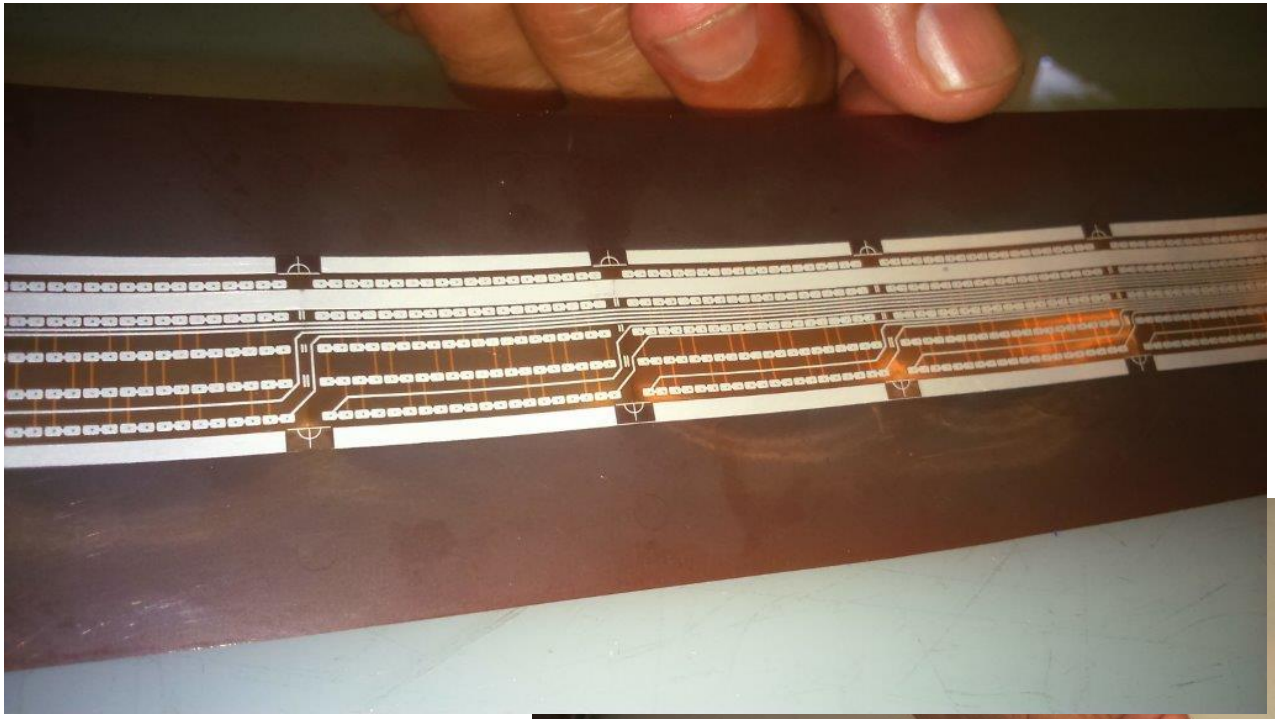


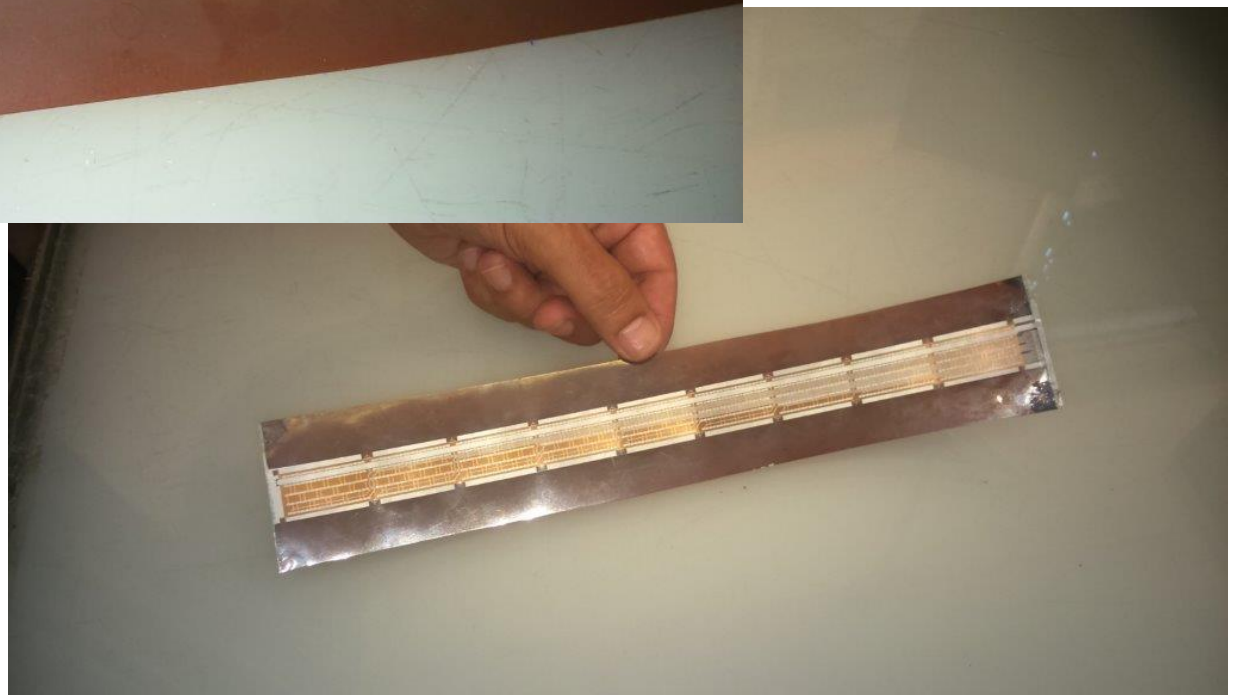
Auto-radiography of metal measured by pixel sensor using 5.9 keV Xrays (^{55}Fe)

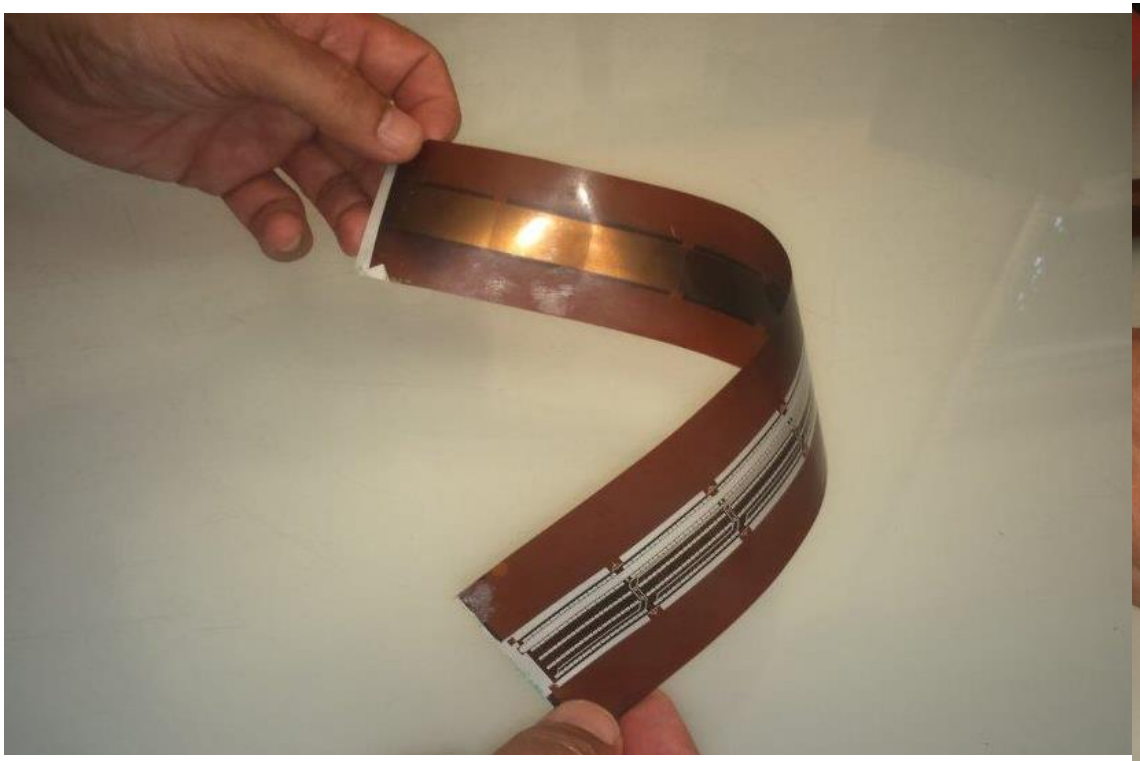
9 chips

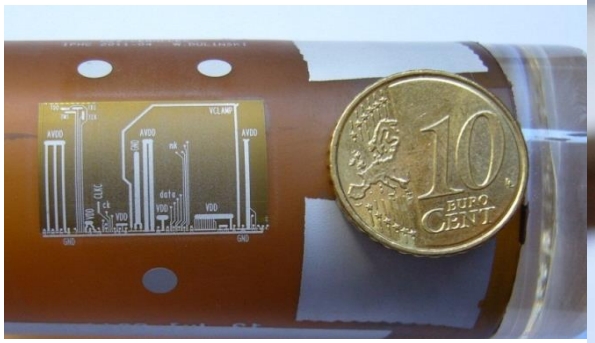


Daisy chain chips structure





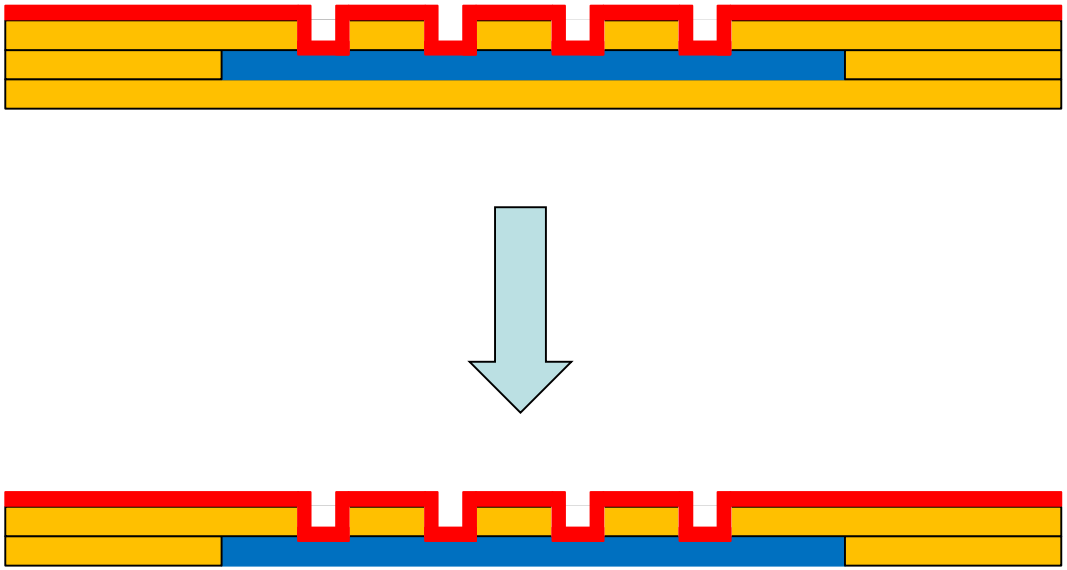



10
EURO
CENT

Problems or things to be tested

- Chip/Kapton CTE mismatch creating small bowings
- Test a room temp epoxy to avoid bowings
- Test a 2 layer metal above chips
- Test a back-kapton-less structure

Back-Kapton-less structure



Positive things

- Already positive results after only 3 trials
- Direct Al to Al contact
- No assembly , no soldering , no bonding
- Flat structure
- Flexible
- Low mass

Future

- Do gluing tests with room temperature glues
- Build new 9 chip Embedded structure if chips available
- Radiation /Climatic /electrical test.