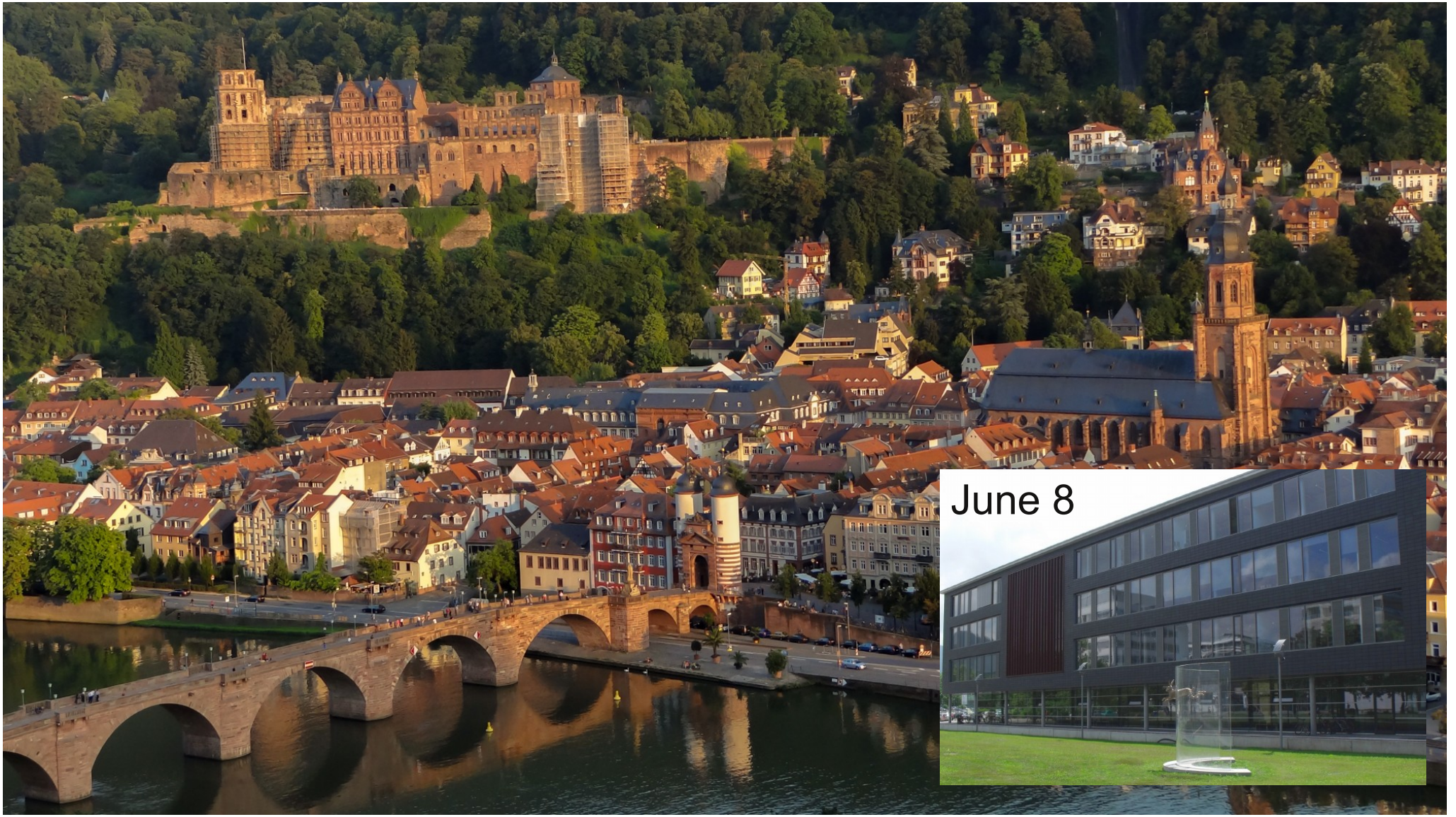
Summary of 1st ATLAS-HVMAPS Workshop in Heidelberg



Workshop Summary

- About 45 participants in person/Vidyo
- 5 sessions:
  - HV-MAPS Chip Designs and Results
  - Mu3e Pixel-Lab Tour
  - Radiation Hardness and Irradiation Results
  - Modules, Data Transmission and Trigger
  - HV-MAPS Organisational Matters

Goals of Heidelberg workshop:

- get overview about (monolithic) HV-CMOS designs
- overview of relevant measurements (e.g. irradiation results)
- discussion of feasibility and possible applications in ATLAS (e.g. 5th+6th layer)
- discussion about next steps → **HV-MAPS demonstrator(s)**

Will not repeat everything said and shown in Heidelberg

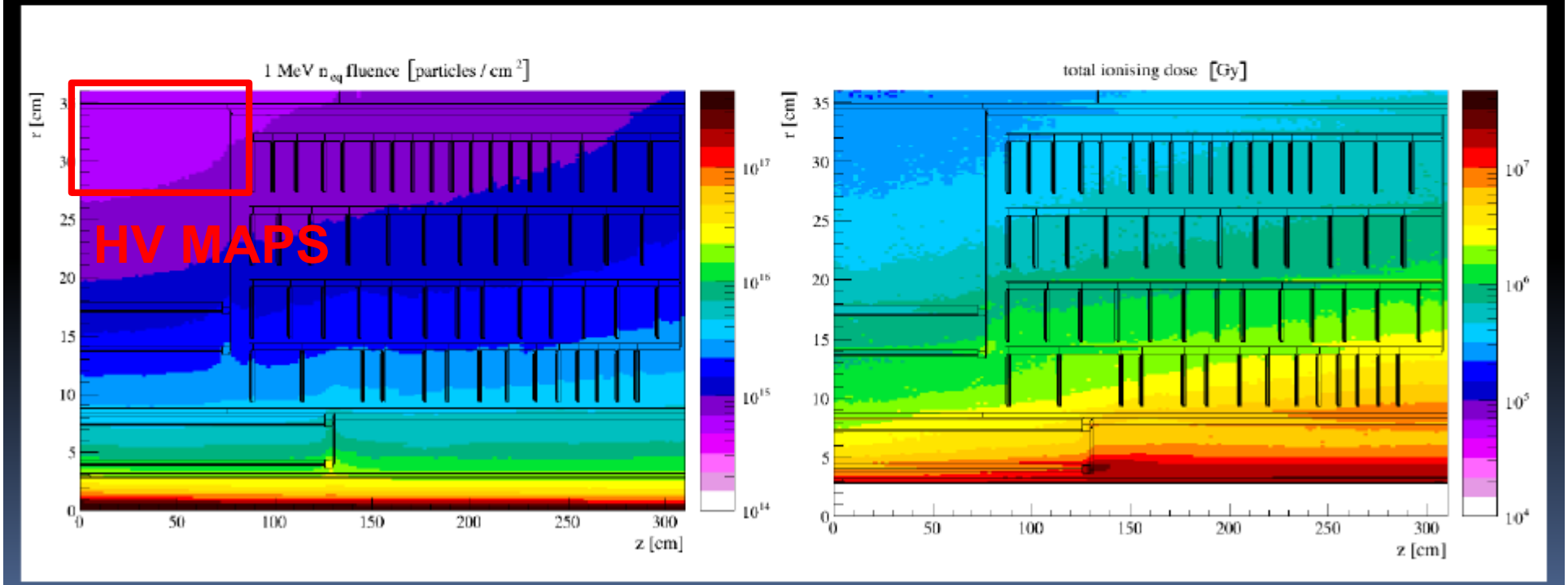
slides are available from Indico:

https://indico.cern.ch/event/393212/

Expected doses

Layer 5/6 are in a relatively quiet environment:

- 5-7 10^{14} 1 MeV n_{eq}
- 30-50 Mrad



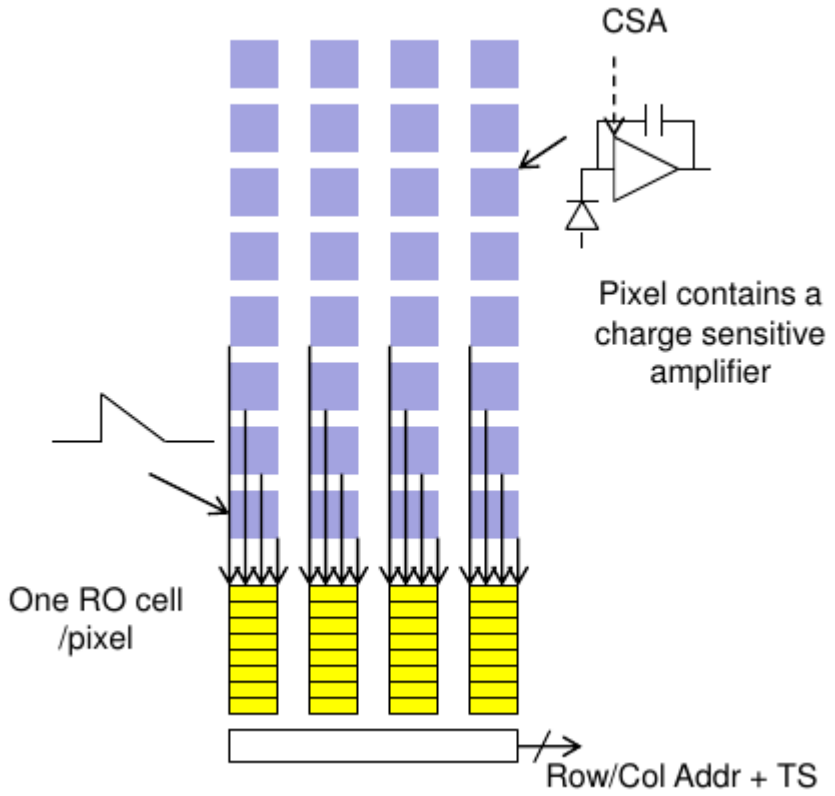
Readout requirements

Need to verify with new simulations. Present estimates, mainly LoI based, at 1 Mhz LVLo readout are:

	R	Hit rate	Raw data rate	BW per FE chip
Layer 1	4 cm	2 Ghit/(s*cm²)	2.7 Gb/s	5 Gb/s
Layer 2	8 cm	820 Mhit/(s*cm²)	1.1 Gb/s	2 Gb/s
Layer 3	14 cm	400 Mhit/(s*cm²)	520 Mb/s	1 Gb/s
Layer 4	20 cm	250 Mhit/(s*cm²)	350 Mb/s	640 Mb/s
Layer 5	30 cm	150 Mhit/(s*cm²)	200 Mb/s	480 Mb/s
Layer 6	34 cm	120 Mhit/(s*cm²)	170 Mb/s	320 Mb/s

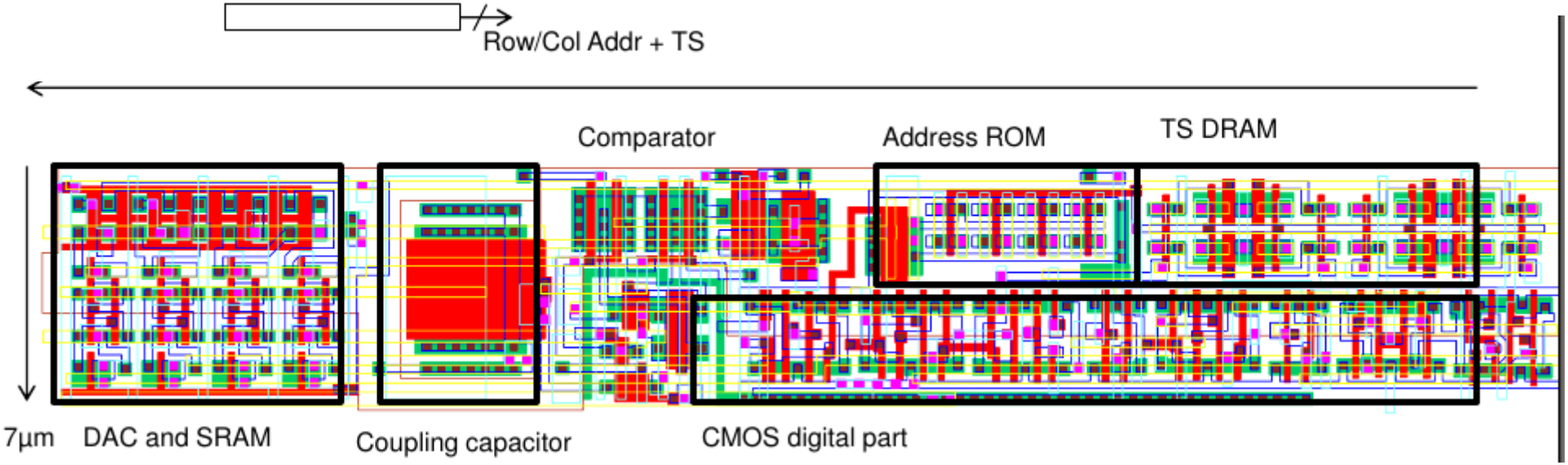
The difference between the raw data rate and the requested BW is to limit transmission latency for track trigger.

HV-MAPS Readout Architectures (Ivan)



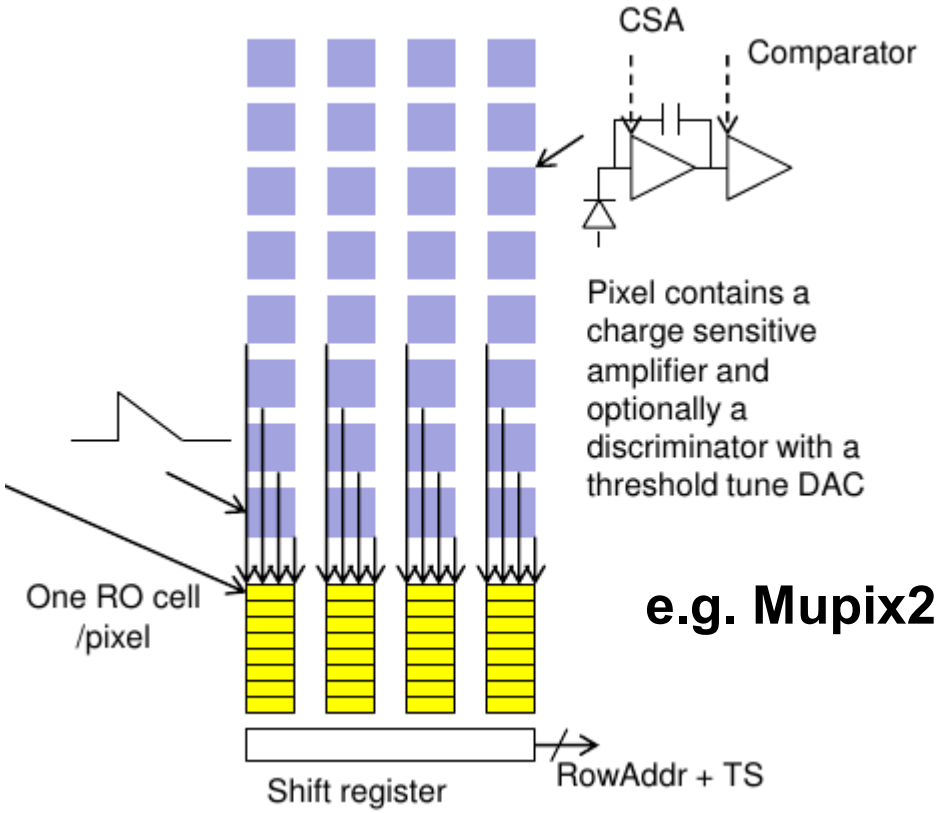
e.g. Mupix7 Design

Hit Digitisation in Periphery

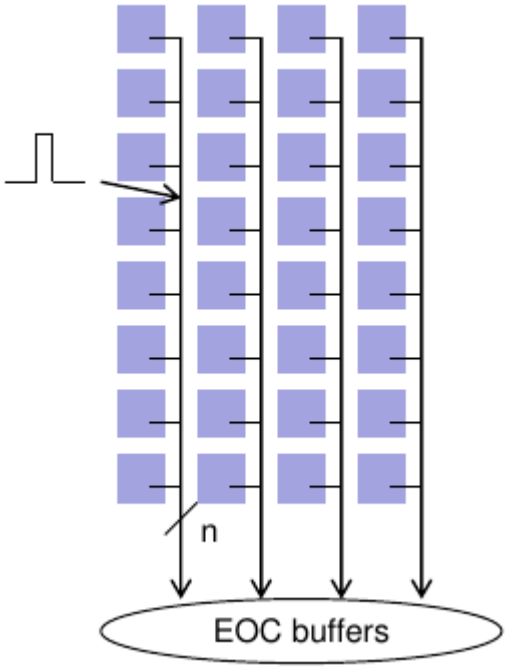


HV-MAPS Readout Architectures (Ivan)

options with comparator in cell



e.g. Mupix2 Design



- **cell-to-periphery lines**

- **in-pixel address**
- **small periphery!**
- **also other alternatives**

hit encoding would also allow small pixel sizes

HV Demonstrators

Eva Vilella (KIT, Geneva, Liverpool):

different layouts in one chip: CMOS/NMOS comparators, analog/digital pixels,different gains, timewalk corrections, test structures.

Raimon Casonova Mohr (Barcelona, KIT):

150x 16 pixels, size 250 x 50 mu^2, priority NAND-NOR scheme, 320 Gbit/s serial link.

Angelo Dragone et al. (SLAC, Bonn):

COOL (LFaundry 150nm), full depletion at 2kOhm, preliminary architecture, 250 x 50 mu^2.

Herve Grabas (UCSC,SLAC,KIT):

CHESS Chip for “strip layers”: 40 x 800 mu^2 “pixels”, strip hit encoding, SLAC ASIC Control IF (SACI); CHESSII design review currently ongoing

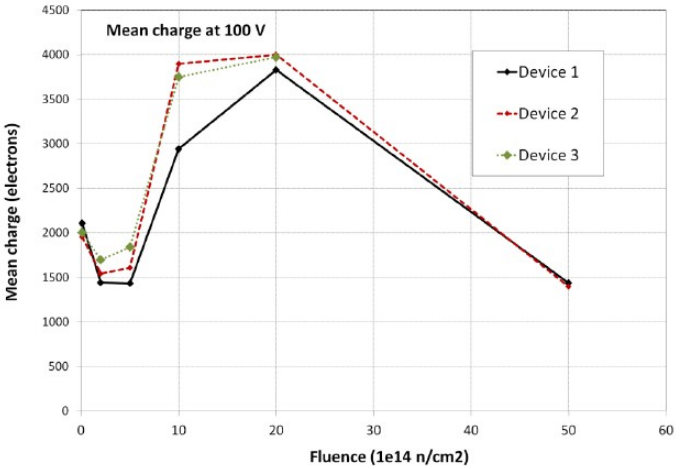
→ several groups want to test different substrates (20-1000 Ohm)

Irradiation Results

Igor Mandic:

Results from CHESS1 (H35) and CCPD (H18); E-TCT results and charge collection results:

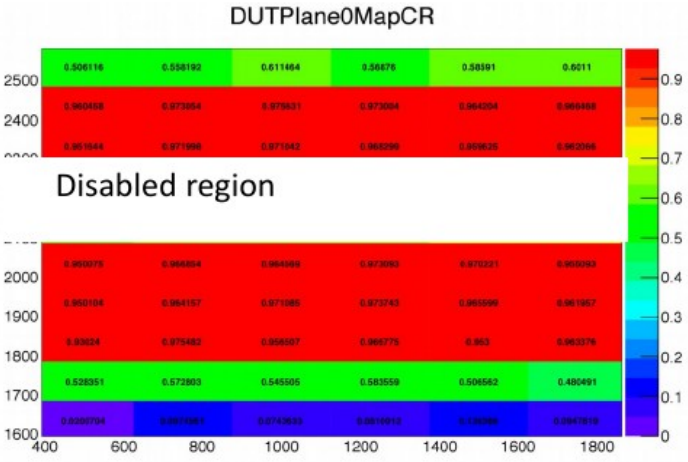
- depletion area increases for fluences up to 2E15 n/cm²
- drop of collected charge above 2E15 n/cm²



Mareon Barbero et al.:

CCPD (HV2FEI4) sensor in AMS H18:

- Xrays: radiation hard up to ~900 Mrad
- efficiency measurements (before vs. after)
- timing measurements



Modules, Data Transmission, Trigger

Modules: Fabian Hügging

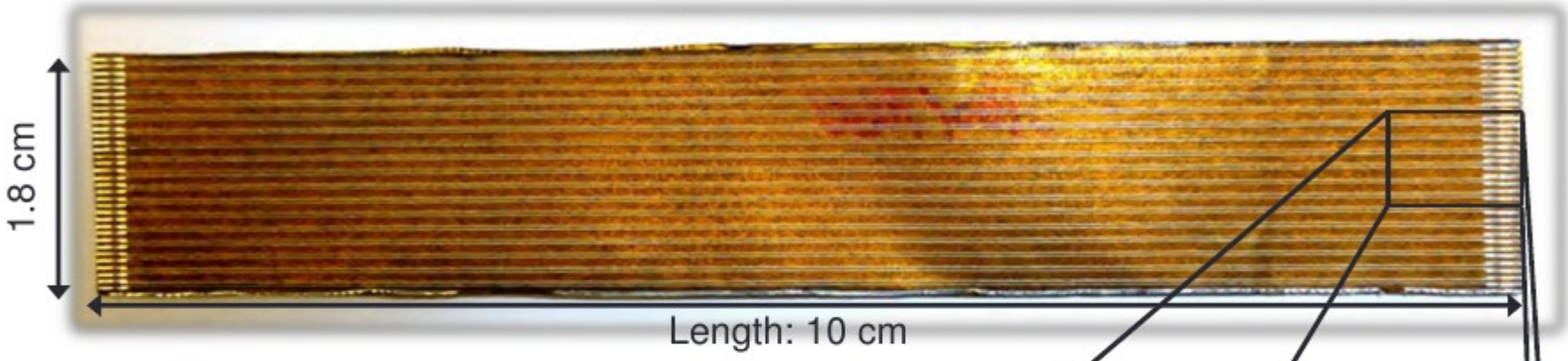
Conclusions

universitätbonn

- Module design for the ITk pixel detector is constraints by many external factors beyond radiation levels, data rates and readout speed:
  - magnitude of module production requires a good testability, robustness and disfavors a large variation of module types
  - cooling, powering and loading requirements are important to understand inside the whole system
- For monolithic CMOS detectors many things are similar as for hybrid pixel modules:
  - benefit from solutions being developed now for hybrid by just copying them
  - but in the end all these issues must be addressed as well in time!
- For charge coupled CMOS detectors things could be quite different depending on the chosen option:
  - this may complicate life because one have to develop own solutions

Data Transmission: Sebastian Dittmeier

Flex print prototypes



- 25 µm Kapton + 12 or 25 µm Aluminum
- Laser evaporation and cutting
- Ground plane
  - 25 µm Kapton + 12 µm Al
  - Reduce crosstalk
  - Enhance impedance
- Lengths up to 1m produced
- Current system: structures ~ 100 µm

Width: 100 µm Separation: 150 µm
Between pairs: 650 µm

Error-free data transmission possible (tested up to 1.6 Gbit/s)

Track Trigger: Richard Brenner

Results SSW=64 (5/5)

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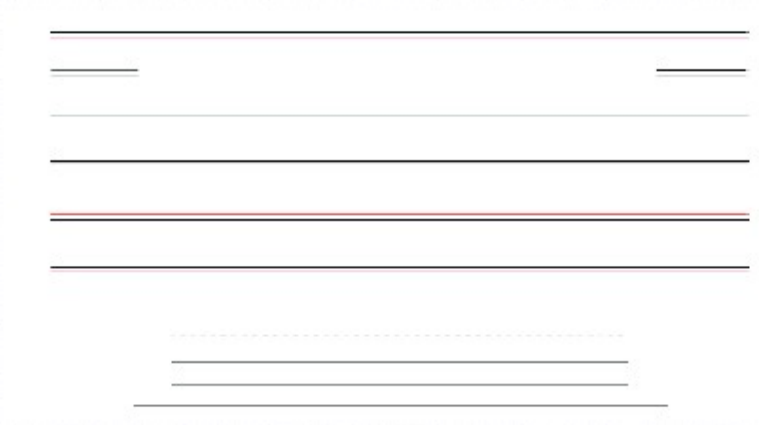


Strip layers: [4,13]

Pixel layers: [0,3]

layers	N patterns	Efficiency	N matched μ160	Layers
4s1p max L	1M	99.60%	12.23	[0,5,8,12,13]
4s1p ext. strip	0.66M	99.68%	30.89	[3,5,8,12,13]
3s2p max L	1.3M	93.14%	10.84	[(0,3,5,8,13]
3s2p ext. strip	0.7M	99.61%	79.39	[2,3,5,8,13]

Efficiencies for 5/5 → layout inefficiencies
Will improve with wild cards

Richard Brenner – Uppsala University 17/(18) ATLAS HV-MAPS WS 8 June 2015

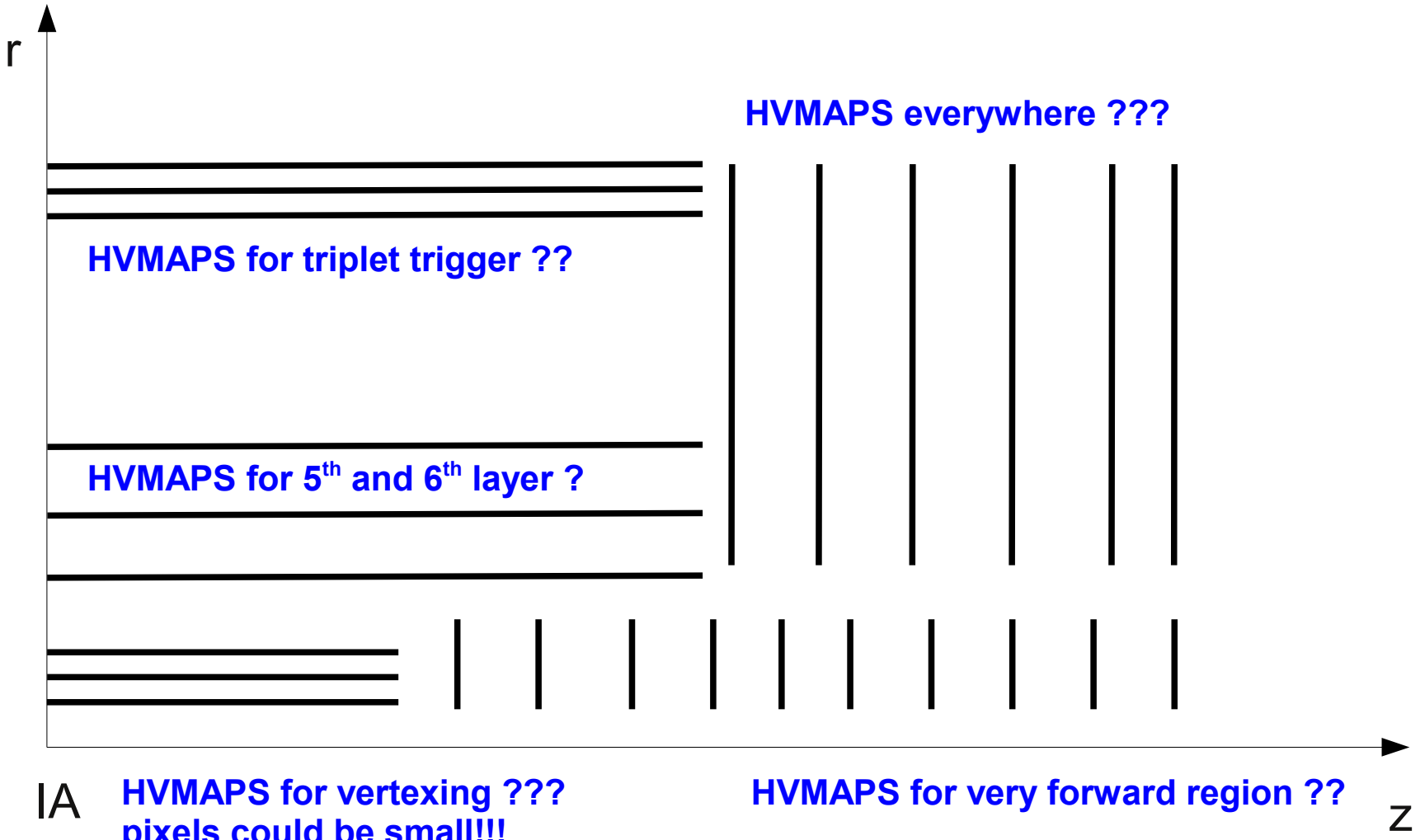
Final (Short) Discussion

Following work packages are suggested:

- HV-MAPS design
- readout
- services
- mechanics
- tracker layouts
- track-trigger
- physics simulation and performance

→ expertise from many areas required!

- should avoid too many incoherent layouts
- concentrate on a few layouts (→ detector regions) and demonstrators (matched to different requirements)
- No discussion about milestones and detailed timelines in Heidelberg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HVMAPS everywhere ???
HVMAPS for triplet trigger ??
HVMAPS for 5th and 6th layer ?
IA
HVMAPS for vertexing ???
pixels could be small!!!
HVMAPS for very forward region ??
z

This Workshop

specifications: get a clearer pictures on requirements for HV-MAPS

tracker layout: what layout and what are the relations (impacts) between layout and sensor technology

HV-MAPS designs: converge to only few projects

Modules and Services: better understand system aspects and how HV-MAPS can be integrated into the ATLAS tracker