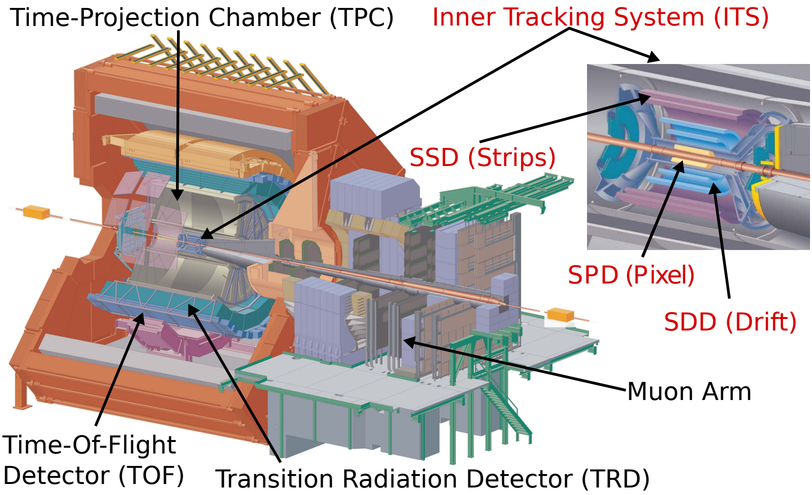
Upgrade of the ALICE ITS

Markus Keil (CERN)

Outline

Outline

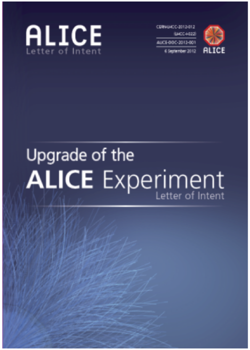
ALICE and the Current ITS



- ALICE is the heavy-ion focussed experiment at the LHC with the main goal to study strongly interacting matter

ALICE Upgrade Strategy

- Motivation: Focus on high-precision measurements of rare probes at low p_{T}
  - Cannot be selected by hardware trigger
  - Need to record large sample of events
- Goal: Pb-Pb recorded luminosity $\geq 10\,\mathrm{nb}^{-1}$ (Plus: pp and p-Pb data)
  - Gain of factor 100 in statistics for minimum bias
- Strategy: Read out all Pb-Pb interactions up to the maximum LHC collision rate of 50 kHz
- When: 2nd long LHC shutdown LS2 (2018/19)

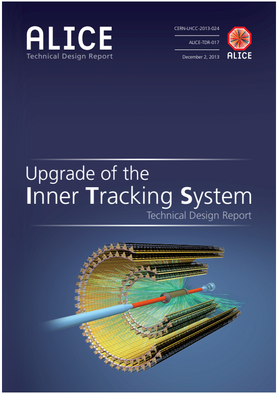


ALICE Upgrade Strategy (2)

- Upgrade of the Silicon Trackers
  - New high-resolution, low-material inner tracking system (ITS), covering mid-rapidity
  - New muon forward tracker (MFT) covering forward rapidity (silicon pixel telescope in front of the hadron absorber, in the acceptance of the muon spectrometer)
- Further Upgrade Items
  - New, smaller beam pipe
  - TPC: replacing of readout planes and electronics
  - Upgrade of forward trigger detectors (FIT) and ZDC
  - Upgrade of readout electronics of: TRD, TOF, PHOS and Muon Spectrometer
  - Upgrade of Online and Offline Systems

ITS upgrade

- Main goal: replacement of ALICE Inner Tracking System (ITS) during LHC long shutdown II in 2018–2019
- Design objectives:
  - **Increased spatial resolution:**
    - $\lesssim 5\,\mu\text{m}$ in longitudinal and transverse directions
  - **Closer to interaction point:**
    - move to $r = 23\,\text{mm}$
  - **Reduced material:**
    - aiming at $\lesssim 0.3\,\%\ X_0$ for innermost layers
    - additional benefit from thinner beam pipe
  - **Increased readout speed:**
    - Record 50 kHz Pb–Pb collisions (minimum bias)



CERN-LHCC-2013-24
fully approved

ALICE

ITS upgrade

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J. Phys. G **41** 087002

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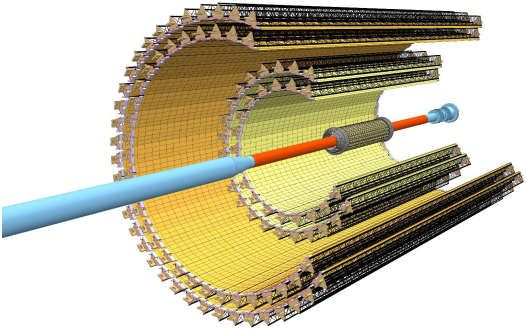
Outline

Layout of the Upgraded ITS

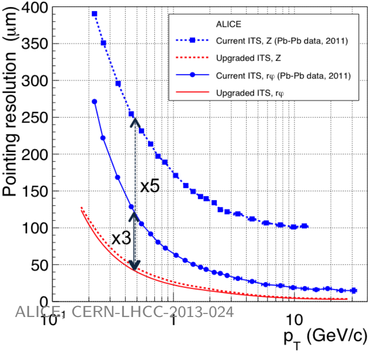


- 7 layers from r=22 mm to r=400 mm
- $\sim 10\,\mathrm{m}^2$ of silicon
- 12.5 GPixels

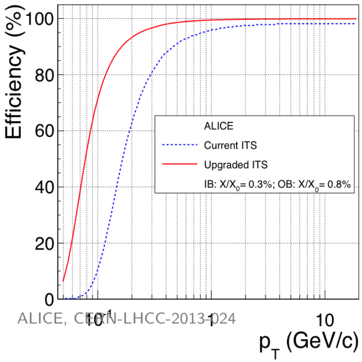
- Moderate radiation hardness required (at 30°C), expected radiation levels (innermost layer, safety factor of 10):
  - 2700 krad (TID) and $1.7 \times 10^{13}\,1\,\mathrm{MeV}\,\mathrm{n_{eq}cm^{-2}}$
- η coverage: $|\eta| \leq 1.22$, for tracks from 90% most luminous region

Expected Performance

- Expected improvement of impact parameter resolution (left) and tracking efficiency (right).



ALICE, CERN-LHCC-2013-024



ALICE, CERN-LHCC-2013-024

Outline

Choice of Sensor Technology

Requirements (TDR):

Parameter	**Inner barrel**	**Outer barrel**
Silicon thickness	50µm	
Spatial resolution	5µm	10µm
Power density	< 300 mW/cm^2	< 100 mW/cm^2
Event resolution	< 30µs	
Detection efficiency	$> 99\%$	
Fake hit rate	$< 10^{-5}$ per event per pixel	
TID radiation *	2700 krad	100 krad
NIEL radiation *	$1.7\text{x}10^{13}$ 1 MeV n_{eq}/cm^2	10^{12} 1 MeV n_{eq}/cm^2

* Including a safety factor of 10, revised numbers w.r.t. TDR

- Very **thin sensors**
- Very **high granularity**
- **Large area** to cover
- **Modest radiation levels**

$\Rightarrow$ **Monolithic silicon pixel sensors**

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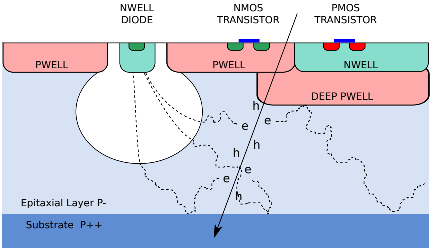
Pixel Chip Technology

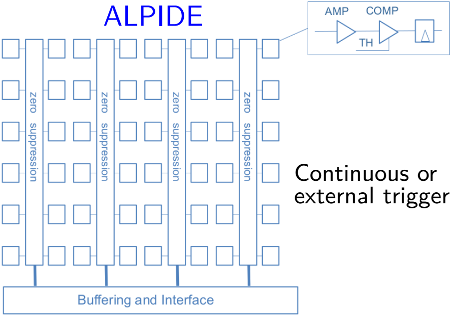


Monolithic active pixel sensors in TowerJazz 0.18 μm CMOS imaging process

- High-resistivity epitaxial layer on p-substrate
- Quadruple well process: deep pwell shields PMOS transistors, allowing for full CMOS circuitry within active area
- Application of (moderate) bias voltage to substrate can be used to increase depletion zone around NWELL collection diode

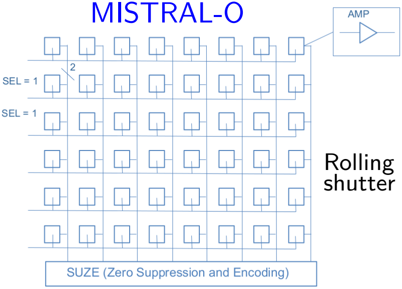
Chip architectures

ALPIDE



Continuous or external trigger

MISTRAL-O



Rolling shutter

- Readout: Data driven sparse readout
- Pixel pitch: 28µm x 28µm
- Event time resolution: $\lesssim$ 2µs
- Power consumption: $\sim$ 40 mW/cm^2
- Dead area: 1.1 mm x 30 mm

- Rolling shutter
- 36µm x 65µm
- $\sim$ 20µs
- 80 – 90 mW/cm^2
- 1.5 mm x 30 mm

- Baseline solution is the ALPIDE
- Both chips have the same dimensions, identical physical and electrical interfaces

The ALPIDE Development Program

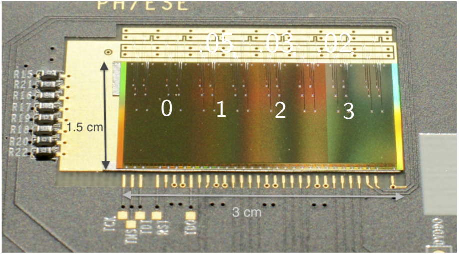
2012	Explorer-0
2013	Explorer-1 pALPIDEss-0
2014 May	pALPIDE-1 pALPIDEss-1 Investigator
2015 April	pALPIDE-2
2015 August	pALPIDE-3
2016 February	ALPIDE

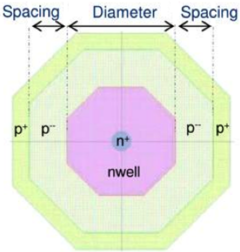
ALPIDE Prototype Generations:

- **Explorer and Investigator:**
  Analog chip to study pixel geometry, starting material and sensitivity to radiation
- **pALPIDEss:**
  Small scale digital chip to study the priority encoder and the front-end electronics
- **pALPIDE-1:**
  Full scale chip to study system effects
- **pALPIDE-2:**
  Full scale chip which supports integration into module prototypes: Supports local bus of Outer Barrel modules

pALPIDE-1

- First prototype with final size (15 mm x 30 mm)
- 512 x 1024 pixels
- Pixel size 28µm x 28µm
- Digital readout with priority encoder
- Four sectors with different pixel layouts

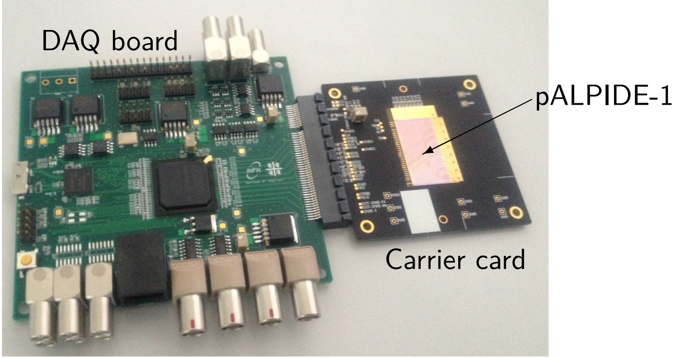




Sector	Nwell diameter	Spacing	Pwell opening	Reset
0	2µm	1µm	4µm	PMOS
1	2µm	2µm	6µm	PMOS
2	2µm	2µm	6µm	Diode
3	2µm	4µm	10µm	PMOS

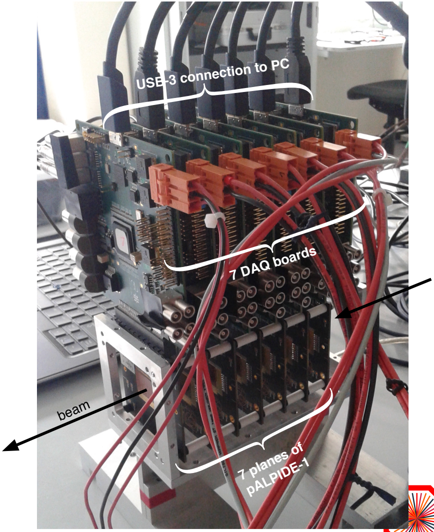
Characterization methods - laboratory

- USB based test system. Performed comprehensive lab measurement program
  - Noise and threshold scans
  - Pulse shape / pulse length
  - Noise occupancy measurements
  - Source measurements
  - For different back bias voltages

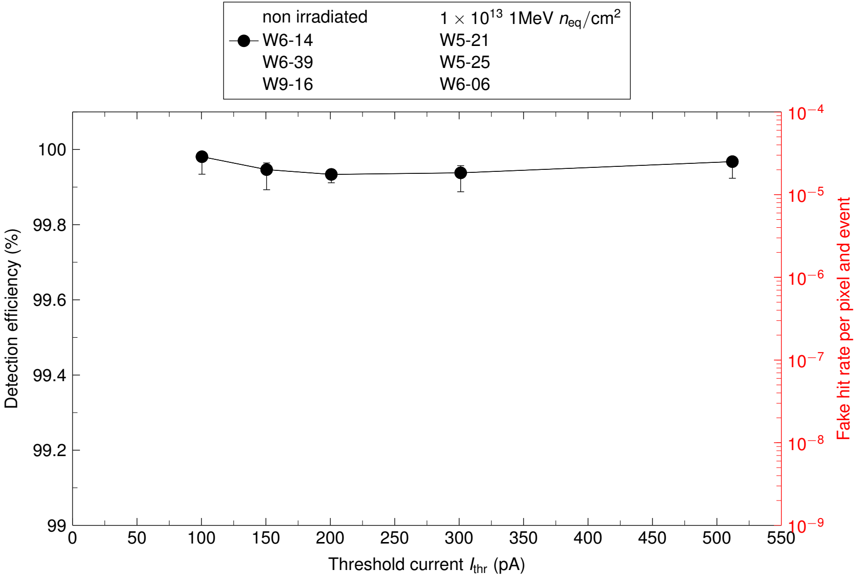


Test beam set-up

- Test beams are carried out using a telescope made entirely of pALPIDE-1
- Extensive campaign with beams at PS, SPS, PAL (Korea), BTF (Italy), DESY (Germany)
- In the following: results with 6 GeV/c π^- from CERN PS
- Tests before and after neutron irradiation



Detection efficiency



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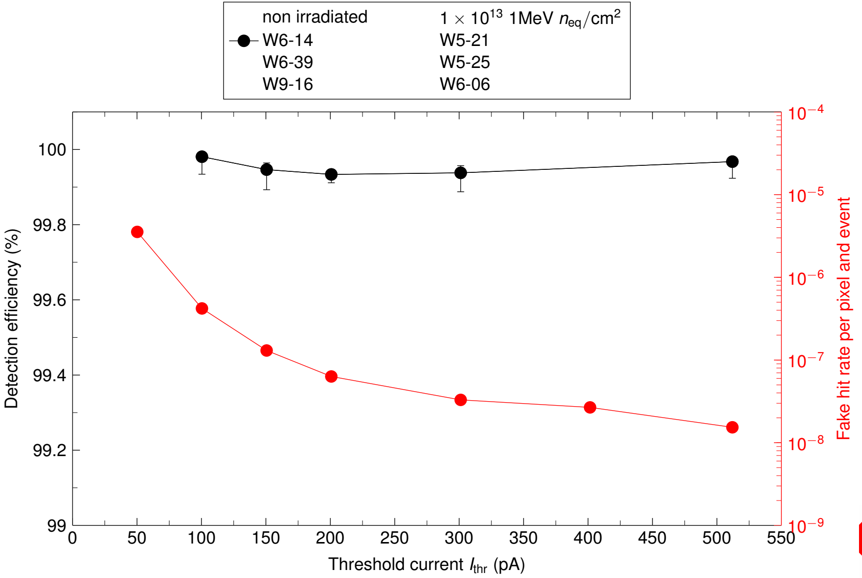
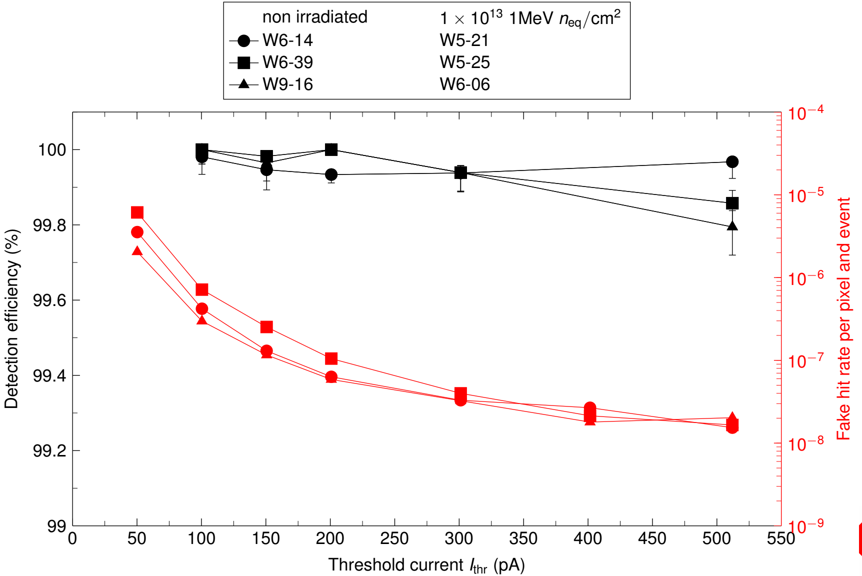


Detection efficiency



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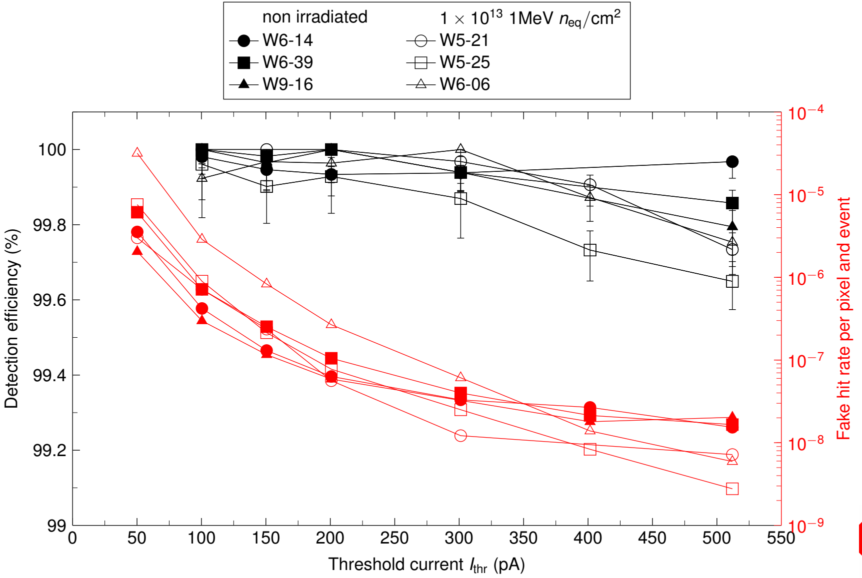
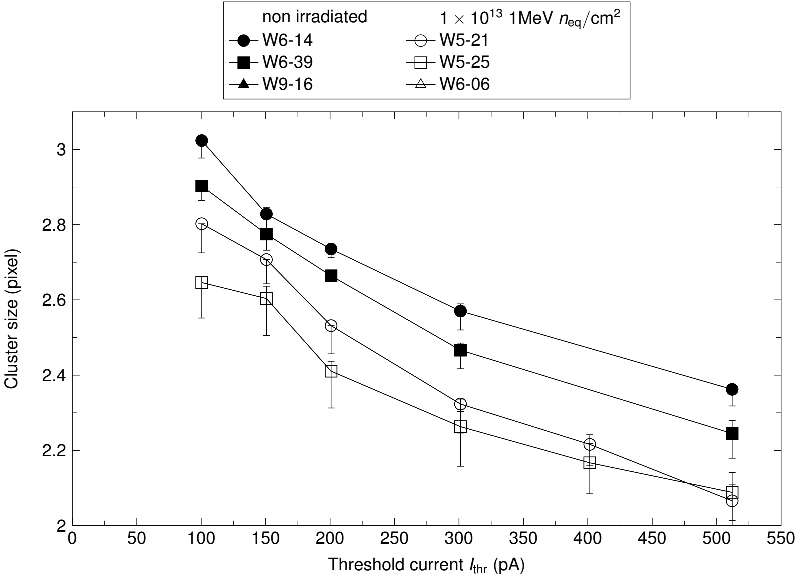
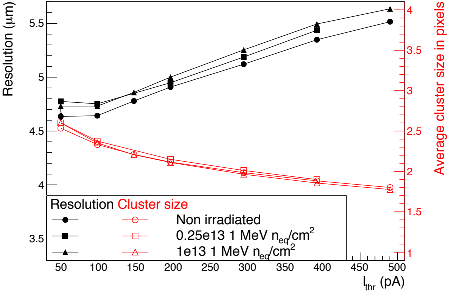


Cluster sizes



Spatial resolution

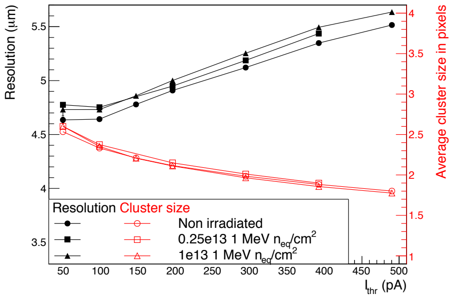
Spatial resolution



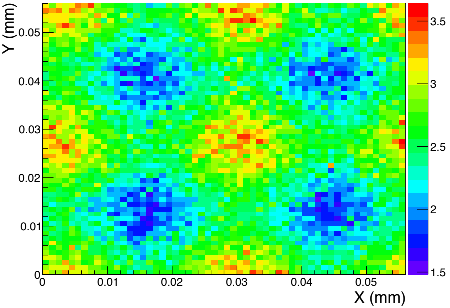
- Average cluster sizes of 1.5–3 pixels
- Spatial resolution of around 4.5 μm to 5.5 μm

Spatial resolution

Spatial resolution



Cluster size

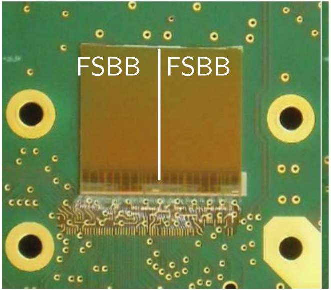


- Average cluster sizes of 1.5–3 pixels
- Spatial resolution of around 4.5 μm to 5.5 μm
- ⇝ Can use telescope tracking to study properties differential in track impinging point
- Cluster size varies nicely leading to good intrinsic resolution

MISTRAL development

MISTRAL FSBB

- First Full Scale Building Block (FSBB)
- Sensitive area: $13.7 \times 9.2\text{mm}^2$ ($\sim$ third of the final chip size)
- Staggered pixels of $22 \times 33\mu\text{m}^2$
- In-pixel pre-amplification and clamping with 6 metal layers
- 416×416 of Columns x Row of pixels ended by discriminator (8-cols with analogue output)
- Double-row readout at 160 MHz clock frequency resulting in 40µs integration time



MISTRAL-O

- Being optimized for the outer layers
  - Target requirements on the spatial resolution: $\sim 10\mu\text{m}$
  - Target requirements on power consumption: $< 100\text{mW/cm}^2$

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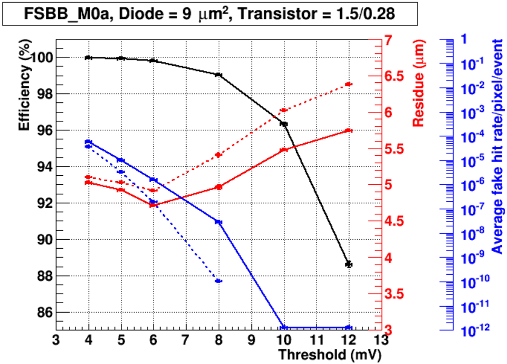
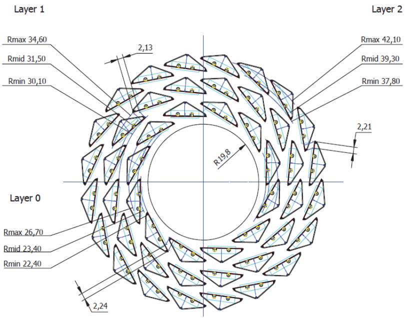
Performance of the MISTRAL FSBB



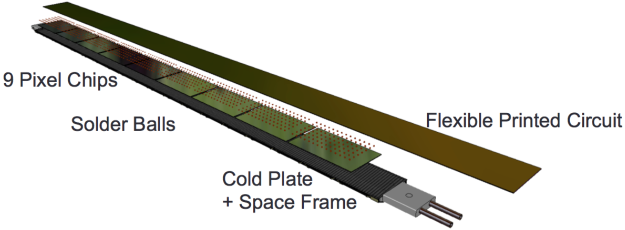
- Large operational margin: 5.0 mV $\leq$ Thr $\leq$ 8.0 mV
- Fake hit rate averaged over 11 sensors
- Fake hit rate drops by O(10) by masking the 20 noisiest pixel
- Tracking resolution is $(4.7 \pm 0.1)\mu$m (U) and $(4.9 \pm 0.1)\mu$m (V) at Thr$=$ 6 mV

Outline

ALICE ITS Inner Barrel



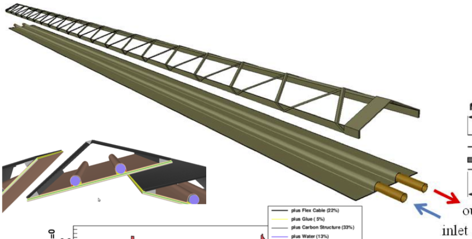
- Three layers, radii: 22, 31, 39 mm
- Length 270 mm
- Nr of staves: 12 + 16 + 20
- 9 chips per stave
- Material budget / layer: $\sim 0.3\% X_0$
- Av. data throughput up to 300 Mbit / s / chip

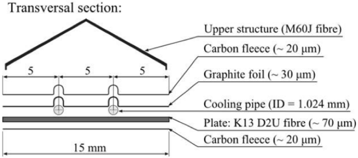


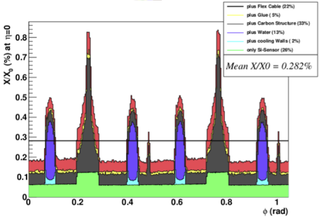
Inner Barrel Stave

Design and Prototypes

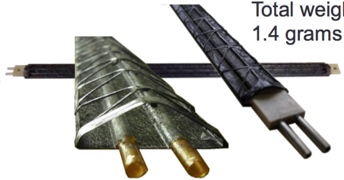
- Lightweight carbon structure with polyimide cooling pipes (wall thickness 25 μm)
- Average material budget $< 0.3\%\, X_0$



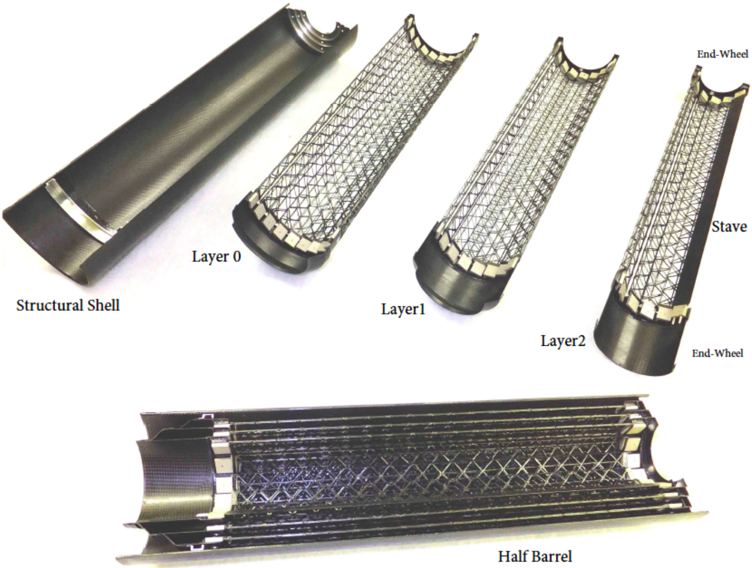




Total weight:
1.4 grams

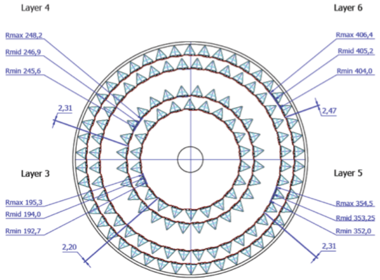


Inner Barrel Prototype



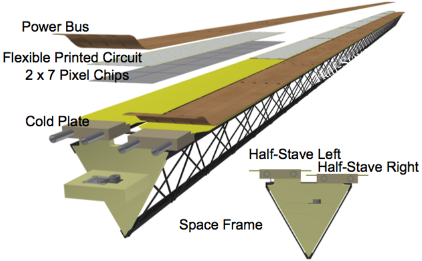
ALICE ITS Outer Barrel

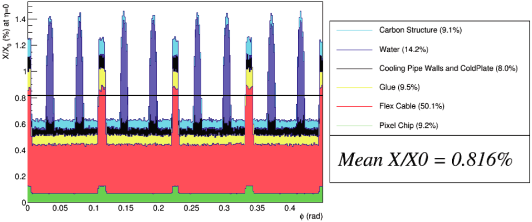
- 4 layers, radii: 194, 247, 353, 405 mm
- Length: 843 (ML), 1475 mm (OL)
- Nr of staves: 22, 28, 40, 46
- Nr of modules/stave: 4 (ML), 7 (OL)
- Nr of chips/module: 14
- Material budget / layer: $\sim 0.8\%\, X_0$
- Data throughput
  < 12 Mbit / sec / cm^2

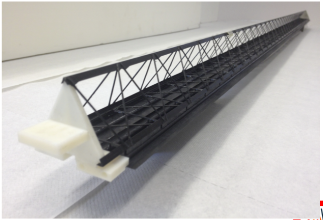


Outer Barrel Stave

- Outer barrel stave consists of two staggered half-staves
- Each half-stave further segmented into modules
- Average material budget per layer $\sim$ 0.8% X_0

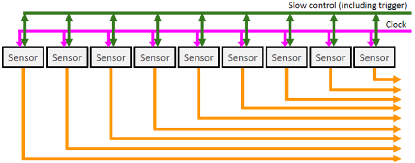




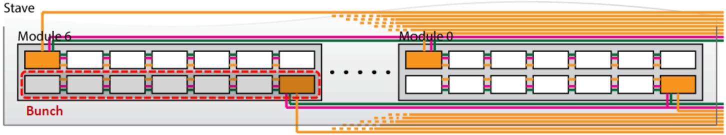


Stave Readout Topology

- From the innermost to the outermost layer
  - The expected hit densities decrease by a factor of 100.
  - The number of chips per (half-) stave increases from 9 to 98.
- Different readout topologies for inner and outer barrel
  - Inner Barrel: each chip drives point-to-point data line to off-detector electronics.



  - Outer Barrel: chips grouped into modules with two master chips; point-to-point link from masters to off-detector electronics.

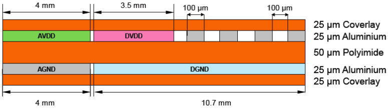


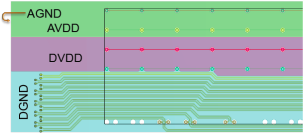
Outline

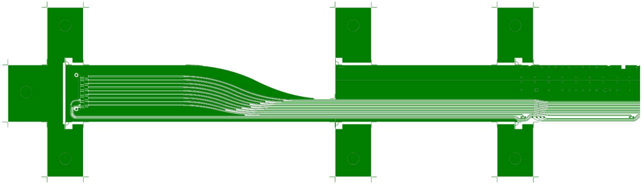
Flex Printed Circuit (FPC)

Here: Inner Barrel

- Flexible printed circuit of low-CTE polyimide and aluminium
- Power planes for digital and analogue voltage
- 11 differential pairs (clock, configuration, 9 data lines)

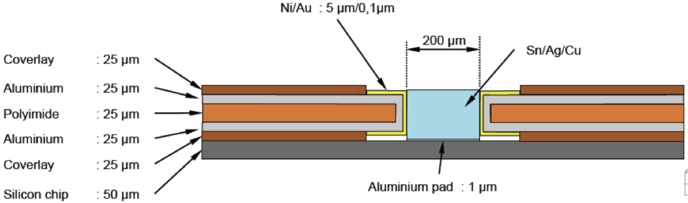


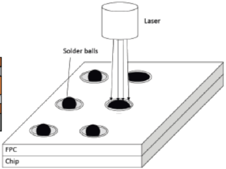


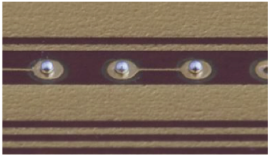


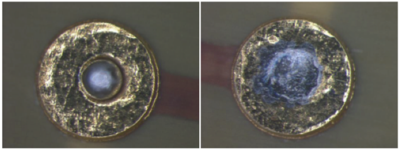
Outer Barrel: Decided to use Cu instead of Al ($\sim +0.1\% X_0$), physics impact low enough

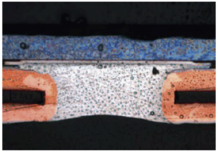
Chip-to-FPC Connection











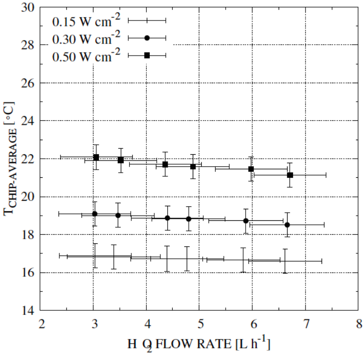
Chip and FPC will be connected by laser soldering

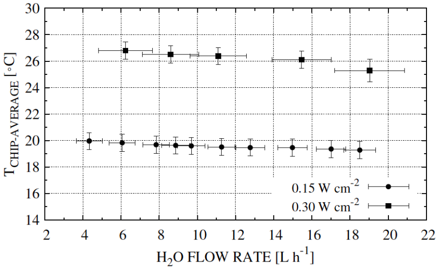
- Connection to dedicated pads distributed over the full chip area
- Successfully tested with daisy-chain and real chips
- Thermal cycling tests currently ongoing

Outline

Cooling

- Goal: Chip temperature below 30°C
- Baseline: leakless (< 1 bar) water cooling
- Thermal characterisation of stave prototypes with heaters for different flow rates:
  - Chip (heater) temperature well below 30°C
  - Pressure drop < 0.3 bar





Summary

- ALICE will replace its entire Inner Tracking System by a MAPS based pixel-only tracker during LS2
  - All R&D items of the project are close to finalised
  - Two working pixel chip prototypes
  - Currently completing R&D and preparing for start of production / construction in 2016