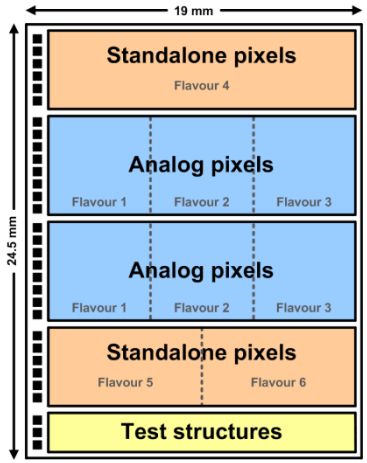
Ideas on MAPS design for ATLAS ITk

HV-MAPS challenges

Fast signal
Good signal over noise ratio (S/N).
Radiation tolerance (various fluences)
Resolution and readout rate
Filling factor and area coverage
Power needs

Signal speed

√ ACHIEVED: provided that drift field is created (HV-CMOS technology) even with “large” technology node (AMS .35) the signal can be kept within < 50 ns. Smaller nodes allows for even shorter time performance. The imminent H35 submissions features pixel flavours with more aggressive time performance and will give further reassurance on this aspect.



- **Analog pixels (2 large arrays of 24 rows x 300 columns each)**
  - Flavour 1 (24 rows x 100 columns) → mid-gain pre-amp. + low-speed
  - Flavour 2 (24 rows x 100 columns) → high-gain pre-amp. + high-speed
  - Flavour 3 (24 rows x 100 columns) → low-gain pre-amp. + very high-speed
- **Digital pixels (2 large arrays of 16 rows x 300 columns each)**
  - Flavour 4 (16 rows x 300 columns) → CMOS comparator in the periphery
  - Flavour 5 (16 rows x 150 columns) → nMOS comparator without TW compensation
  - Flavour 6 (16 rows x 150 columns) → nMOS comparator with TW compensation
- **Test structures**
  - Single diodes & extra pixels

Good S/N ratio

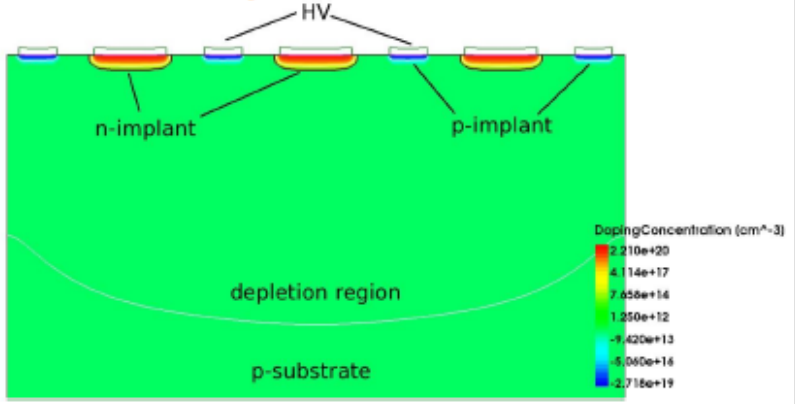
The requirement for fast signal shaping limits the noise performance of the analogue stage. For this reason (besides the charge collection speed) the presence of strong electric field in the sensor p-bulk is demanded. Deep depletion operations (where deep is a variable number, but $> 50\ \mu m$ is a good number) will yield the S/N .

Radiation tolerance (various fluences)

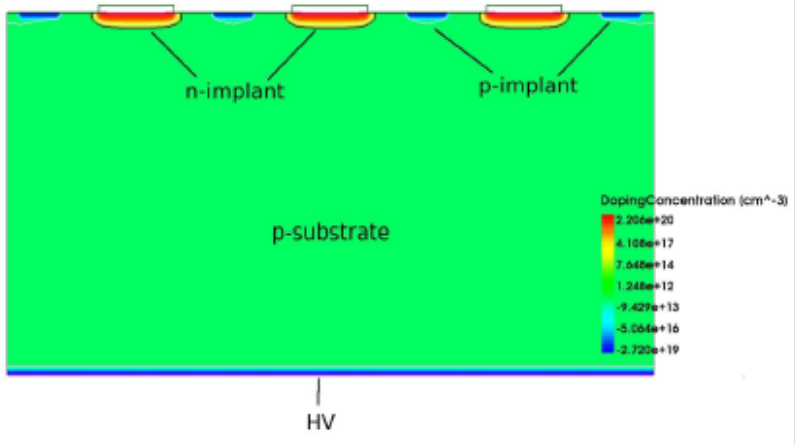
Need to operate with near 100% tracking efficiency after the target irradiation fluence. These will change depending on the radial distance, but we should set ourself targets like 0.5, 1, 3, 5 x 10^{15} n_{eq} cm^{-2} (displacement damage) and 10, 50, 100 and 250 Mrad (TID). A substantial impact on the performance is given by the biasing scheme.

The Two Bias Schemes compared

- HV top

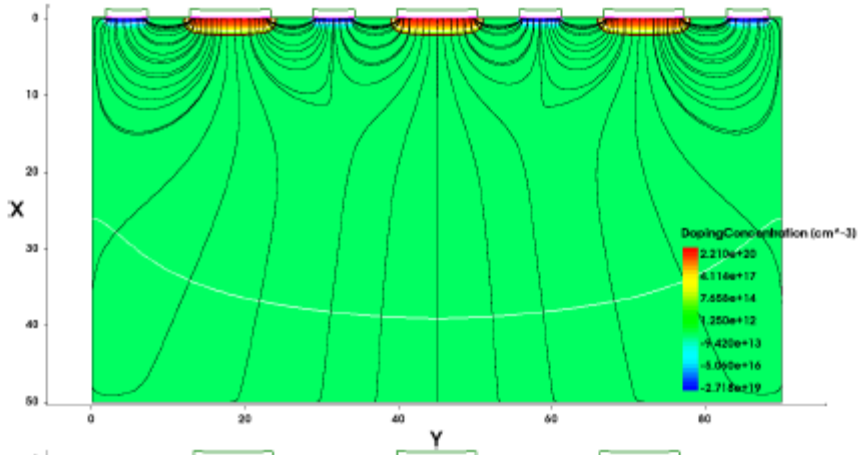


- HV back (p-implants floating)
- Full depletion at -60V (50µm thickness)

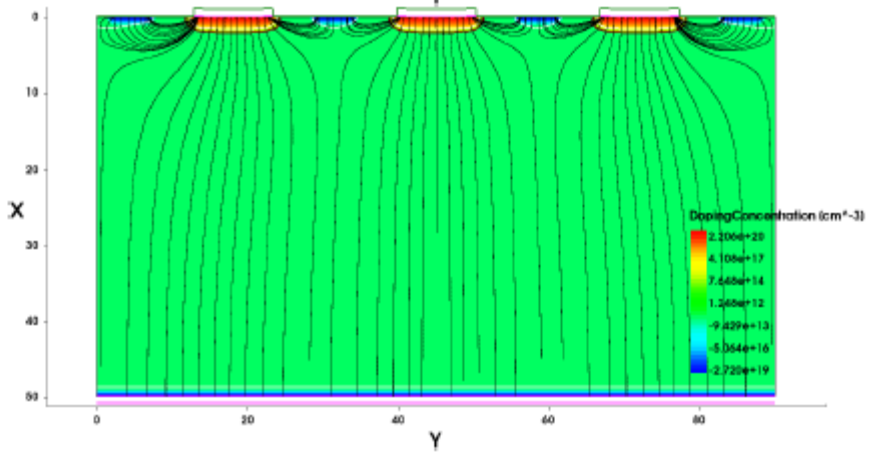


E-field Lines Comparison

- HV top

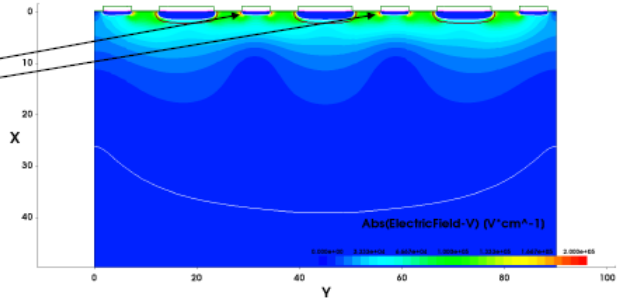


- HV back
- More uniform field

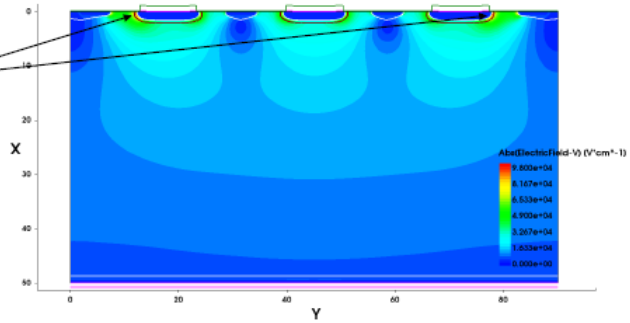


E-field Value Comparison

- HV top
- High field regions
- Value $2x10^5$ V/cm

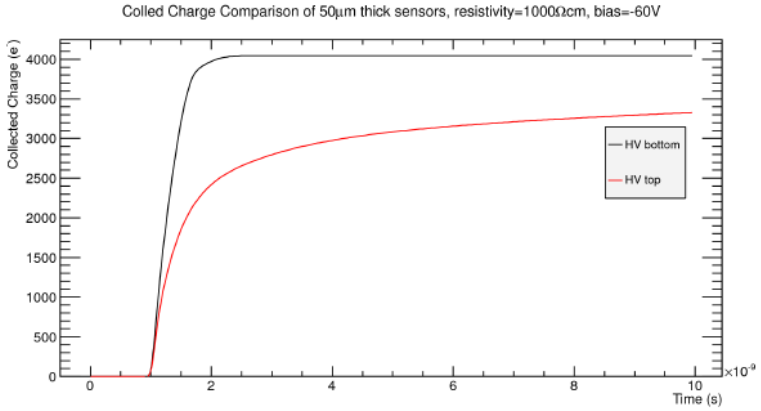


- HV back
- High field regions
- Value $9.8x10^4$ V/cm
- Lower field value
- Deeper field



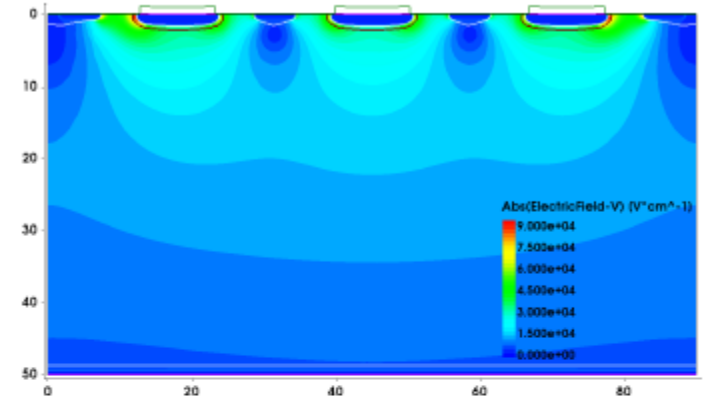
Charge Collection Comparison

- Mip enters at 1ns at width of 45µm, 80eh pairs per µm
- Deposits total charge of 4000e$^-$
- Back bias full charge collection at 2ns compared to ≈60% for HV top

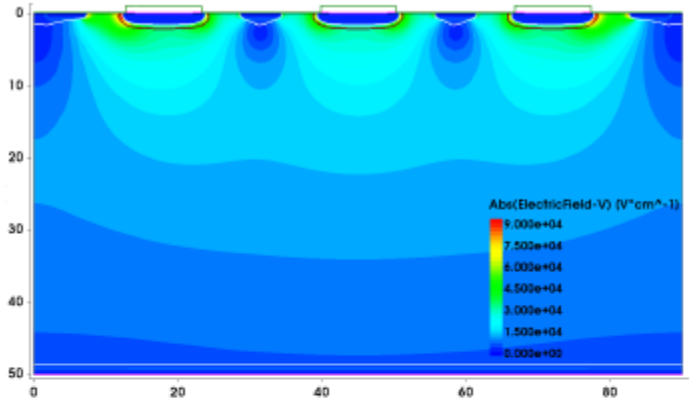


The electric field keeps a similar shape with irradiation and the backplane biasing should allow violating the maximum applied bias allowed from the technology.

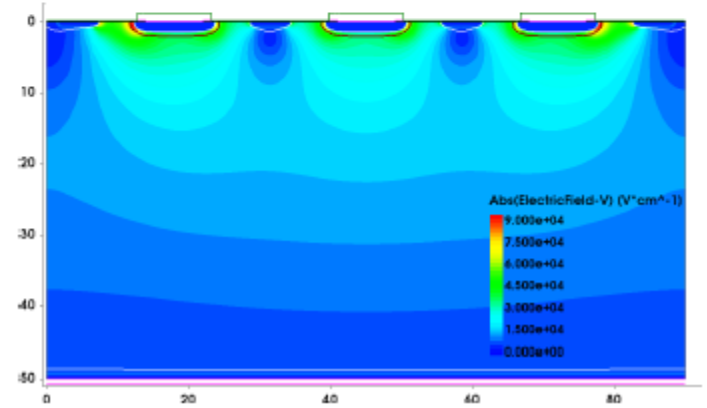
E-field with Radiation



- $\Phi_{eq}=1x10^{13}cm^{-2}$ (CLIC)



- $\Phi_{eq}=1x10^{14}cm^{-2}$



- $\Phi_{eq}=1x10^{15}cm^{-2}$

Back biasing is a strong recommendation!!

Radiation tolerance (various fluences)

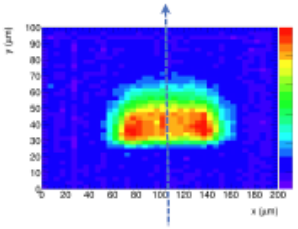
Substrate resistivity is also a parameter for radiation tolerance. The depletion depth depends on both the resistivity and the applied bias voltage. It could be a parameter that is advantageous to optimise for the specified target fluence (layer). It should be notice that the effective space charge(N_{eff}) of p-type bulk silicon does not increase immediately with irradiation!

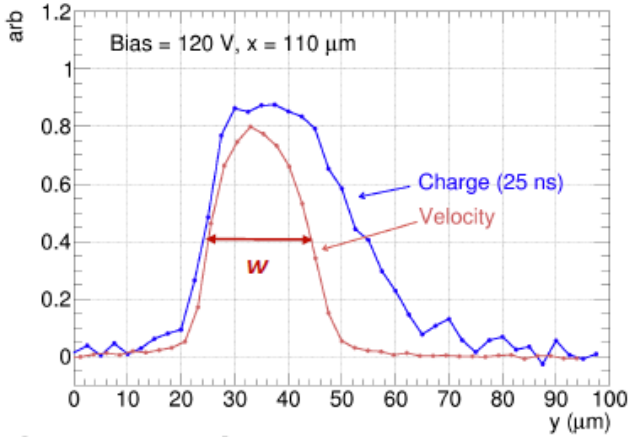
Edge-TCT

Chess1, not irradiated

1) **charge: time** integral of induced current pulse (25 ns)
2) **velocity** (in E-TCT): induced current immediately after the laser pulse

$$I(x,y,t\sim 0)\approx qE_w(x,y)\left[\bar{v}_e(x,y)+\bar{v}_h(x,y)\right] \quad \bar{v}_e(x,y)+\bar{v}_h(x,y)\propto E$$



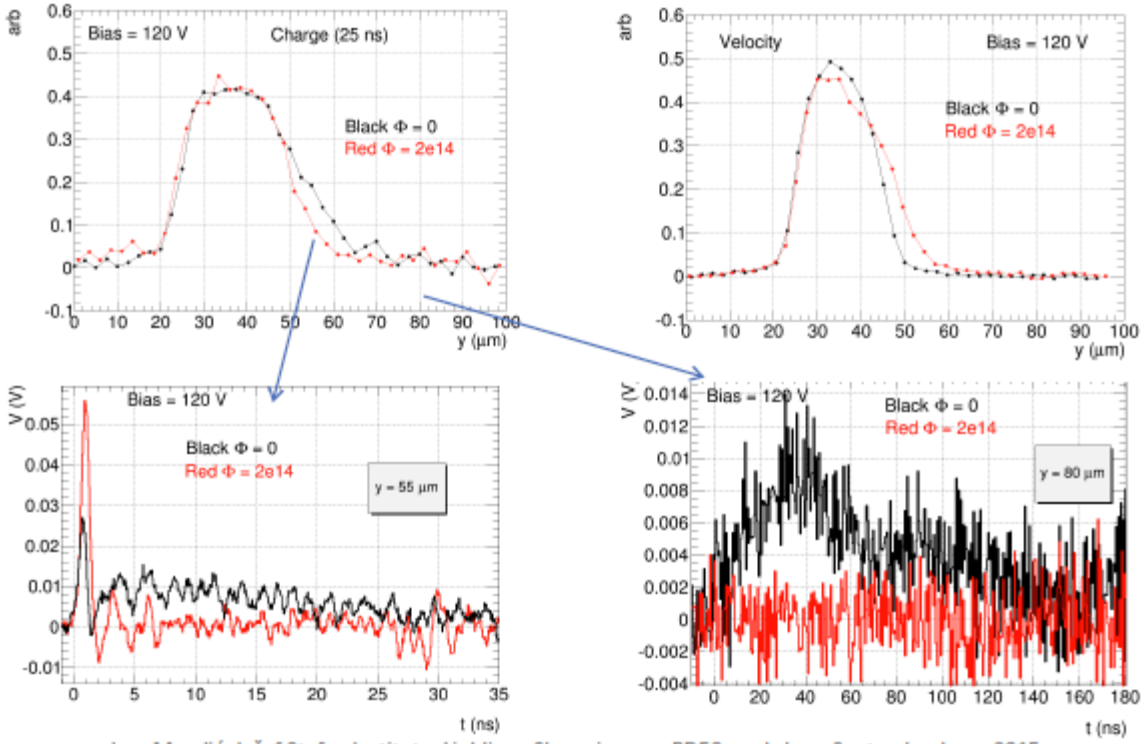


- **high velocity → electric field → depleted region**
- charge collection region wider (diffusion)
  → take into account non zero laser beam width (~ 10 µm)

Edge-TCT

Chess1, irradiated with neutrons to 2e14 n/cm^2 in reactor in Ljubljana

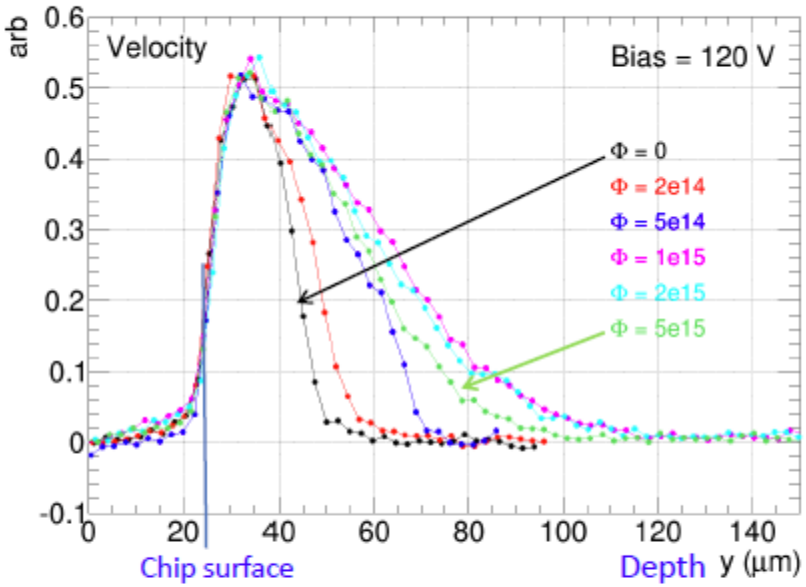
- charge collection region narrower
- field region (velocity) increases ➔ acceptor removal
- no long tails of induced current pulses ➔ trapping, less diffusion

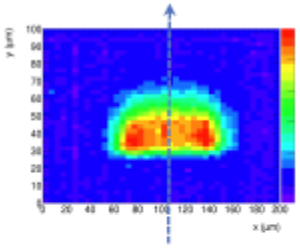


Edge-TCT

Chess1, irradiated with neutrons up to 5e15 n/cm2

Fluence steps: 2e14, 5e14, 1e15, 2e15, 5e15



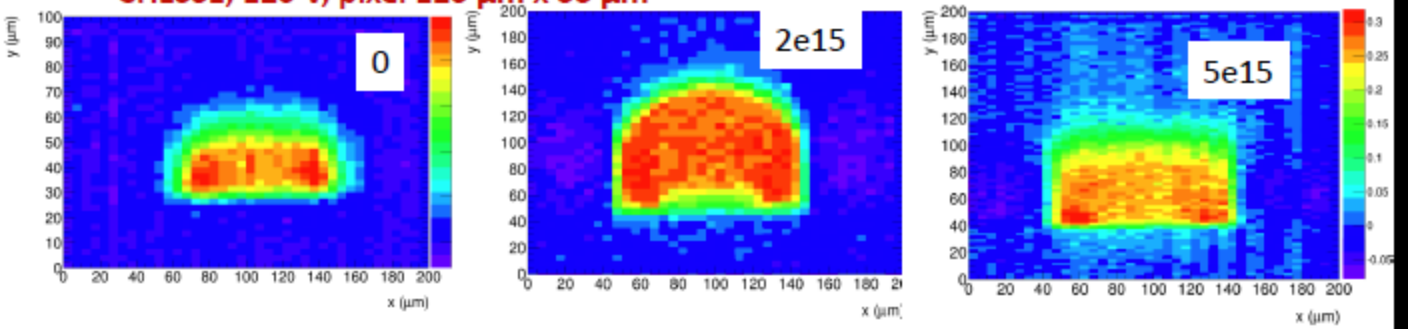


- the depth with electric field (depleted depth) increases with fluence up to ~ 1e15
  - ➔ concentration of initial acceptors falls with irradiation faster than new acceptors are introduced ➔ space charge conc. falls
- depleted depth smaller at 5e15 than at 2e15
  - ➔ acceptor removal finished, space charge concentration increases with irradiation
- **after 5e15 depleted depth still much larger than before irradiation**

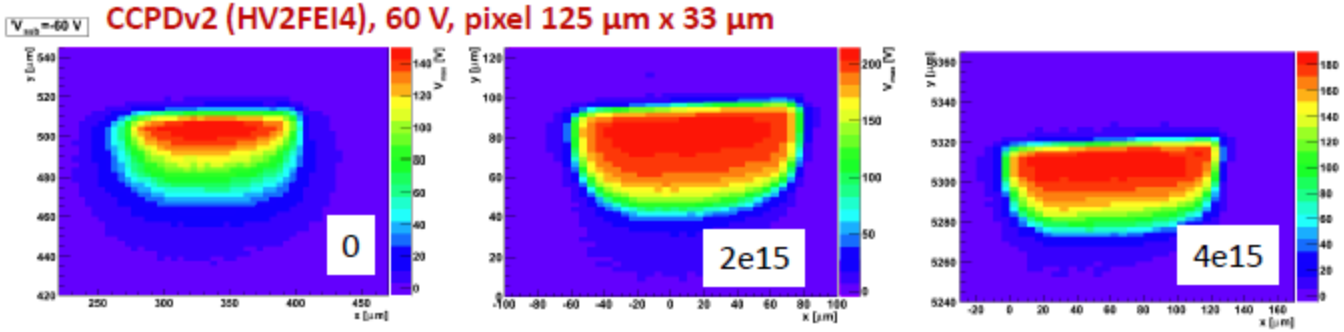
Edge-TCT

Irradiatied with neutrons

CHESS1, 120 V, pixel 125 µm x 33 µm



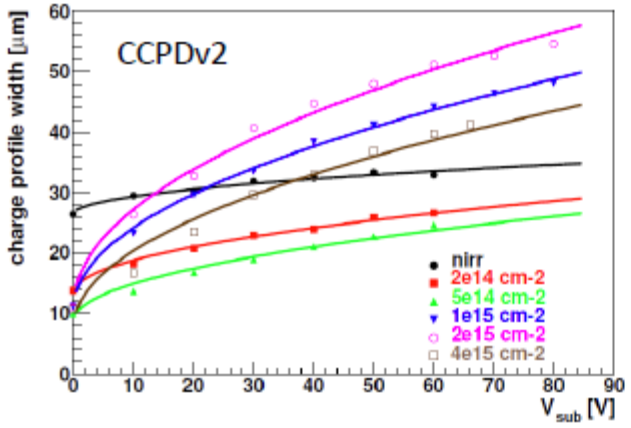
CCPDv2 (HV2FEI4), 60 V, pixel 125 µm x 33 µm

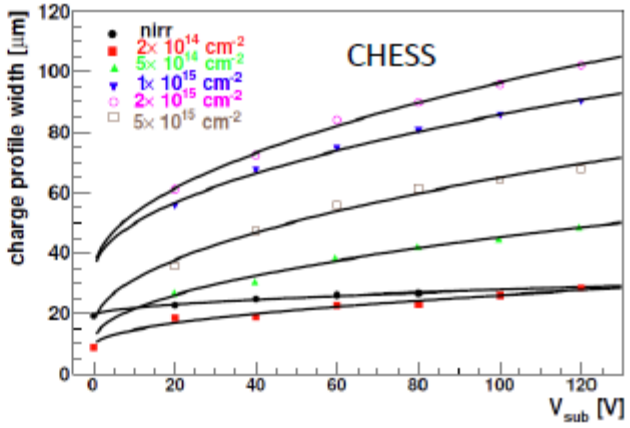


- charge collection region at 5e15 (4e15) smaller than after 2e15 but still much larger than before irradiation

Edge-TCT

- from E-TCT measurements extract the charge collection width vs. Bias voltage





- fit with: $Width(V_{bias}) = Width(0) + \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_{eff}} V_{bias}}$

N_{eff} : effective acceptor concentration - free parameter

➔ get N_{eff} dependence on neutron fluence

Evolution of N_{eff} with fluence

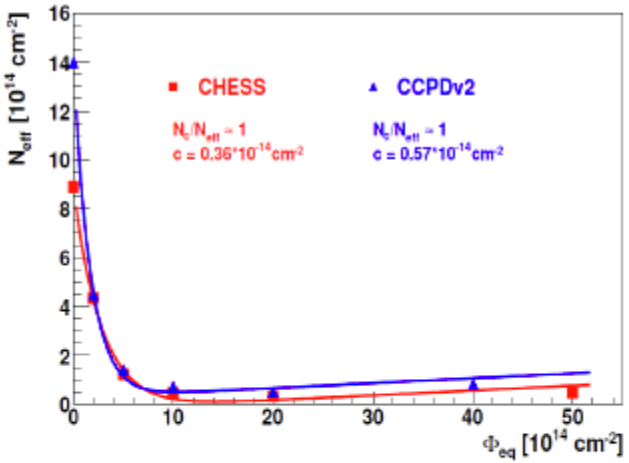
$$N_{eff} = N_{eff\,0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$$

Initial concentration

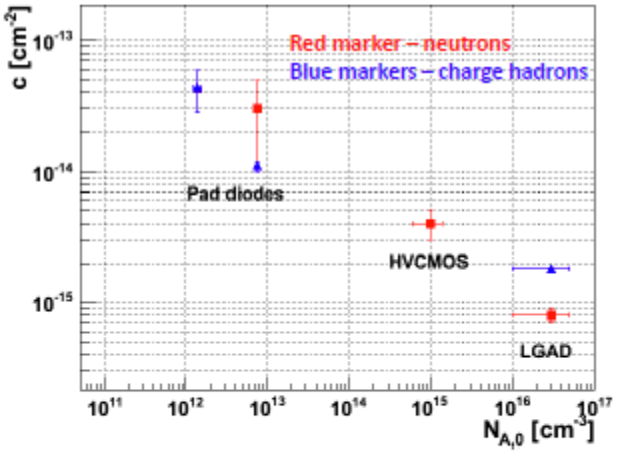
acceptor removal

Radiation introduced deep acceptors (stable damage): g = 0.02 cm^{-1} (fixed)

N_{eff} vs. fluence



Removal rate c depends on initial space charge concentration



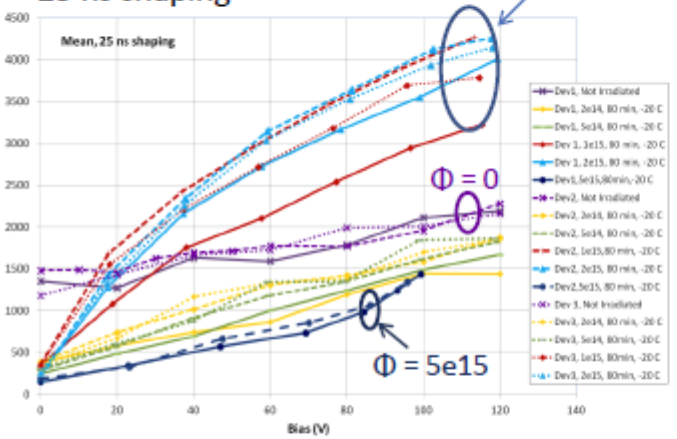
G. Kramberger, 10th Trento workshop

http://indico.cern.ch/event/351695/session/4/contribution/4/material/slides/0.pdf

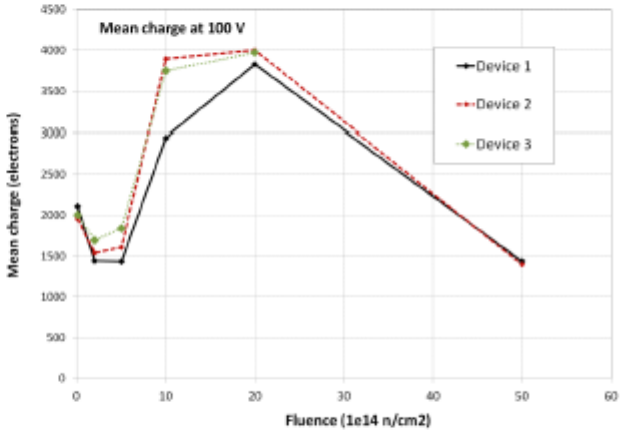
MIP CC measurement

CHESS1 large passive HV-CMOS array – 3 devices irradiated with neutrons
Fluences: 2e14, 5e14, 1e15, 2e15, 5e15

Mean Charge vs. bias
25 ns shaping



Charge vs. fluence



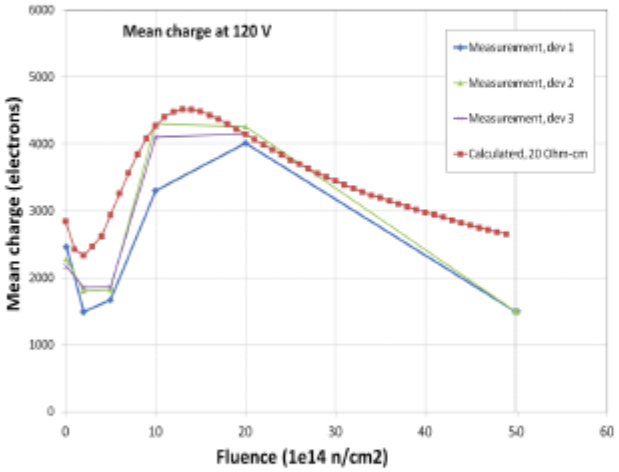
- charge drops after first irradiation steps: **smaller diffusion contribution**
- charge increases with more irradiation ➔ **depleted region increases due to acceptor removal**
- charge drops at higher fluence ➔ **acceptor removal finished, space charge conc. increases with fluence, more charge trapping**

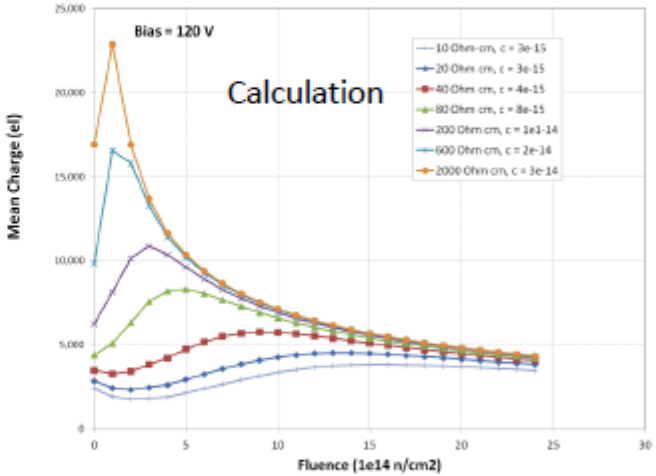
Calculate CC for different resistivites:

➔ Mean Charge = depletion(μm)* 100 el/μm * trapping_loss + Diffusion (mostly gues)

- 1300 el at Φ = 0
- 650 el at Φ = 1e14
- ..
- 0 el at Φ > 4e14

Compare measured/calculated





- higher resistivity → more charge
- possible to stay above initial charge in certain fluence range

The idea of tuning the resistivity to the radiation fluence is feasible mainly if backside biasing is implemented.

Resolution and readout rate

Compromise between the pixel size and the readout complexity.
Small pixels can be achieved in CMAPS, analogue encoding can be used for improving granularity. All this adds to the digital circuitry.
Part (if not all) of the digital activity is outside the sensitive area and it has impact on tiling.

Filling factor and area coverage

Filling factor has two aspects: in the active area (possible loss of efficiency in the inter-area between collecting n-wells) and periphery for digital circuits
The first effect is strongly mitigated (aka solved) by “deep depletion” and collection by drift.
The second aspect depends on readout architecture and choices (e.g. In pixel discrimination).

LF15A is a modular 0.15 µm RF CMOS process, offering up to 6 levels of Al plus thick metal (2 - 6 µm), optionally a MIM capacitor, a polyimide passivation and I/O voltages of 1.8 V, 3.3V and 5.0 V.

- Substrate resistivity 1-2kΩcm
- Allow isolated NWELL within a DNWELL (Full CMOS)
- Large fill factor ~85% for 50x250 µm^2 pixel
- Break down voltage ~120V

Thinned to 125um:

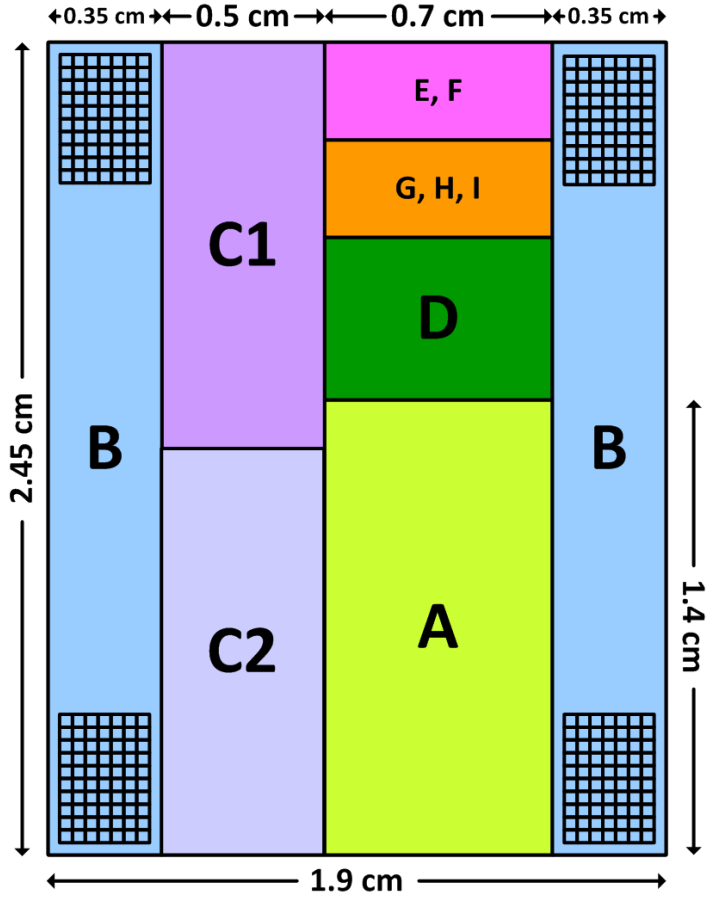
- full depletion from the back side should be feasible (80V at 2kΩcm)
- Q_{MIP} ~ 10000e^-
- Cin ~ 400fF (70fF DNW to SUB, 330fF DNW to PW) for 50x250 µm^2 pixel (worst case)
- Considering sharing a threshold around 1000e^- should give us reasonable efficiency. Required Noise ~100e^-

Filling factor and area coverage

The reticule size with a maximum of ~ 2 x 2 cm^2 obliges to make a rather laborious tessellation work to produce large area systems. This could be improved if CMAPS detector can be diced in multiple reticules. The inter-reticule area could result in a non-sensitive region. This has to be minimised or made sensitive. Deep-depletion devices can allow to make the field extended laterally to cover the inter-reticule area. We need to study how strongly this mitigation factor improves the coverage using stitching methods (with the foundries that allow for it) or by dedicated crafting of the n-well geometry in the border pixels.

Routing demonstrator - Floorplan

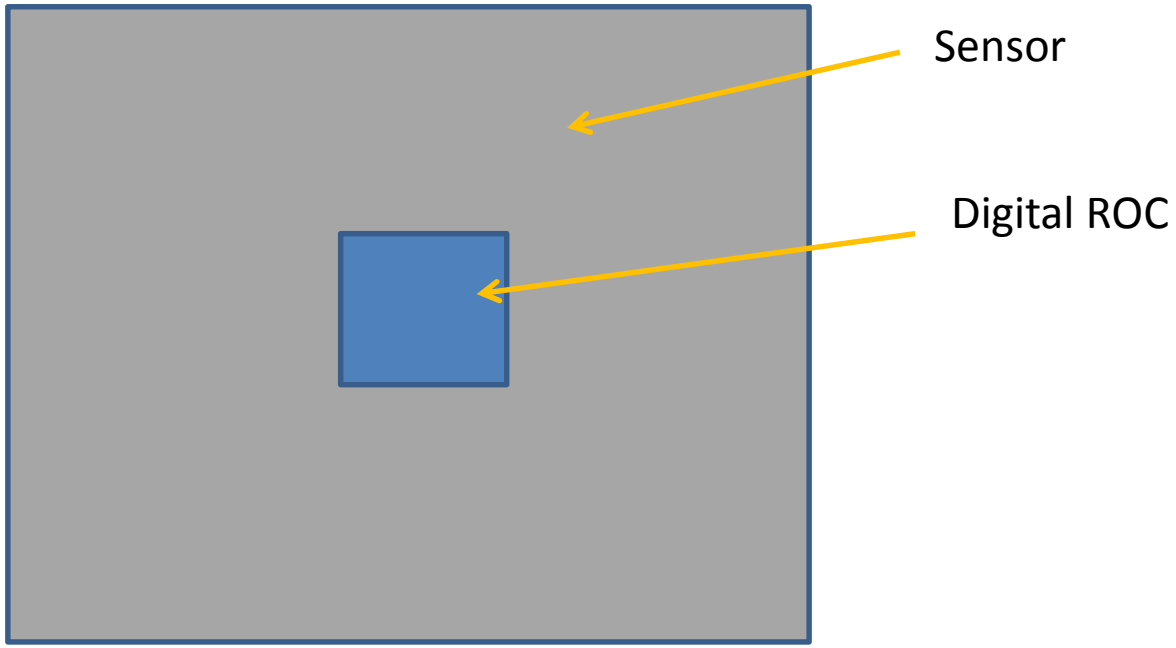
- **Floorplan** (engineering run with maximum reticle size of 1.9 cm x 2.45 cm)



- **A** → Not decided at the moment
- **B** → Pixel array with metal routing lines to test fan-out (x2)
- **C1** → Type B pixel array with HV strip pads for readout
- **C2** → HVPixelM chip with rolling shutter readout
- **D** → Digital circuit with comparator that has adjustable threshold
- **E** → 25 µm x 25 µm macro-pixel with 4 sub-pixels with encoding (readout with CLICpix, Medipix, Timepix)
- **F** → Test structures (diodes, pixels with/without comparators, different feedback)
- **G** → Pixels with encoding for strip readout
- **H** → Pixels with fan-out structure for strip readout
- **I** → Test powering FEI4 through top metal layer

Filling factor and area coverage

The routing of channels to a readout pad area could allow to use a small readout chip for removing the digital circuits from periphery (this implies use of stitching and TSV on the readout chip).



HV-MAPS challenges

Fast signal √

Good signal over noise ratio (S/N). Improving if backplane biasing implemented. At CMOS foundry level or post processing.

Radiation tolerance (various fluences).). Improving if backplane biasing implemented. Possible playing with substrate resistivity. NOTE: deep depletion with high voltage better than deep depletion with high res substrate.

Resolution and readout rate. System dependant. Optimisation exercise.

Filling factor and area coverage. Study stitching or multi-reticule dicing.

Power needs. System dependant.