Cold Electronics R&D for ArgonCube

M. BISHAI, H. CHEN, G. DE GERONIMO, F. LANNI, D. LISSAUER, V. RADEKA, B. YU

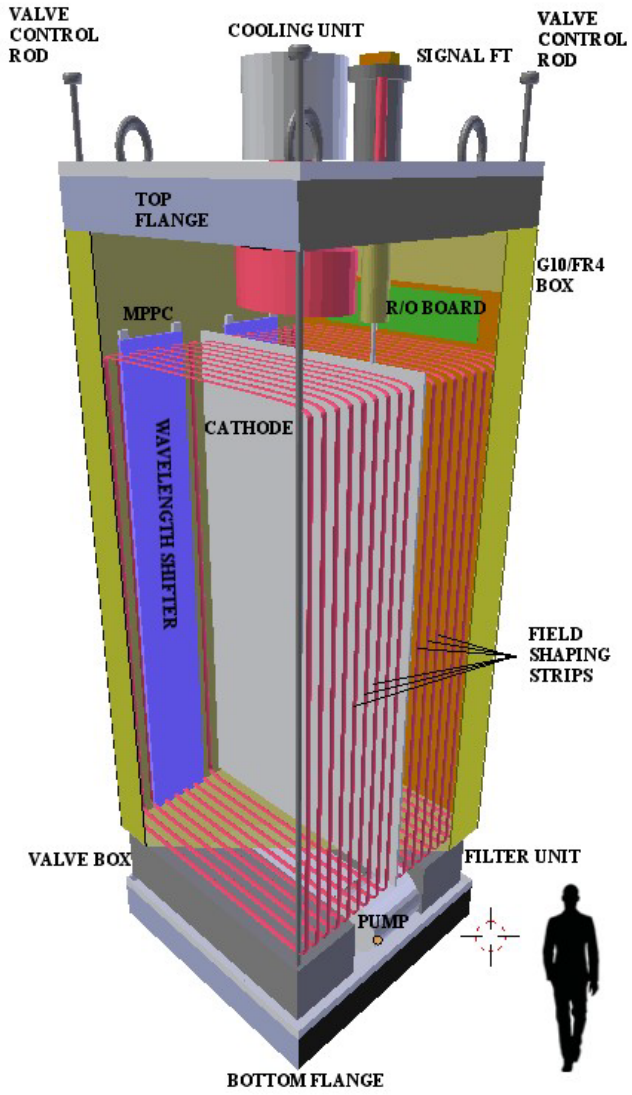
BROOKHAVEN NATIONAL LABORATORY

AUGUST 27TH, 2015

Outline

- Introduction
- Cold Electronics Development for Phase-1 R&D
  - Cold ASIC Advancement Plan
- Cold Electronics Development for Phase-2 R&D
  - Electrode Configurations with reduced ambiguity
  - Pad Readout With Power Switching
  - An Example of Pad Readout
- Summary

Introduction

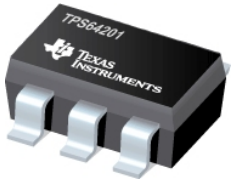


- ArgonCube: a novel, fully-modular approach for the realization of large-mass liquid argon TPC neutrino detectors
- A well motivated R&D proceeding through 3 phases
- This talk will focus on cold electronics development related to Phase-1 R&D and some preliminary ideas for Phase-2 R&D

Cold Electronics Development

- R&D of CMOS cold electronics started in 2008
  - Analog FE ASIC was the first one developed, following by ADC ASIC development, studies of cold regulator and FPGA etc.
- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - ARGONETUBE
  - LArIAT
  - DUNE 35 Ton
  - ICARUS 50l TPC at CERN
  - SBND
  - protoDUNE at CERN
  - DUNE Far Detector
- Cold electronics design is best performed jointly with the TPC electrode design for different experiments
  - As a part of our future program, finer segmentation electrodes and readout will be explored (planar anodes instead of wires) → ArgonCube Phase-2 R&D

Cold Electronics

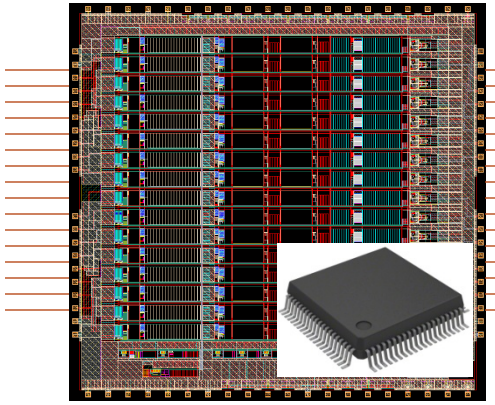


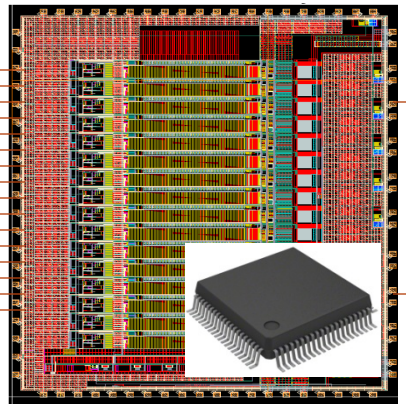
voltage regulation
(COTS)
(< 100mV dropout)

front-end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.



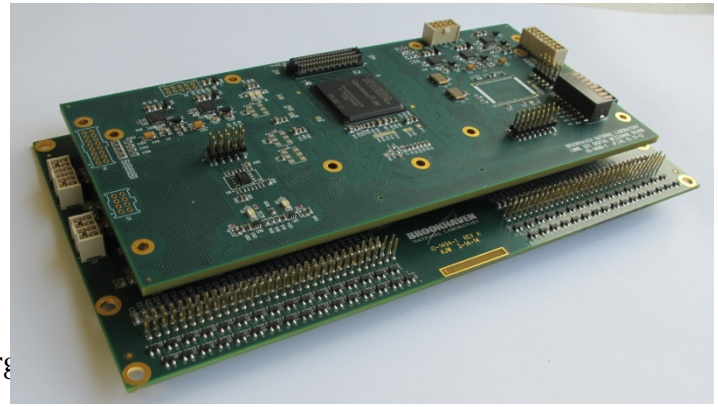


overall 128:2
multiplexing

8 x

1 x

A Complete Front End Readout Chain



front-end cold
module
serving 128 wires
~ 2.4 W

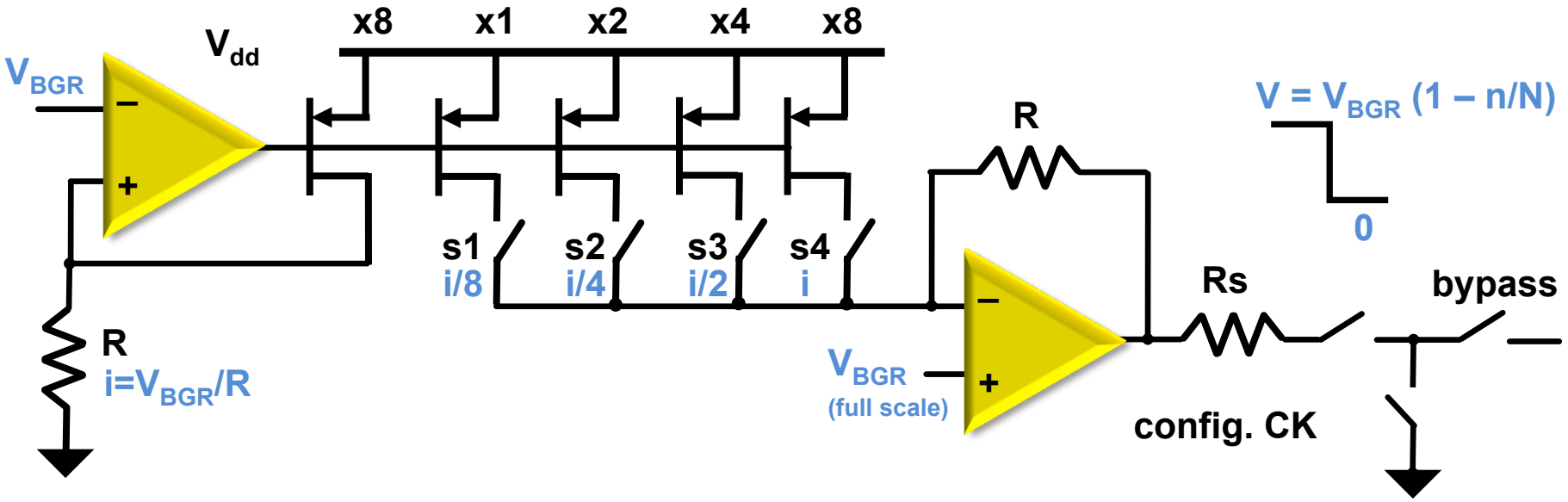
Cold ASIC Advancement Plan

- The next step in the cold electronics advancement will require a revision of both the FE and the ADC ASICs
  - The purpose of the revision is to make the ASICs more versatile and adaptable to different detector designs and different readout architectures, as well as to make more resistant to ESD
  - The revision does not require any changes in the basic ASIC design
- The development of cold ASICs will be jointly supported by SBND and DUNE
  - The first submission is planned in January 2016
  - The second submission is planned in July/August 2016 after the full evaluation of the first submission

Revision Plan of Analog FE ASIC

- Revision of FE ASIC will aim to further improve the robustness of chip and simplify the system design of the front end readout electronics
  - Revisions are limited to fine adjustments with low risk
- List of changes
  - Improve the input & output protection
  - Implement smart reset
    - Use combination of CS and CK to generate reset internally
    - Eliminate the requirement of external reset pin
    - Circuit has been exercised in other ASICs (ADC, VMM etc.)
  - Improved driving capability of the last stage of shaper
  - Implement internal pulse generator
    - To perform precision charge calibration
    - External high precision calibration is still accessible by bypassing internal calibration circuit
    - External calibration pulse input becomes an option, easy to scale to larger detector
  - *Plan to Implement read back of internal serial configuration registers*

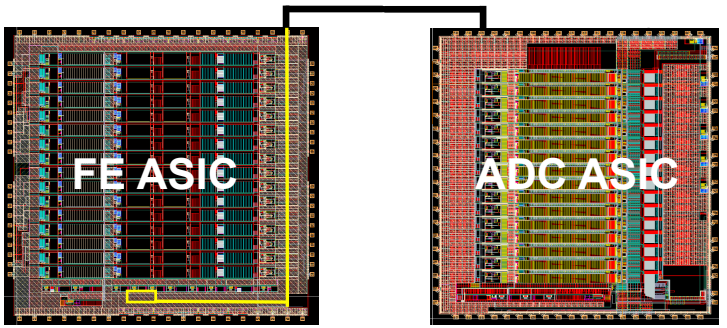
Integrated Calibration Circuit



- proven configuration, implemented in many front-end ASICs
- band-gap referenced (low temperature dependence)
- 4-bit or 5-bit programmable
- 40 mV to 1.2 V, 40 mV steps (>= 4 points per gain)
- non-linearity < 0.5 %, non-uniformity < 2 %
- re-usage of amplifiers (low risk implementation)
- re-usage of signals (config. clock)
- fully compatible with present scheme and pinout
- connect 8 FE-ASICs to reduce dispersion
- can be routed to calibrate ADCs as well

measured

$V_{BGR} \approx \begin{cases} 1.185\ V & \text{at } 300\ ^{\circ}K \\ 1.164\ V & \text{at } 77\ ^{\circ}K \end{cases}$



Revision Plan of ADC ASIC

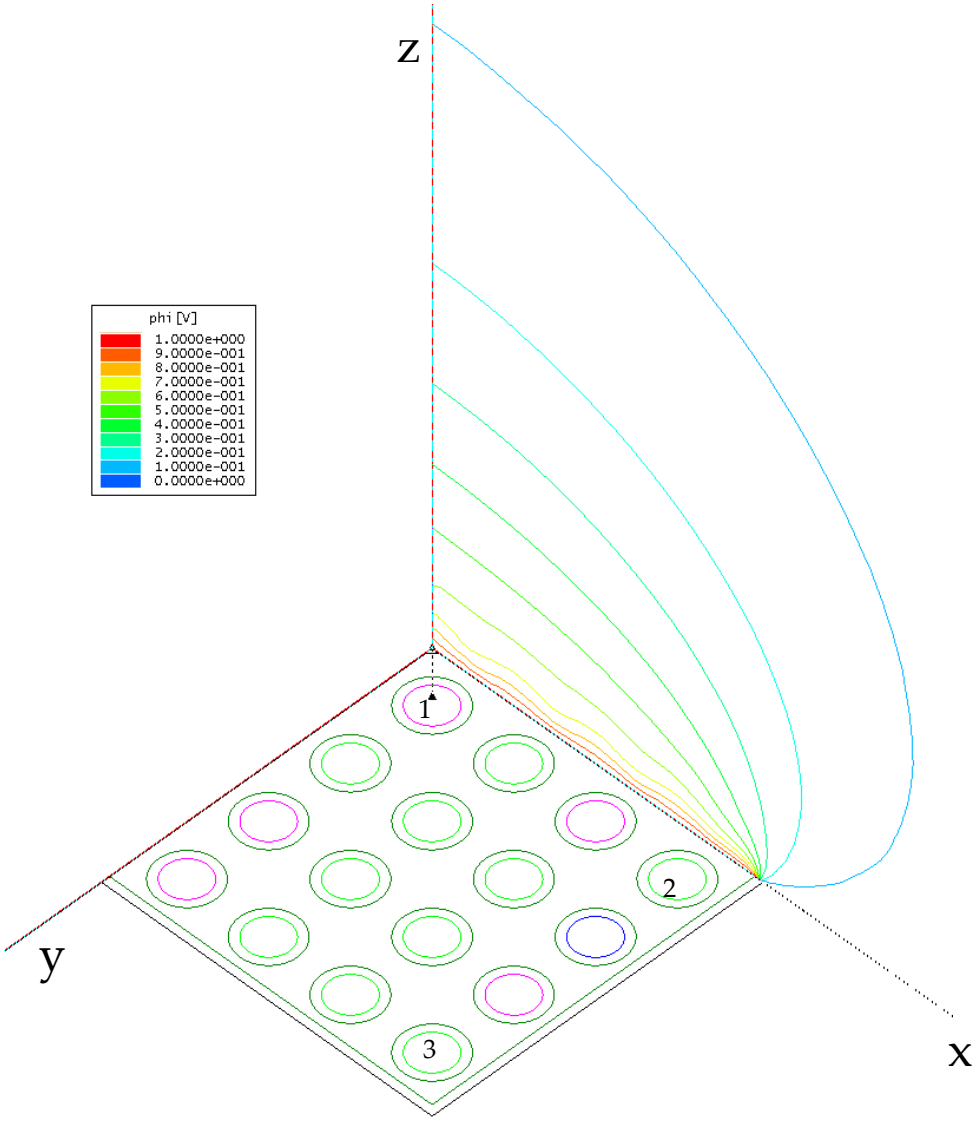
- Revision of ADC ASIC will aim to further improve the performance, simplify the usage and interface to the front end readout electronics
  - Revisions will be based on the test results of the current version and the discussion of DUNE COLDATA interface in July, 2015
- List of changes
  - Implement the power on default configuration
  - Improve the input & output protection
  - Improve the ADC DNL/INL performance
  - Implement user friendly interface
    - Add dedicated test pattern generation command instead of using SDI input
  - Implement compatible SPI interface between FE ASIC and ADC ASIC
    - Future design will have a pair of FE ASIC and ADC ASIC daisy chained together
    - Both chips will use single ended signals
  - Implement compatible interface to COLDATA ASIC
    - Implement ADC_CONV input and ADC_BUSY output
  - *Plan to Implement read back of internal serial configuration registers*

A pad electrode concept - FEA Model by Bo Yu

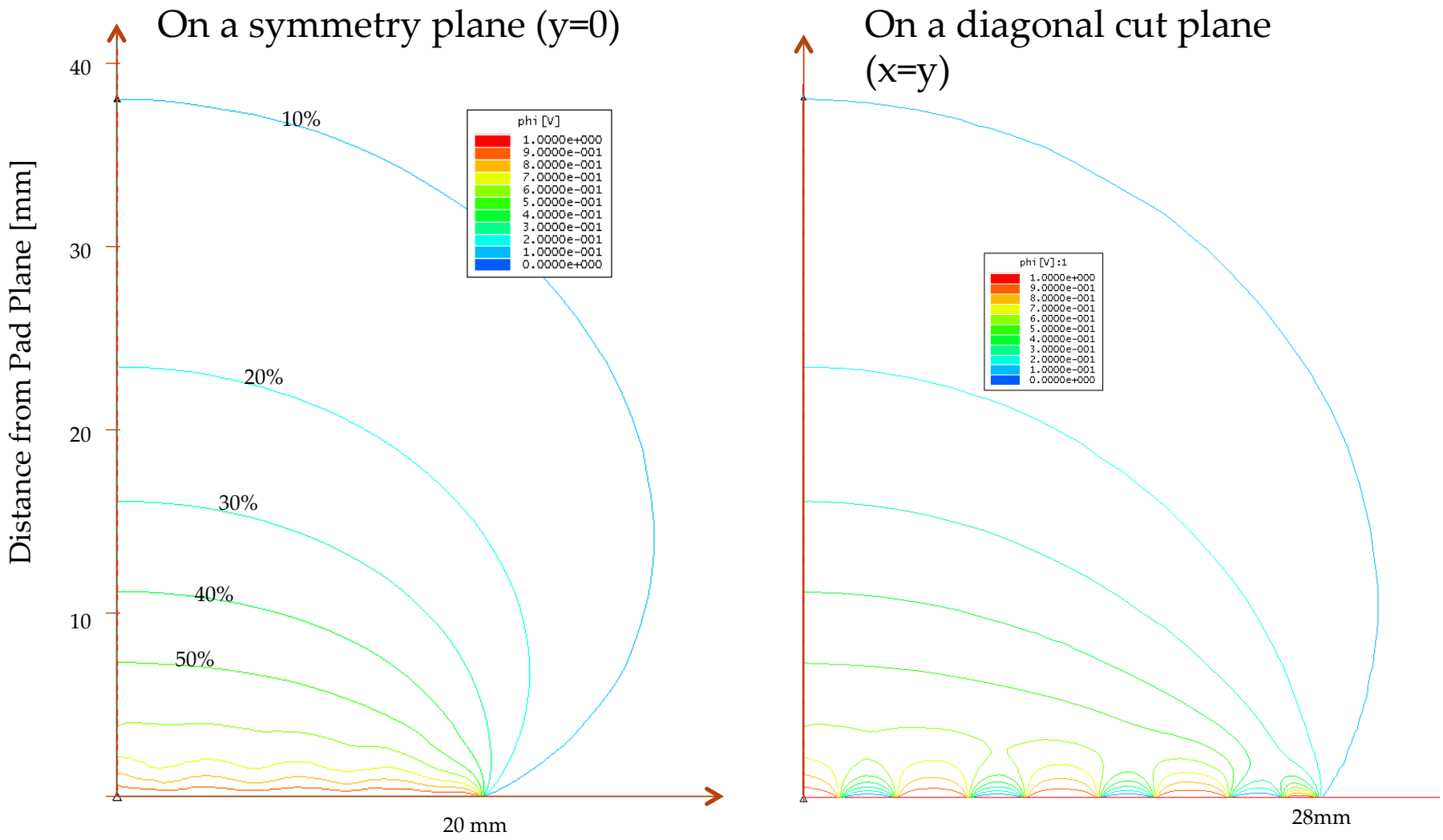
The model represents ¼ of the 64 channel pad group with one induction pad. The collection pixels are circles with diameter of 2.5mm at a pitch of 5mm. The induction pad covers a 39.5mm x 39.5mm area. The gap between electrodes is 0.5mm.

The problem volume is 1m on each axis. Two faces of the volume (x=0, y=0) are mirror symmetry boundaries to simulate the full 64ch group.

This weighting potential distribution is obtained with the induction pad at 1V, while all other electrodes are grounded.

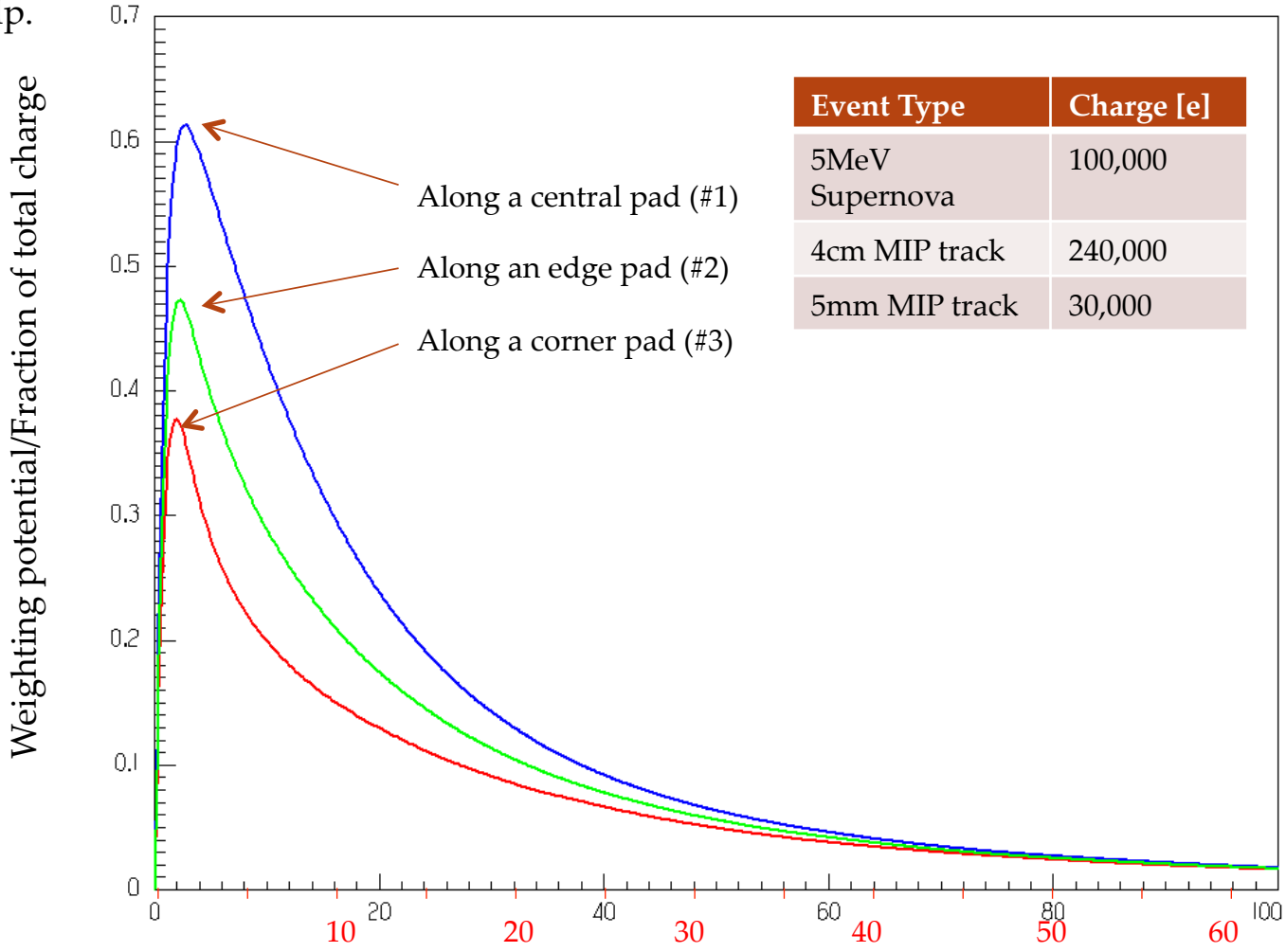


Weighting Potential Contour on two Cut Planes



Weighting Potential vs Distance

These are the weighting potential values along 3 drift lines centered on 3 collection pads (labeled on the first slide). There is significant delay in the induced current rise time on for the edge and corner pixels. On the other hand, these events will induce signal on the adjacent induction pads. Perhaps a lower threshold and adjacent induction pad coincidence logic could help.



Event Type	Charge [e]
5MeV Supernova	100,000
4cm MIP track	240,000
5mm MIP track	30,000

Pad Readout Cold Electronics Concept

- A first look shows the trigger based pad readout might be ***possible***
- Pulsed power may be essential to make scaling up of this concept feasible. A wake-up time for the ASIC needs to be less than 10us, which is ***feasible.***
- Cold electronics design is very challenging due to power consumption of FEE on large number of readout channels
  - Pad size: 5 mm x 5 mm
  - Anode size: 2 m x 10 m
  - Collection pad: 800,000
  - Induction tile: 12,500
  - Power of cold electronics: 10 mW/ch (FE+ADC only)
  - Power Cable: 25 x AWG0000 – 50 mm x 50 mm

Pad Readout Cold Electronics

- Cold electronics design is very challenging due to power consumption of FEE on large number of readout channels

	Peak Power
# of Active Channel	812,500
# of Standby Channel	0
Power [W]	8,125
Current [A]	4,514
Voltage Drop on 5 meters Cable [mV]	145.2

Pad Readout Cold Electronics

- Cold electronics design is very challenging due to power consumption of FEE on large number of readout channels

	Peak Power	Off Mode
# of Active Channel	812,500	12,500
# of Standby Channel	0	0
Power [W]	8,125	125
Current [A]	4,514	69
Voltage Drop on 5 meters Cable [mV]	145.2	2.2

Pad Readout Cold Electronics

- Cold electronics design is very challenging due to power consumption of FEE on large number of readout channels
  - One possibility is to keep FEE in standby mode, which consumes a current about 2 orders of magnitude lower
  - Quickly wake up channels only when trigger arrives
  - Sophisticated power control system

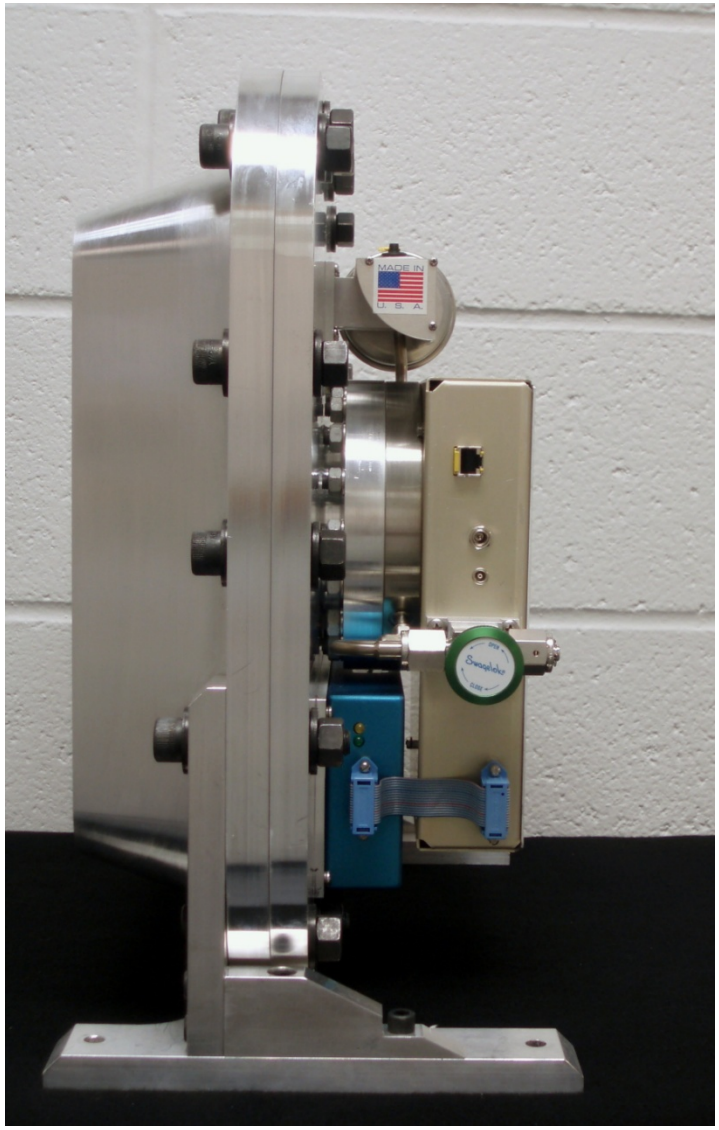
	Peak Power	Off Mode	Standby Mode
# of Active Channel	812,500	12,500	12,500
# of Standby Channel	0	0	800,000
Power [W]	8,125	125	205
Current [A]	4,514	69	114
Voltage Drop on 5 meters Cable [mV]	145.2	2.2	3.7

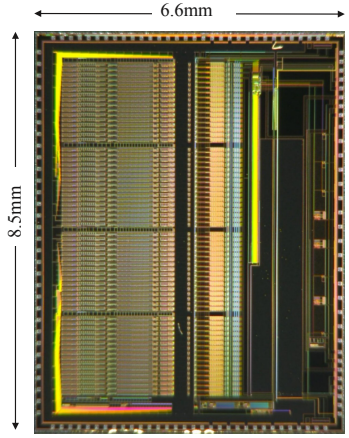
Pad Readout Cold Electronics

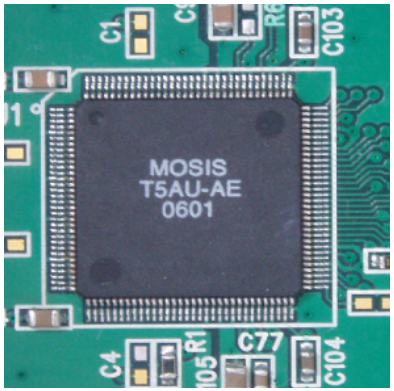
- Cold electronics design is very challenging due to power consumption of FEE on large number of readout channels
  - As a comparison, for 3 wire planes with 5 mm wire pitch
  - Channels: 6,000
  - Power: 120 W

	Peak Power	Off Mode	Standby Mode	Running Mode
# of Active Channel	812,500	12,500	12,500	112,500
# of Standby Channel	0	0	800,000	700,000
Power [W]	8,125	125	205	1,195
Current [A]	4,514	69	114	664
Voltage Drop on 5 meters Cable [mV]	145.2	2.2	3.7	21.4

An Example of Pad Readout

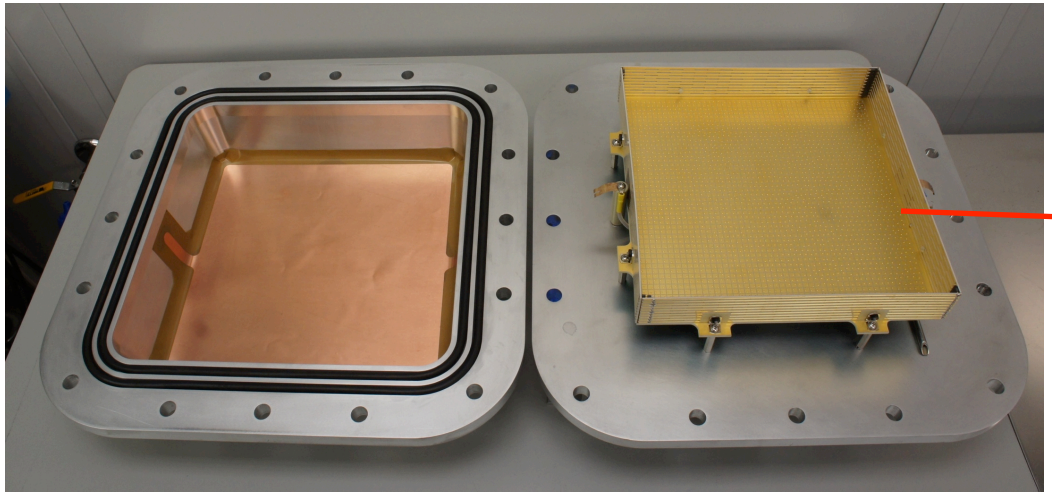




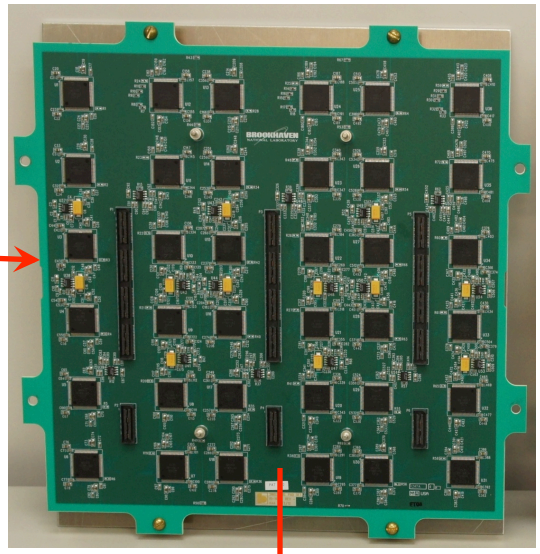


- A ^{3}He based neutron detector is being developed at BNL
  - Ionization mode pad detector for small angle neutron scattering
  - Goal: 1m × 1m area, 2.5mm resolution, 10^{8} Hz
- Prototype of 1/16 size, 24cm × 24cm in operation
  - 2,304 independent 5x5mm pads
  - Strong reliance upon ASICs
  - 64-channel ASIC, 2.3 mW/ch for single event counting; **TPC waveform recording requires ~10 times higher power**
  - 6.6mmx8.5mm, 315k MOSFETs
- Currently developing a detector for SANS @ ANSTO in Australia
  - 1m x 1m
  - (16) 24 x24cm pad boards tiled 4x4
  - 37,000 pads, 10^{8} n/s

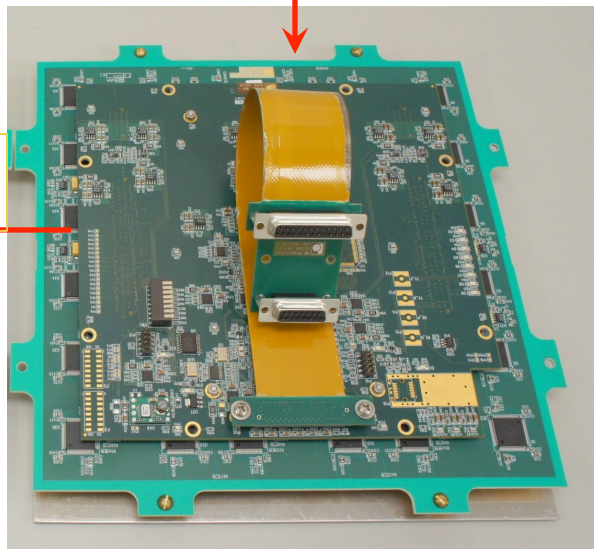
An Example of Pad Readout



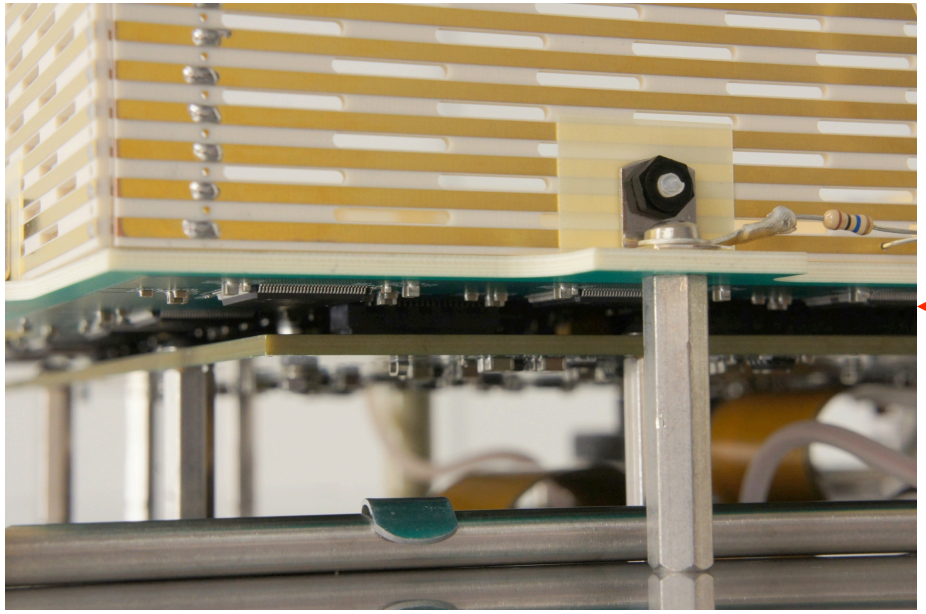
Back side of electrode



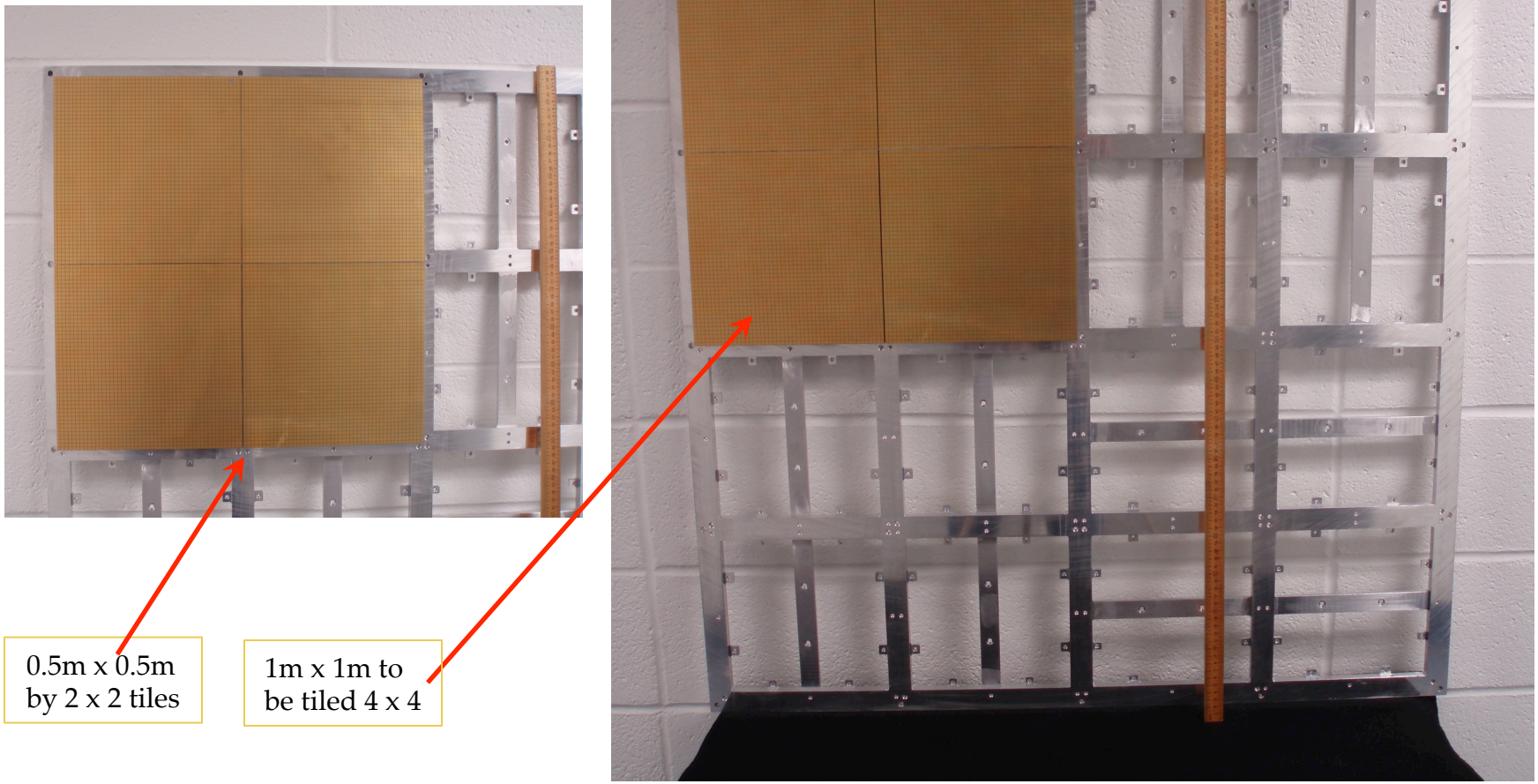
FPGA board mounted on the ASIC board



Assembly of eletrode & electronics



An Example of Pad Readout



- **Scaling up to 1m x 1m will be already very challenging: steady state power for TPC readout ~ 800 watts/m^2.**

Summary

- ArgonCube is a modular LAr TPC design, with very challenging requirements for pad readout
- It offers a good opportunity for many R&D studies
  - Sense electrode configuration
  - Pad readout design with power switching
- Cold ASIC advancement for SBND and protoDUNE can be used in the ArgonCube Phase-1 R&D
- One can develop a staged program with test beam at CERN for ArgonCube Phase-2 R&D
  - Start from wire electrode, to possibly strip electrode and finally pad electrode, to exercise different readout schemes
  - Testing and commissioning of a TPC with pulsed power readout will be much more involved than of the continuously powered TPC (which already presents a challenge).