TDAQ → TDR

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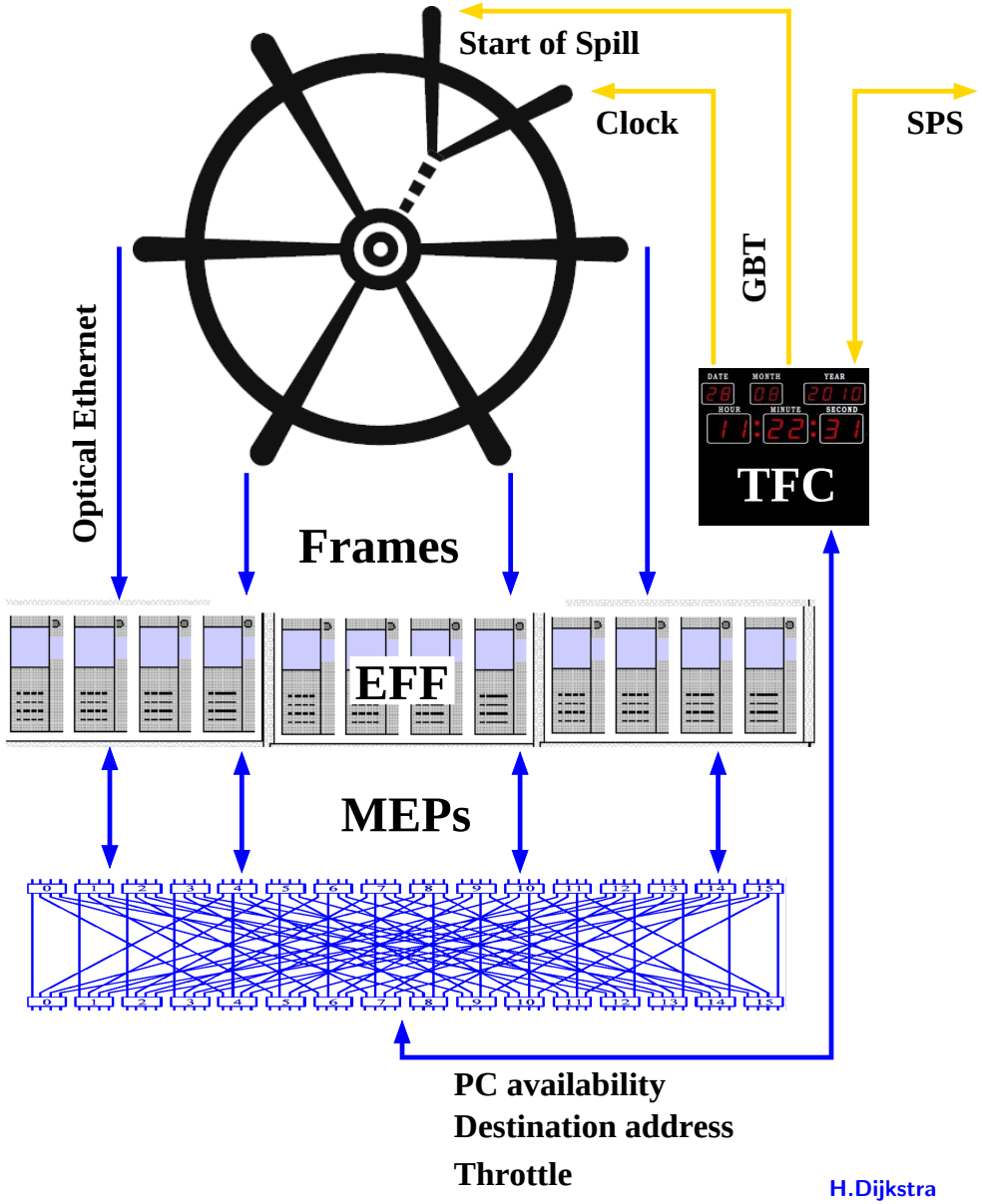
- Reminder new layout of DAQ.
- Progress on demonstrator for the TDR.
- Your DAQ needs you!

New DAQ Layout Reminder

- TFC: only clock/start of cycle → FE
- FE sends frames → PC-NIC
- PCs: built (JUMBO)MEPs, throttles and send to destination via switch.

For more details: see backup slides.



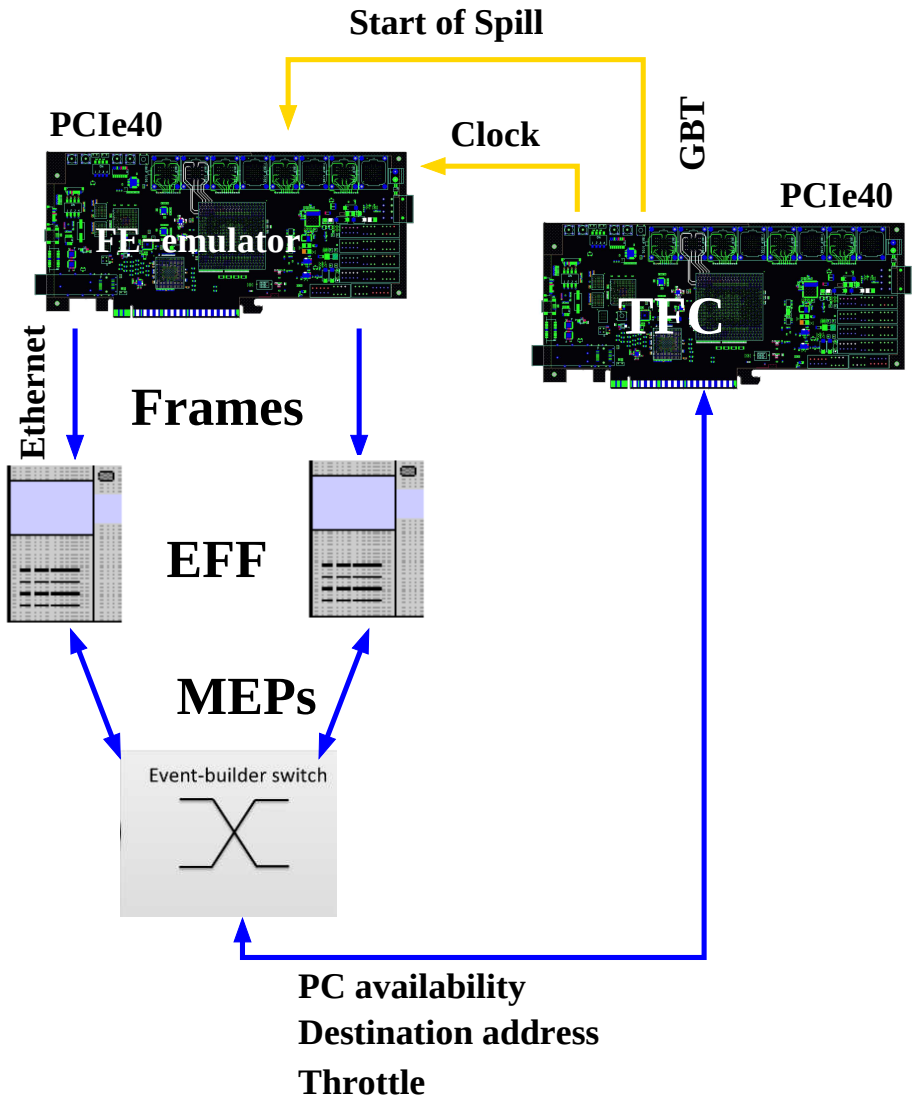
TDR Demonstrator

Hardware:

- TFC: use LHCb-PCIe40 board?
- FEs: emulate with PCIe40 board?
- 2 PCs with I/O NICs.
- Switch to connect PCs.

Really core of real system:

- TFC: could be final one.
- FE-emulation: could produce many Ethernet links, with different phases/link etc..
- MEP and Event building software: could be final one.
- Only need to scale number of PCs and Switch.



Steps towards Demonstrator

Put following milestones in Addendum to SPSC:

- Definition of the common readout protocol: Q3/2016
- TDAQ demonstrator performance evaluated: Q3/2017
- Readout control specification for FE and BE: Q3/2018

Present status:

- Uppsala takes responsibility for TFC. In contact with LHCb. Studying what is the most promising solution to implement TFC.
- FE-emulation:
  - We will built our own emulator. Investigating what is "cheapest" way, commercial card, or LHCb line?
  - We invite one or two FE developpers to contact us, so that we can "ping" with them instead of working in the vacuum. No hurry, sometime next year to start discussion?
- PC software+emulation: manpower needed!
  "New" institute might be interested, under discussion.

SHiP

Conclusion

- Evaluating best choices for Demonstrator.
- Which sub-det(s) can we contact to discuss best FE$\leftrightarrow$DAQ interface?
- Still looking for manpower!

SHiP

BACKUP SLIDES

New DAQ Discussion

- FE↔DAQ much simpler:
  - FE just have to put their data on an optical Ethernet link.
  - Point↔point link to a PC-NIC. Many low occupancy links (150 RPC links!): aggregate switches (say 31→1) in between FE and PC. But: always one destination/FE-link, given during configuration.
  - FE does not throttle, just truncate in case its own buffer is full, and set truncation bit for this frame.
  - Less buffer needed in FE, since it can send Frames (say every 100 ns).
  - Only caveat:
    - FE used to send MEPs (with >600 Bytes/MEP)/Ethernet package.
    - Now could send "Frames" of ~ 10 Bytes, but Ethernet overhead/package ~ 40 Bytes.
    - Up to FE to pack more frames into one Ethernet package to reduce overhead fraction.
- TFC does the same as before:
  - It generates the clock, and transmits start of SPS-cycle over GBT → FE.
  - It receives availability from PC (via Ethernet from the switch).
  - Iso sending destination/throttle to FE, it now sends it over Ethernet via the switch to all PCs.
- New role of the PCs:
  - PC now has to built MEPs from the frames it receives.
  - Drop those MEPs throttled by the TFC if there is no free PC buffer for them.
  - It should add the destination to the MEPs, and send them of via the switch to a PCs.
- Use NICs iso PCIe40 cards: cheaper!
- PCs like before do event building, and run trigger software.

DAQ Data-Formats

FE Frame: A frame length of 100 ns would suffice for most sub-detectors. Using the start of the SPS-cycle to synchronize the different sub-detectors. Note: clock will be 40 MHz.

Frame-size (2B)	J $(4B)$	Source-ID(2B)	Truncated(1b)	Version(7b)	Data of frame

J = frame # in a SPS-cycle.
Source-ID: point-point FE-PCNIC connection, but aggregate multi-FE into one before the PCs.
One Byte (avoid overhead ☺) for (truncation bit + version#)

Below what is happening on the PCs:

- Multi Event Package (MEP): put all data of one cycle in "JUMBO" MEP on its PC.

MEP-size(4B)	Cycle#(4B)	Source-PC(2B)	Magic(2B)	Data

Data contains:

Frame$_{J=0}$	.....	Frame$_{J=\text{last of cycle}(=72\times10^6\ ?)}$

TFC collects availability from PCs, and distribute the MEPs/cycle destination to PCs, over the switch.

- Event: all MEPs of a SPS-cycle are routed to the same PC in the EFF.
One PC will run the trigger code on one full SPS-cycle of say 7.2 seconds.
If the trigger selects a group of frames, it will produce an "Event", which will then be written to storage. The data format of an event:

Event-size	Trigger header	Trigger data	Cycle#	Frames$_{K-n}$	.....	Frames$_{K+n}$

No duplication of events anymore due to JUMBO-MEPs (thanks Federico Alessio!)

Miscellaneous

Sub-det	Target Tracker	RPC	Drift Tubes	BckGr Tagger	Veto Taggers	Spectr Tracker	Calo	Muon
#-channels	120k	8.2k	4k	1.7k	0.8k	41k	13k	8k
Time window (ns)	350	100	1500	50	50	250	100	30
Data size (Bytes)	28/hit	3/hit	3/hit	4/hit	5/hit	3/hit	160/cl.	3/hit
Hits/particle	10	22	40	2	2	40	1	16
Ethernet links	few	150	10	few	few	few	16	20

- Compare data rates: LHCb will have a few TB/s, while SHiP is estimated to transfer few GB/s.
- Prefer optical Ethernet (400 m) iso GBT: this means "no" radiation at FE.
- Radio-protection note:
  https://edms.cern.ch/edmsui/#!master/navigator/document?D:1185319677:1185319677:subDocs
- Mario Campanelli trying to follow this up:
  - Where are the FEs of the sub-detectors located?
  - What is the radiation level? Preliminary: < 100 Gy (for 2×10^{20} POT)
- If there is a FE which needs/wants GBT to send data: no problem!
  Just need to buy PCIe40 for those PCs which receive this FE-info.