HV-HR CMOS Detectors for FCC-ee (and also hh)

ITK

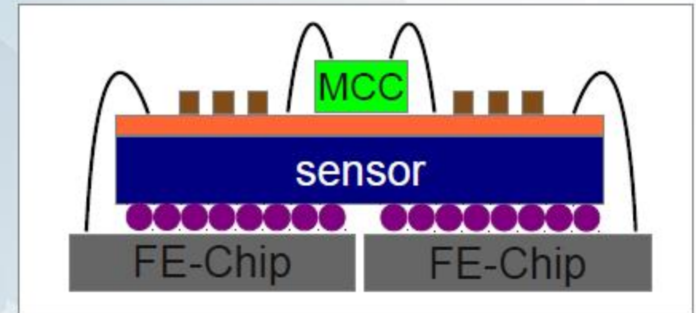
General considerations for Si tracking at FCC

- FCC-ee
  - Cost of present (planar pixels):
    - Sensor 25-40 euro/cm2
    - FE : 14 euro/cm2
    - Bump-bonding : 40-45 euro/cm2
  - Low amount of material <<1% X0 per layer
  - Granularity : few μ pitch
- FCC-hh
  - Radiation hardness
  - Low power (for cooling)

Silicon Hybrid Detectors

<u>Features</u>

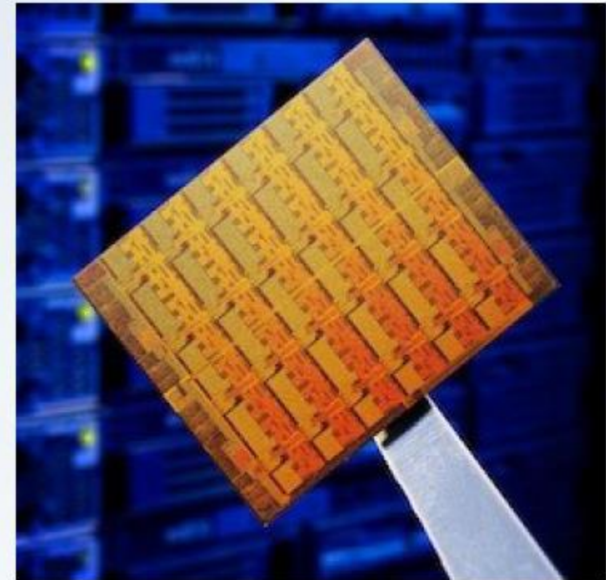
- high signal and high noise
- complex compound
- bump bonding
- wire wrapping
- custom-made sensor
- lots of material (radiation lengths!)



- expensive (e.g. ATLAS II pixel HW: 16 mill.CHF for ~5m^2)
- scalability problem (e.g. Future experiments at FCC)
- miniaturization problem >10^8/m^2 bump bonds?
- quality assurance problem

CMOS Features

- minimum pixel size 10-20 feature size
  → 5μm possible!!!
- low power (CMOS)
- low noise compared to hybrids
- compact VLSI design
- standard process
- cheap



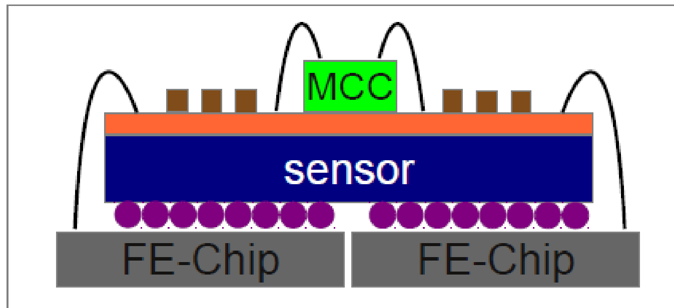
Hybrid versus Monolithic

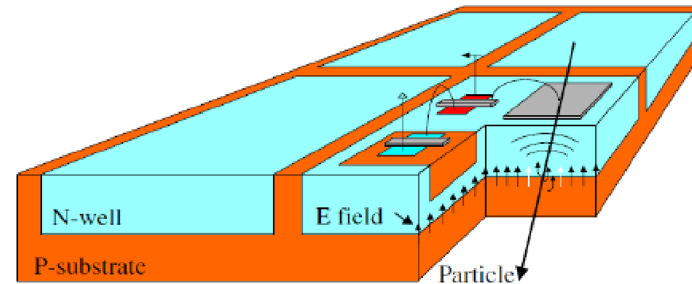
<u>Hybrid design</u>

- high signal
- high noise
- lot of material
- many interconnections
- minimum pixel size limited by bump bonds
- expensive (connections!)
- complex production

<u>Monolithic design</u>

- low signal — can be increased!
- low noise
- 50 µm thickness possible → Mu3e
- only few connections
- minimum pixel size only limited by features size — ~4x4 μm^2 for 180nm
- cheap CMOS process
- easier (faster) to construct?





CCPD – Capacitively Coupled Pixel Detectors

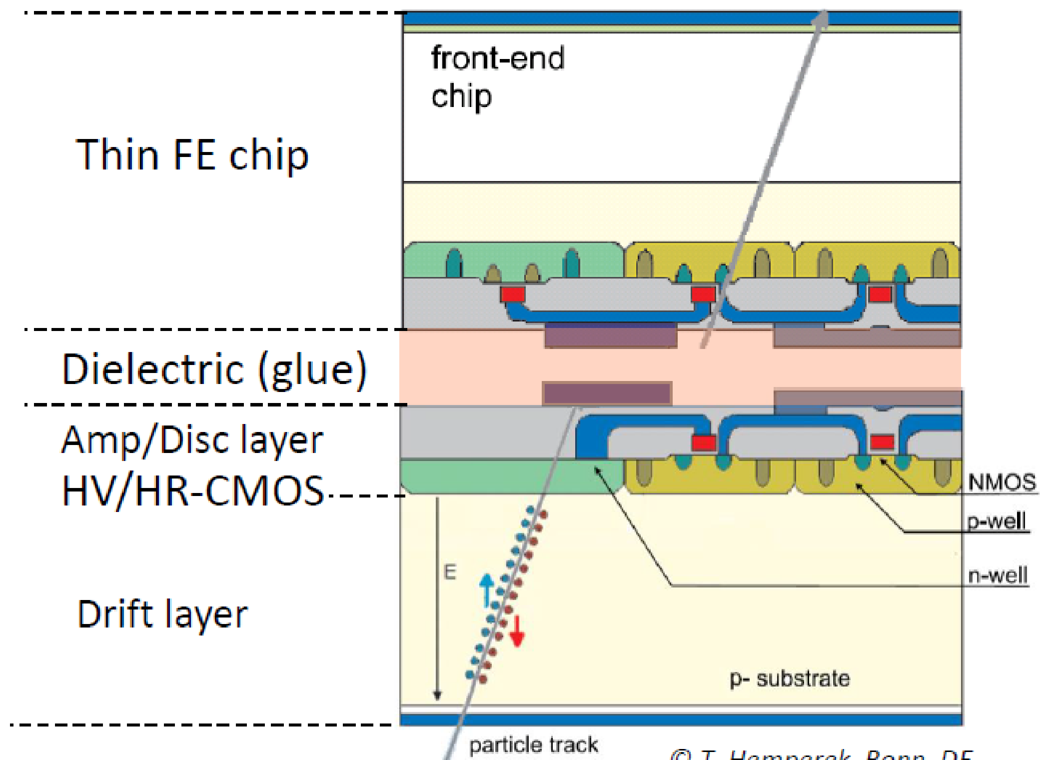
New generation of Pixel detectors under development for the ATLAS Pixel detector at the HL-LHC

- Passive hybrid detectors use “resistive” coupling between sensor and R/O chip
- HV-CMOS detector use a High Voltage chip technology to make sensor and amplifier which is then coupled to the “usual” front-end chip…

- through a dielectric…

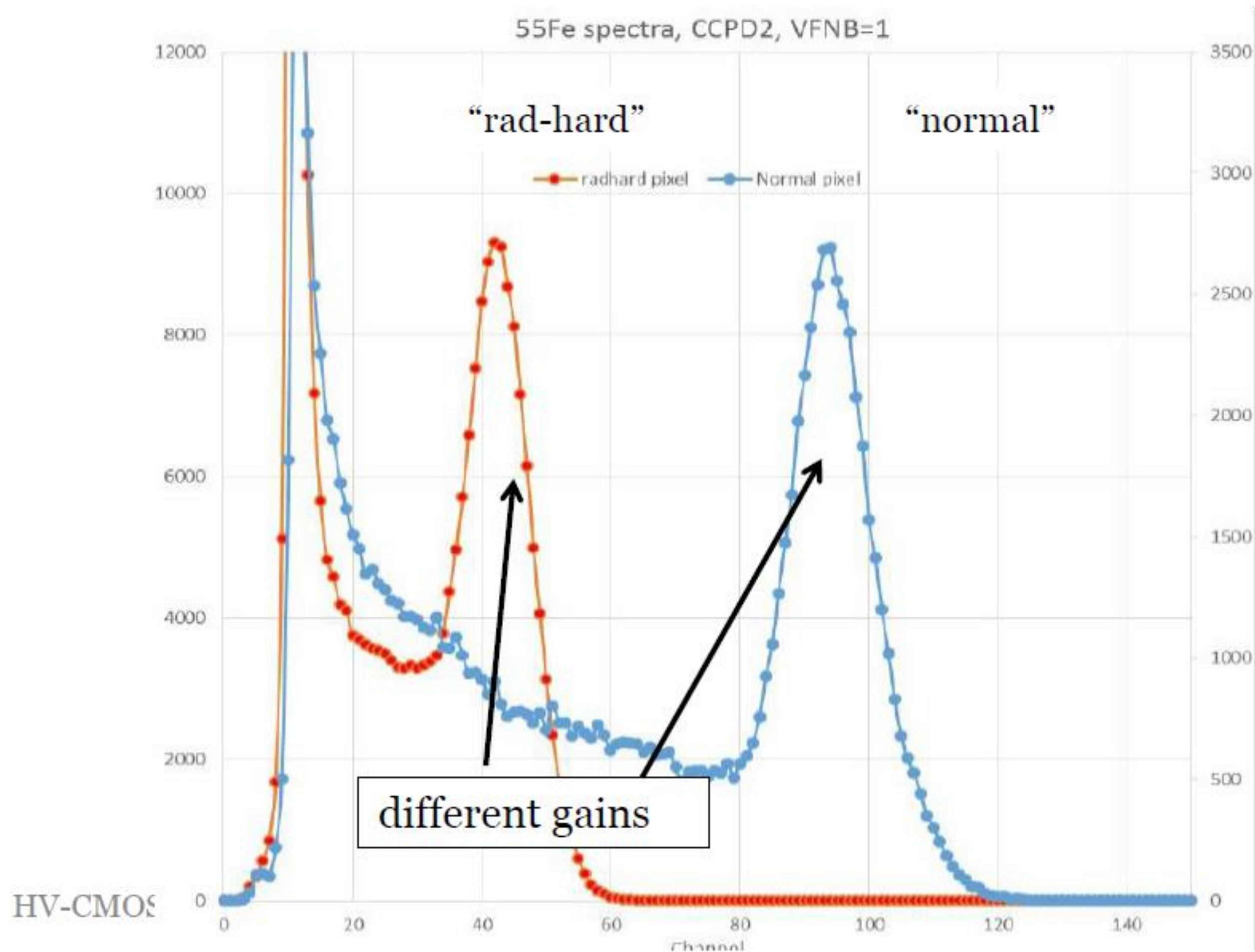
Why capacitive?

- Passive sensors need diode biasing from amplifier other than for collecting charge: AC coupling is (almost) not an option.
- **Capacitive coupling it might be cheaper**: glue and alignment looks easier.



HV2FEI4_V2

- Few pixel flavors with enhanced rad-hardness: guard rings, circular transistors… (different pixel types lead to different gains -expected-).



(Some) Requirements

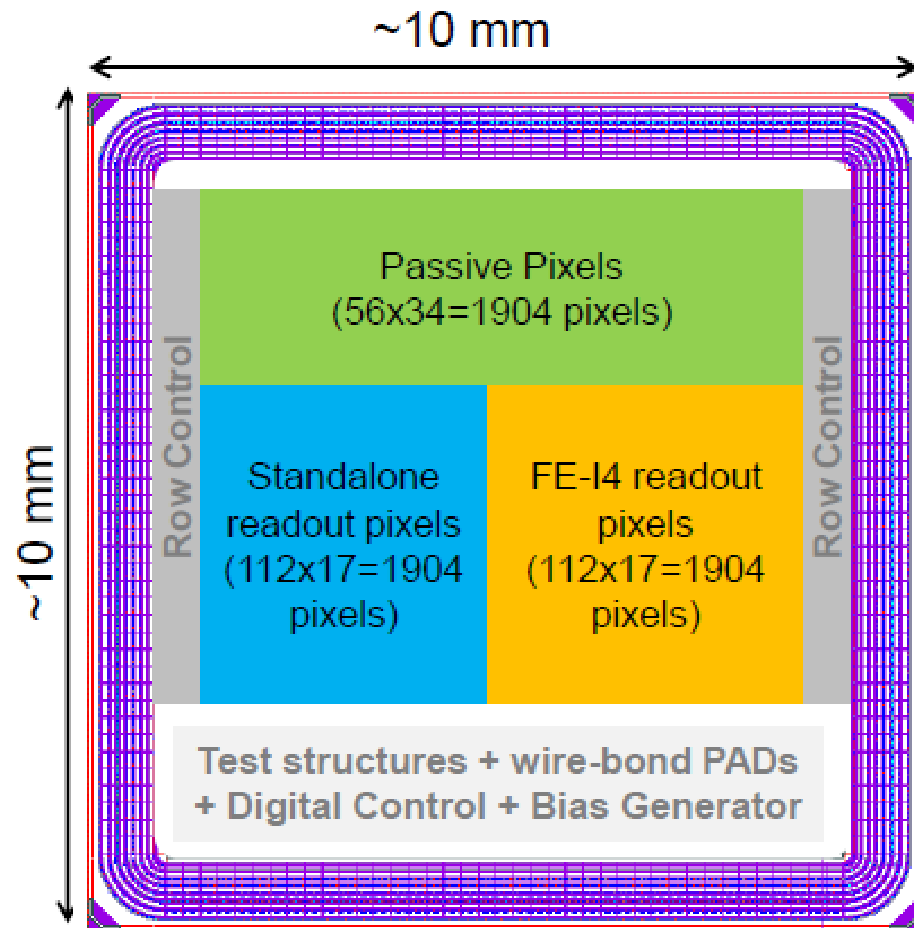
- *Capacitance uniformity*
  - Between pixels, from an assembly to another: ~10 % → thickness uniformity
  - Most critical for analog coupling (no discriminator in the HV/HR-CMOS)
  - RD-53 chips will have 50µm pitch, but also versions for very small pixels: 25µm pitches are considered
  - X-Y alignment: better than few µm (cross talk / signal loss)
- *Glue requirements*
  - Low viscosity: 0.1 ÷ 0.5 Pas
  - Radiation hard: epoxy
  - Not degassing
  - Low temperature curing, investigating UV/Temp curing glues
  - Minimum thickness of glue to give for full adhesion (usual specs are 1-2 mil, but we want less!)
- *For chip-to-wafer and wafer to wafer TVS are needed on one or both facing chips*
  - For the moment we are looking at chip-to-chip processes

Irfu activities

- Participation to the design of a 150 nm Lfoundry demonstrator chip (in HL-LHC context)
- Interest to start R&D on the mechanical aspects of capacitive coupling
- Expertise developed will be useful for FCC-ee
- Monolithic pixels (HV-MAPS) best choice for FCC-ee, given low expected occupancy

DEMONSTRATOR

- Process: **LFoundry 150nm HV-CMOS**
- Bonn, CPPM, IRFU collaboration
- Based on 2 previous prototypes (pixel electronics **inside/outside** detection diode) designed by Bonn&CPPM
- Passive, digital, and analog output pixels
- Pixel properties:
  - Pitch: **250µmx50µm**
  - Peaking time: **~20 ns**
  - Power dissipation: **~20µW** (analog)
  - Detector capacitance: 200-400fF
  - Noise : **100-250e-**
- Re-use of already validated peripheral circuits
- Submission foreseen for **September 2015**



Demonstrator layout