VFC-HD

STATUS @17-07-2015

STATUS

- 2 Boards received:
  - 1 working as received
  - 1 needing rework and now functional
- Performed tests:
  - SFP tested at 6.5Gbps
  - FMC lines tested including Gbit lanes at 6.5Gbps
  - VME interfacing
  - PROMs including the FPGA programming one
  - Clock sources and voltage controlled oscillators
  - Utilities: GPIO, Unique ID and temperature monitoring chip, Voltage monitoring and control, I2C expanders and Muxes, …..
- Missing DDR3 test

DISCOVERED BUGS

- One clock polarity inversion
- Push button not connected
- Signals at 3.3V arriving on the DDR3 bank
  - FMC_CLK2BIDIR
  - BLM Daisy chain
  - P0HwLowByte
- CERN PS can have short circuit and needs to be soldered by hand or an extra PCB should be added between the VFC and the module to act as passive spacer

DDR3 CONSIDERATIONS

- Concerns:
  - The max frequency for a DDR interface on the ARRIA V is 600MHz -> fastest standard supported is DDR3-1066 (maybe 1333)
  - Fly-by not supported (always there in DDR3 SO-DIMM)
- Options:
  - Go for DDR2 as it doesn't use fly-by topologies in DIMMs
  - Run the DDR3 at lower speed (we are anyway forced to do so)
  - Make our own SO-DIMM module with a clock buffer (no fly by)