# Status of digital integration electronics

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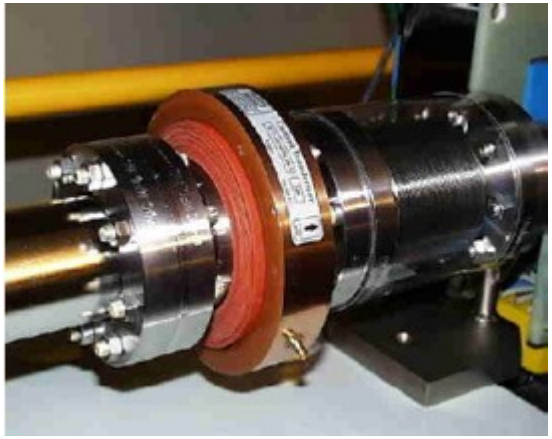
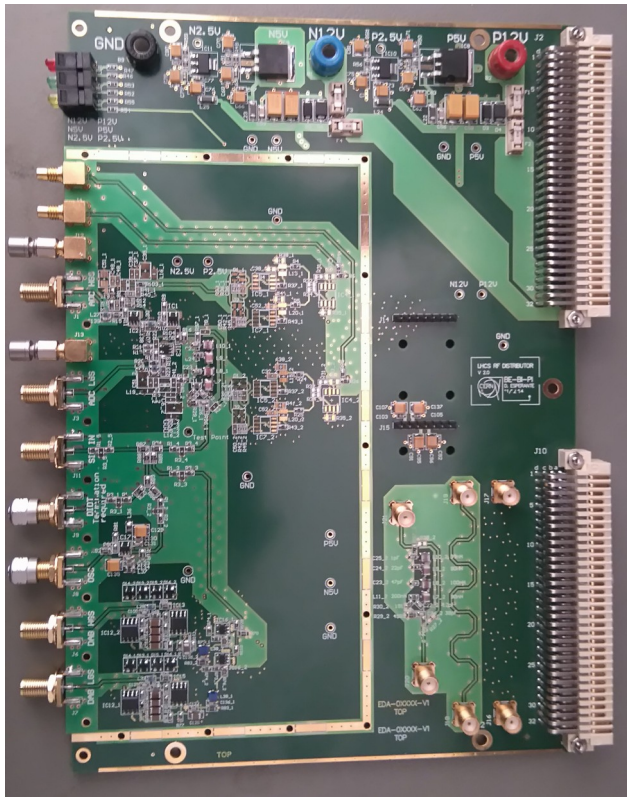
# Overview

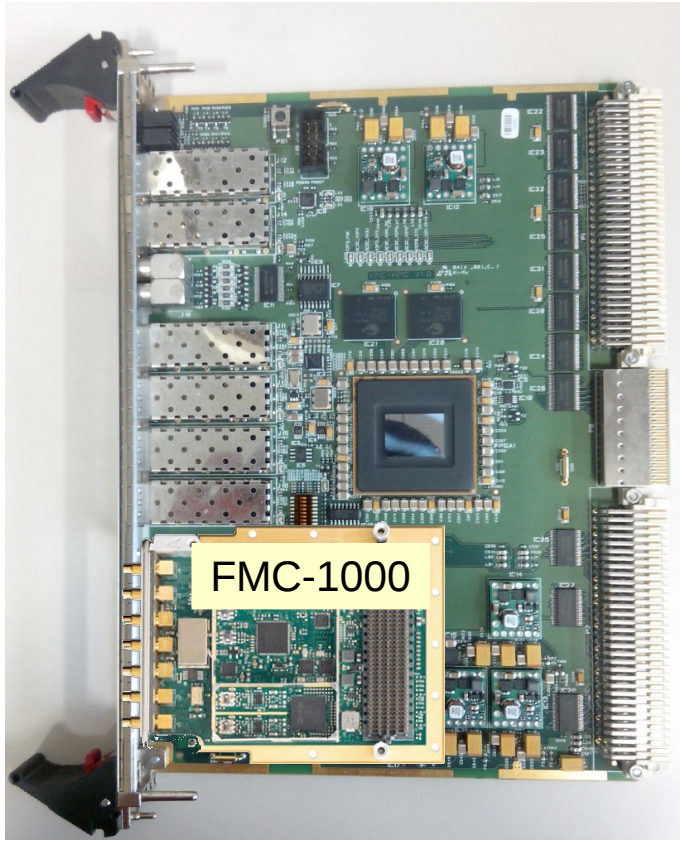
- Up to 1 GSPS digital sampling to replace used analog integrators
  - 600 MSPS currently due to VFC FPGA transceiver limitation
  - Expecting production of VFC with Arria V GT (10 GSPS limit)

- Current status
  - Received FMC-1000 hardware from Innovative (May 21st)
  - First beam tests at SPS (since July 8th)
  - Demonstration project for JESD204B link available

# Basic idea








BCT

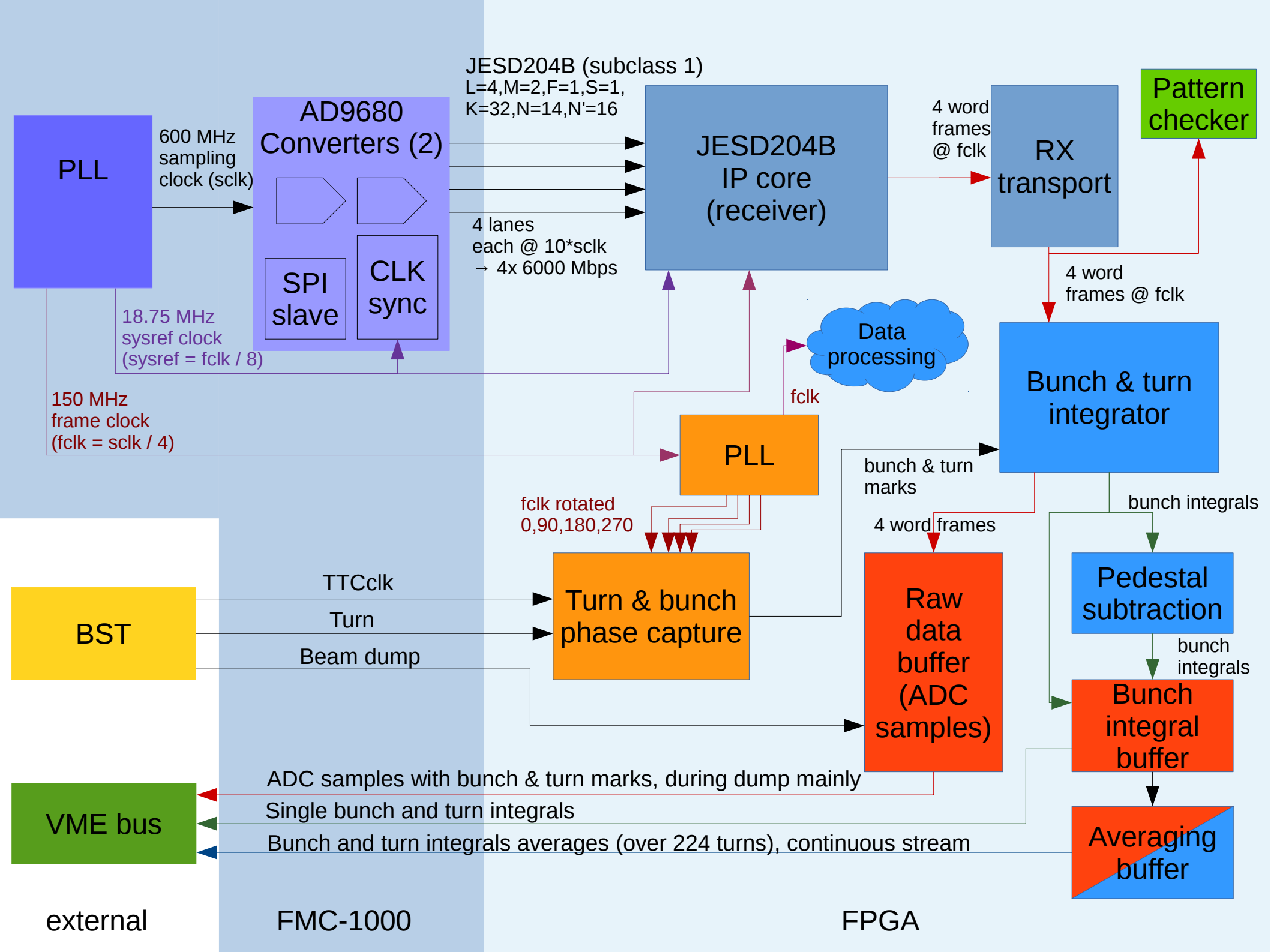
FBCT/ICT(Bergoz)
BCTW

RF distributor

Low/High gain
Gaussian filter

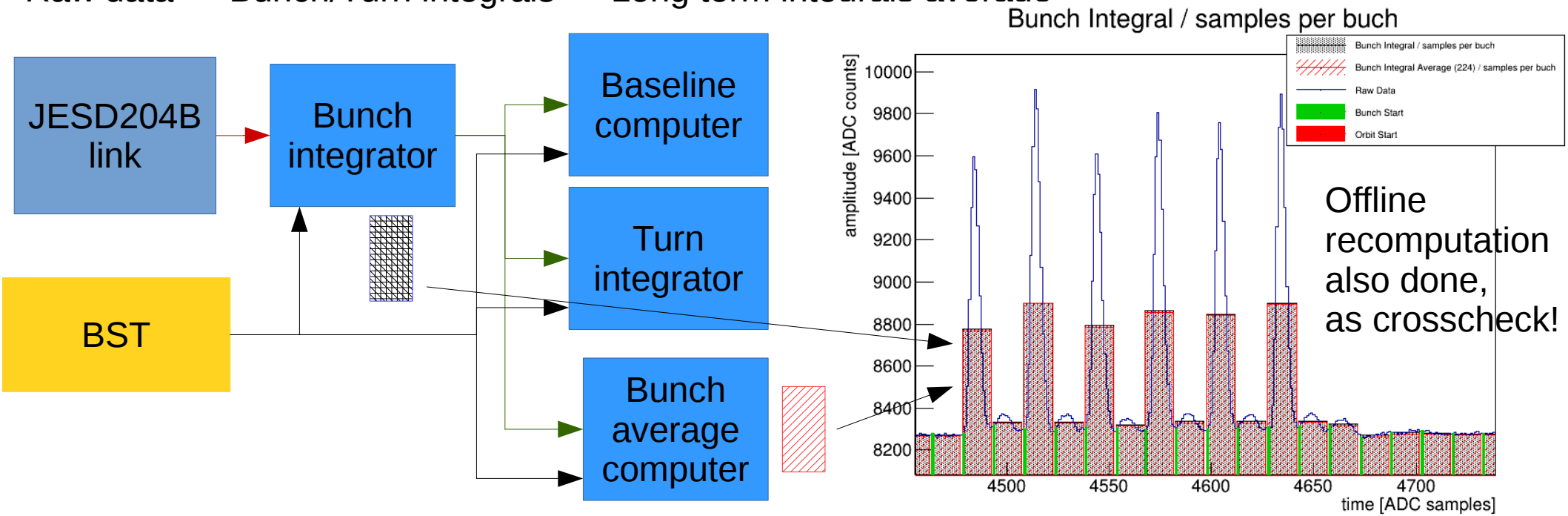
VFC carrier
+ FMC-1000

VME


JESD204B (subclass 1)
L=4,M=2,F=1,S=1,
K=32,N=14,N'=16
PLL
600 MHz
sampling
clock (sclk)
AD9680
Converters (2)
SPI
slave
CLK
sync
4 lanes
each @ 10*sclk
→ 4x 6000 Mbps
JESD204B
IP core
(receiver)
4 word
frames
@ fclk
RX
transport
Pattern
checker
4 word
frames @ fclk
18.75 MHz
sysref clock
(sysref = fclk / 8)
Data
processing
Bunch & turn
integrator
150 MHz
frame clock
(fclk = sclk / 4)
fclk
PLL
bunch & turn
marks
bunch integrals
fclk rotated
0,90,180,270
4 word frames
TTCclk
Turn
Beam dump
BST
Turn & bunch
phase capture
Raw
data
buffer
(ADC
samples)
Pedestal
subtraction
bunch
integrals
Bunch
integral
buffer
ADC samples with bunch & turn marks, during dump mainly
Single bunch and turn integrals
Bunch and turn integrals averages (over 224 turns), continuous stream
VME bus
Averaging
buffer
external
FMC-1000
FPGA

# Data processing in FPGA

Raw data → Bunch/Turn integrals → Long term integrals average




- Bunch margins identified by sampling the bunch/turn clock, identical # of ADC samples per bunch → unused samples
- Baseline acquired each turn during abort gap
  - Baseline subtraction ON/OFF possibility
- Automatic machine (LHC/SPS) ID based on BST

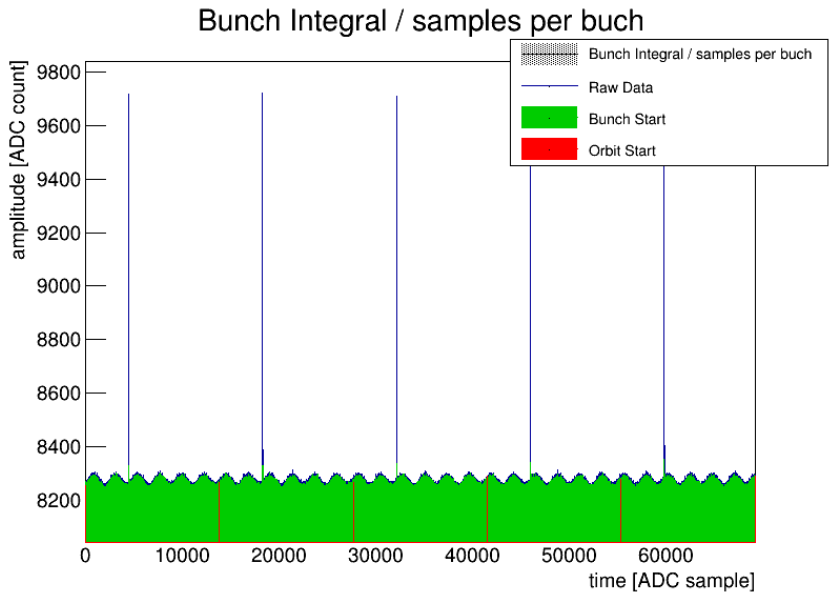
# Available measurements

- Continuous
  - Per bunch integral long term average with selectable averaging period (# of turns)
  - Turn integral long term average, same period
  - Start of averaging time stamped

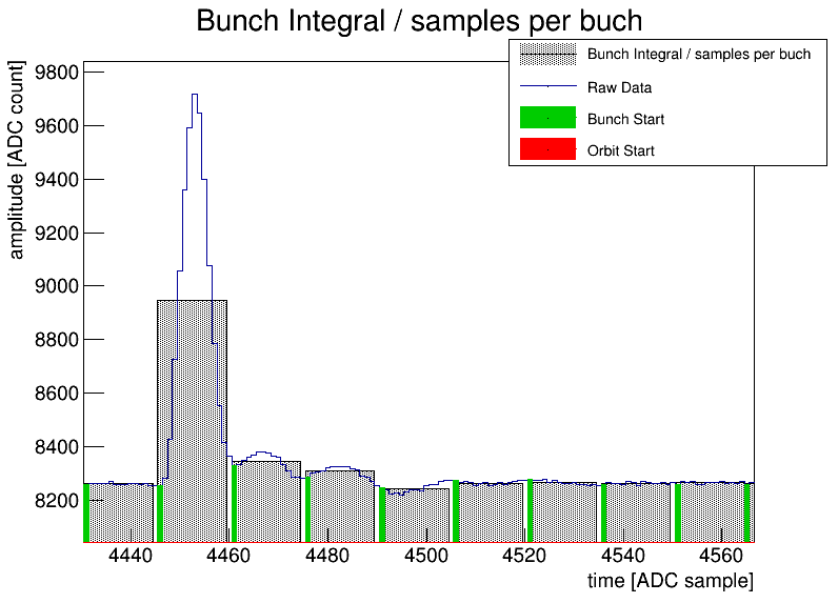
- Triggered (dumps)
  - Raw ADC data
  - Bunch integrals
  - Baseline
  - Turn integral
  - Dump start time stamped

# Beam tests – single bunch

5 consecutive turns of single bunch fill

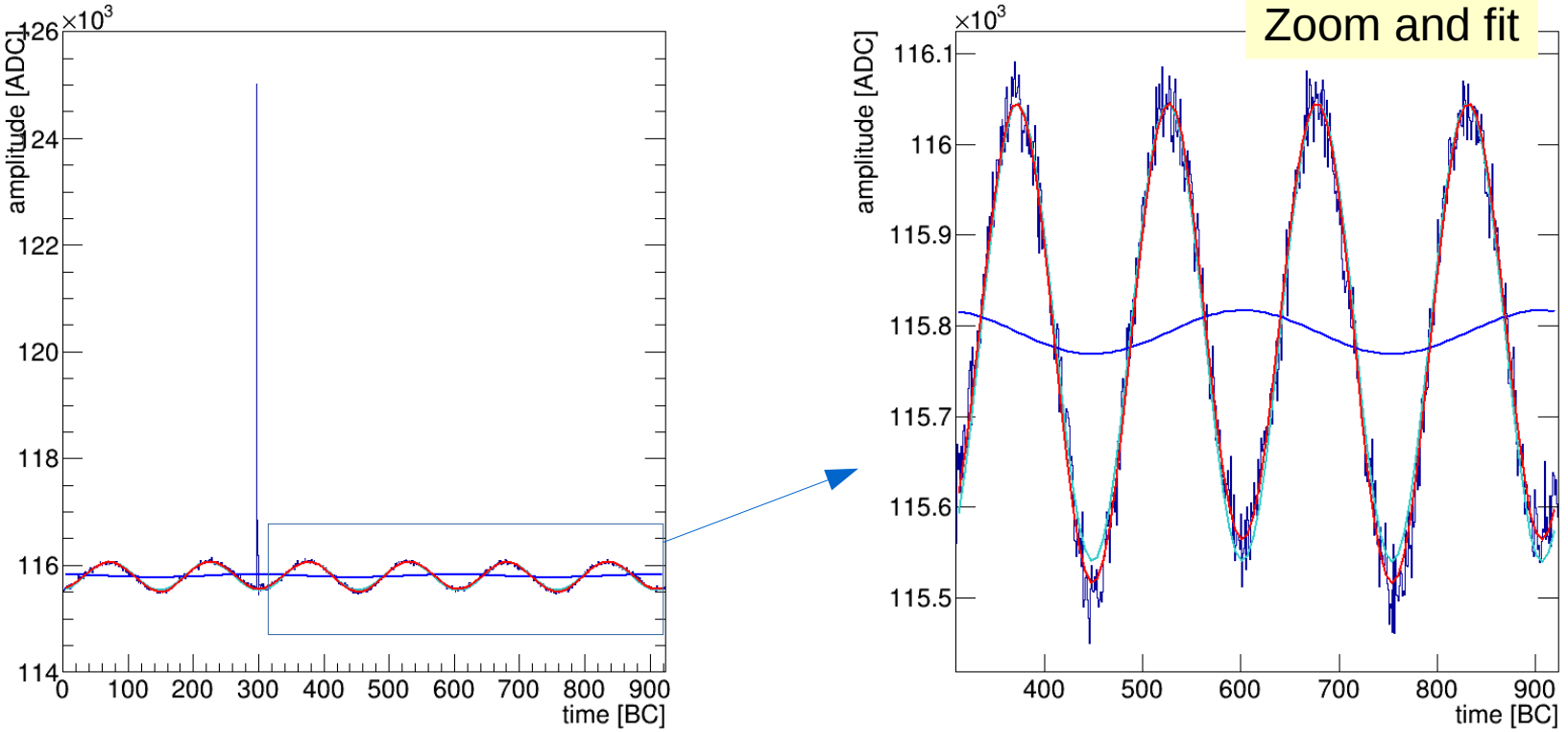



Zoom in



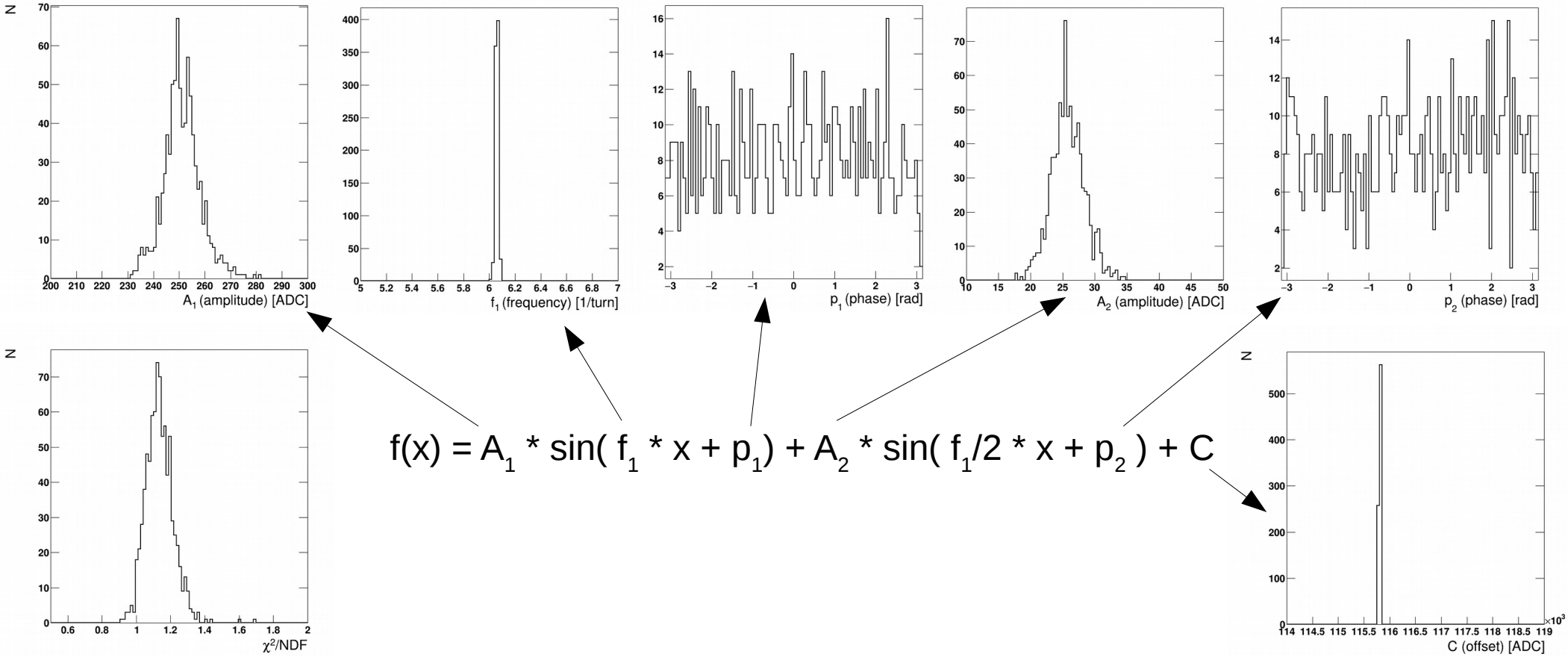

- Installation at SPS, BA3
  - FBCT → amplifier → RF distributor → FMC-1000
  - Re-using existing setup
- Oscillating baseline observed
  - Visible on scope at amplifier output as well, not visible on amplifier input
- Single bunch signal ringing & droop observed
  - Observed in front of amplifier as well, with scope → needs to be quantified

# Baseline subtraction



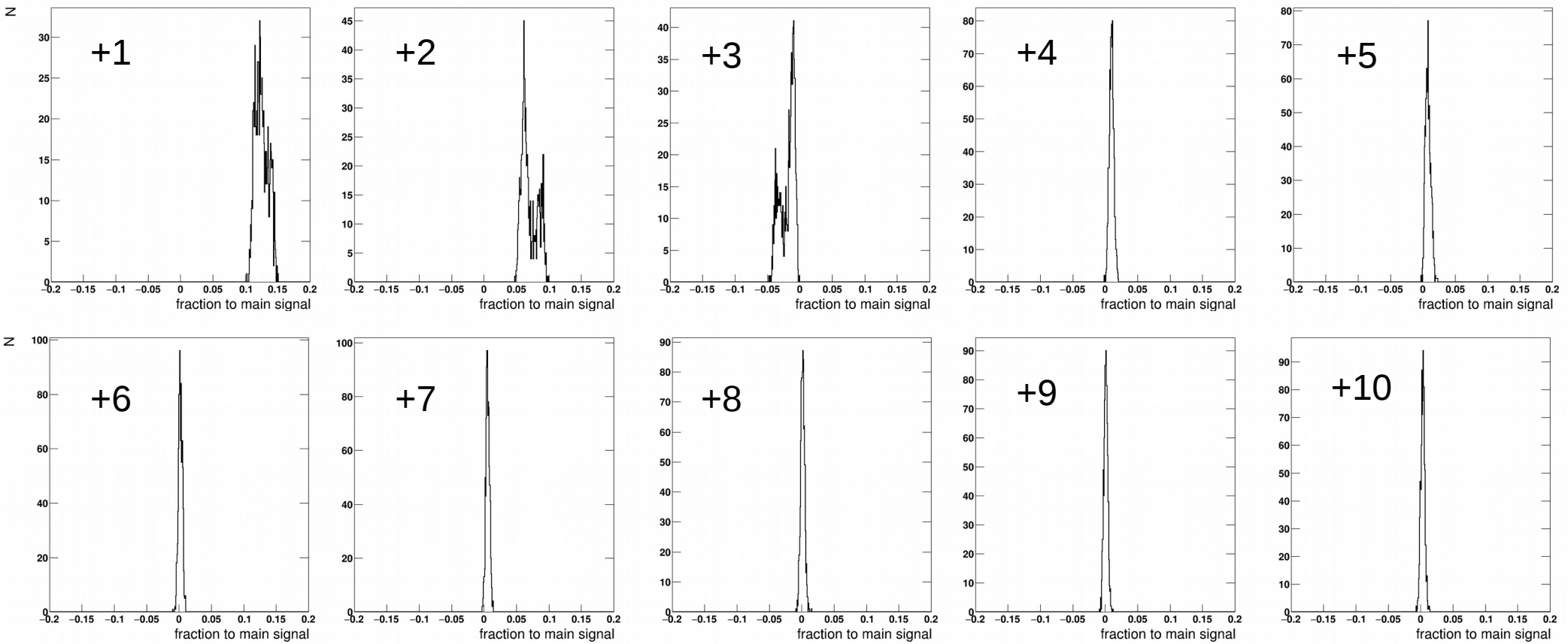

- Working with bunch integrals from now on
- Double sin fit of two consecutive harmonics
  - $f(x) = A_1 * \sin( f_1 * x + p_1) + A_2 * \sin( f_1/2 * x + p_2 ) + C$

# Background fit results

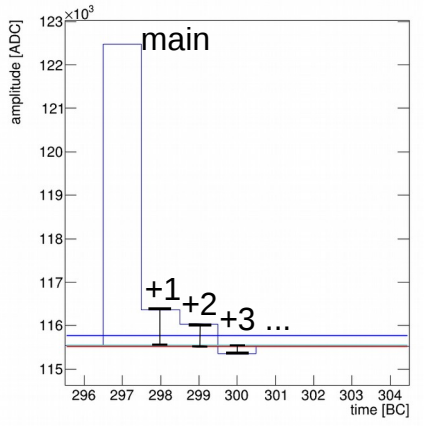



- Stable frequency and offset, unstable phase
  - In respect to turn start
  - $f_1$ = 6.06 turn$^{-1}$
- Fit can be used to extrapolate baseline below signal on per dump bases

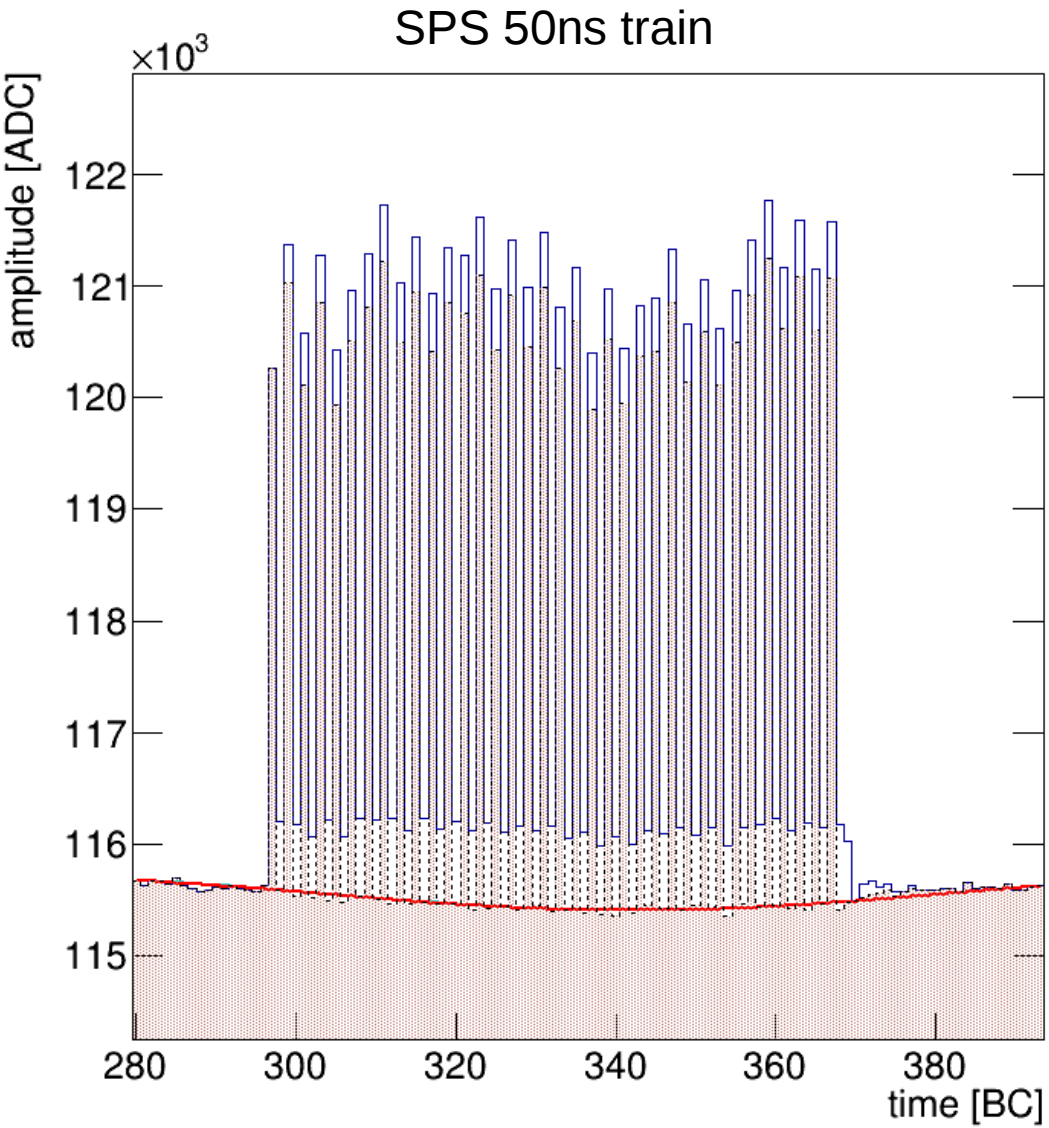
# Deconvolution of ringing



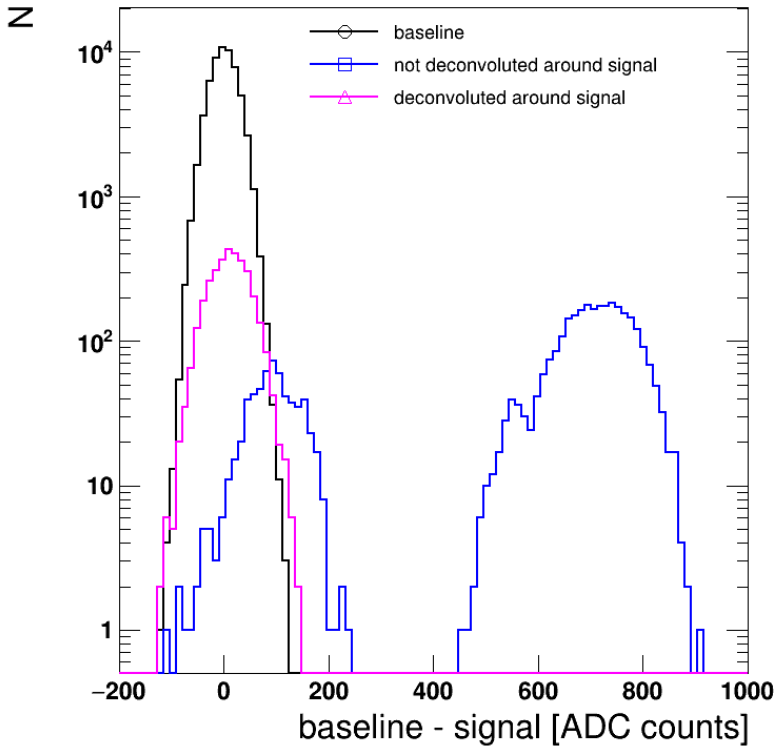

- Signal to baseline extrapolation difference
  - For bunches following the main signal
  - Plotted as a fraction of the main signal
  - Sampling phase effects observed



# Deconvolution application




- Simple deconvolution of 10 consecutive bunches seems to give reasonable results



# Near future

- Try to understand the oscillating baseline
  - Not hurrying to implement subtraction in FPGA, since the effect might be specific to the temporarily used setup
- Adapt FPGA code for 2 parallel ADC channels
  - Running single channel code so far
- Prepare FPGA code for frequency increase to 1 GSPS
  - Requires parallelization, since the FPGA fabric can not work with 250 MHz frame clock

- Write documentation
- Calibration setup preparation

# Already existing outputs

- Arria V GX example project with AD9680 dev board showing JESD204B core implementation
- Development versions of Arria V GX project with AD9680 dev board or FMC-1000 implementing the whole functionality

- Preliminary register/memory map
- Basic python scripts to configure/pull data