The control system of the ATLAS Level-1 Muon Barrel Trigger

V.Bocci[†], G.Chiodi[†], G.Ciapetti[†], D.De Pedis[†], A.Di Mattia[†], A.Di Girolamo[†], E.Gennari[†], C.Luci[†], A.Nisati[†], E.Pasqualucci[†], Fr.Pastore[†], E.Petrolo[†], F.Spila[†], R.Vari[†], S.Veneziano[* †], L.Zanello[†], G.Aielli[‡], R.Cardarelli[‡], A.Di Ciaccio[‡], A.Di Simone[‡], L.Di Stante[‡], A.Salamon[‡], R.Santonico[‡], A.Aloisio[§], M.G.Alviggi[§], V.Canale[§], G.Carlino[§], F.Conventi[§], R.De Asmundis[§], M.Della Pietra[§], D.Della Volpe[§], P.Iengo[§], V.Izzo[§], A.Migliaccio[§], S.Patricelli[§], G.Sekhniaidze[§], M.Bianco,[¶], G.Chiodini,[¶], M.R.Coluccia,[¶], E.Gorini[¶], F.Grancagnolo[¶], R.Perrino[¶], M.Primavera[¶], S.Spagnolo[¶], V.Aprodu[‖], D.Bartos[‖], S.Buda[‖], S.Constantin[‖], M.Dogaru[‖], C.Magureanu[‖], M.Pectu[‖], L.Prodan[‖], A.Rusu[‖], C.Uroseviteanu[‖]

Abstract

The ATLAS Level-1 Barrel Muon system [1] is devoted to identify muons crossing the two outer Resistive Plate Chambers (RPC) stations of the Barrel Spectrometer, passing a set of programmable p_t thresholds, to find their position with a granularity of $\Delta\eta \times \Delta\phi \simeq 0.1 \times 0.1$, and to associate them to a specific bunch crossing number. The system sends this trigger information to the Central Trigger Processor within a fixed latency of about one microsecond. The system is also responsible to record Resistive Plate Detector hits, to provide muon track position with a spatial resolution of about 1 cm to higher level triggers, to refine precision chambers' data and for monitoring purposes. The system is hardware based but its high level of programmability and its deployment in the cavern poses many requirements to its control data path. The control system has to be reliable, it has to survive to an amount of radiation comparable to conditions of space devices, and has to connect about 800 on-detector processor destination boxes spread over a large area. The choice which has been implemented uses a field-bus based system, with microcontroller-based destination nodes taking care of initializing and controlling local devices accessible via local buses. Configuration data is stored locally for fast initialization running in parallel over all nodes. Linux-based PCs, integrated in the ATLAS data acquisition system, run initialization and control applications while reading configuration data from an Oracle database. A detailed description of the hardware and software organization of the system is done, with results from the setup used for chamber commissioning.

THE MUON BARREL SPECTROMETER

The Barrel spectrometer is divided longitudinally in two (Side-A and Side-C), and in the non-bending projection into 16 physical sectors. The physical sectors are called Large and Small, respectively if the chambers are positioned between magnet coils or inside the coil structures. Detectors are organized radially into an Inner, Middle and Outer layer. Trigger chambers are used only in the Middle and Outer Layers. One physical sector is further subdivided into two Trigger Sectors.

THE LEVEL-1 BARREL SYSTEM

The ATLAS Level-1 Barrel system is divided into an on-detector and an off-detector part, as shown in Fig.1.

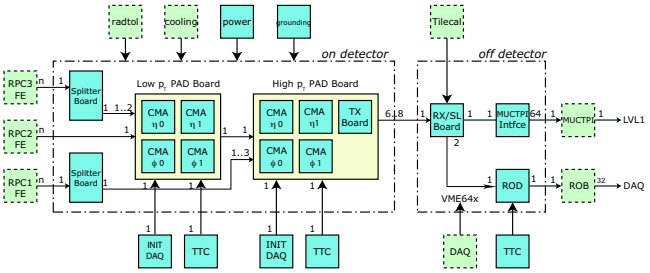

Figure 1: Block diagram of the Level-1 Barrel readout and Trigger Slice.

The on-detector part is mounted directly onto the detector stations. *Splitter boxes*, responsible for receiving and fanning-out discriminated front-end signals, and *PAD processors*, constituting the core of the RPC readout and Level-1 Trigger. Processors are organized in Trigger Towers, made of one Low and one High Pt PAD board. They are connected to each other via copper cables carrying readout and trigger data.

The off-detector part resides in VME64 [2] crates, and is made of Optical Receiver/Sector Logic Boards (RX/SL), Readout Drivers (ROD) and MUon Central Trigger Processor Interface Barrel board (MUCTPIB). The RX/SL receives readout and trigger data from all the Trigger Towers belonging to a Trigger Sector via an optical connection. It has two distinct functionalities. One one side it is part of the Level-1 pipeline, its main purposes are to find the two highest p_t candidates belonging to a Trigger Sector, assign them to an η-ϕ coordinate (RoI) and flag if

* correspondig author, email: stefano.veneziano@roma1.infn.it
† INFN Roma and Universitá di Roma "La Sapienza", Italy
‡ INFN Roma II and Universitá degli Studi di Roma "Tor Vergata", Italy
§ INFN Napoli and Universitá degli Studi di Napoli, Italy
¶ INFN Lecce and Universitá degli Studi di Lecce, Italy
‖ National Institute for Physics and Nuclear Engineering "Horia Hulubei", NIPNE-HH, Bucarest, Romania

the track is passing overlap regions between Trigger Sectors, either in the Barrel or in the interface region between Barrel and Endcap. On the other side it also has to check fragments, do the event building and ship data fragments to the Readut Driver. The ROD connects two Trigger Sectors to the ATLAS Data Acquisition System (ATDAQ). It collects readout data from two adjacent RX/SL boards and uses a standard ReadOut Link (ROL) to send data to ReadOut Buffer INput modules (ROBINs). The MUCTPIB is a simple board which is able to drive a 10m long differential 32-bit bus connecting the RX/SL trigger output to the MUon Central Trigger Processor Interface MUCTPI Input processor boards. The MUCTPI collects trigger data from the Level-1 Barrel and Endcap systems and communicates with the Central Trigger Processor, which takes the final decision on the basis of a trigger menu.

The Trigger Processor (PAD)

A PAD processor board hosts a large number of configurable devices and sensors. The interface between the control bus and the local buses is the Embedded Local Monitoring Board (ELMB) [8] mezzanine. The ELMB contains a microcontroller, connected to various local buses.

The main components who need to be configured are:

- Coincidence Matrix CM ASIC [3], core readout and trigger component. Four ASICs are present into a PAD processor, and each of them comprises 158 programmable registers 8- to 64-bit wide;
- TTCrq mezzanine [5], is responsible for distributing the LHC clock and all the timing signals generated by the Central Trigger Processor and Timing Modules;
- PAD Logic FPGA (Field Programmable Gate Array), which contains the Event Building and Trigger logic responsible for assigning a Muon candidate to an η-ϕ coordinate;
- PRODE [6] Delay chips, which delay and distribute the main timing signals: Bunch Counter (BC), Level-1 Accept (L1A), Bunch Counter Reset (BCR), Event Counter Reset (ECR);
- Optical link mezzanine, which transmits trigger and readout data using a time-multiplexing algorithm assuring fixed latency for trigger data;
- temperature and voltage sensors, monitoring the main heat sources and voltage domains of the board;
- flash memories, used to store local configurations.

HARDWARE ARCHITECTURE OF THE CONTROL SYSTEM

The spectrometer arrangement drives the control system segmentation. Each detector station of the 16 Large and 16 Small Chamber sectors is controlled by a control bus, implemented in the CAN industrial standard[7]. Two control buses share a $70m$ long cable, providing CAN signals and power to the destination nodes.In terms of CAN nodes between 8 and 14 nodes share the same physical bus, running at a rate of 250 baud. A total of four control PCs are required to control the full system, each PC hosting four 4-channel CAN cards, for a total of 64 CAN buses and about 800 nodes.

The local Node

The architecture of the local node is shown in Fig 2. Each microcontroller is able to access a number of devices sharing six I2C[11], two JTAG[10] and one SPI[12] bus. A service bus is dedicated to on-board monitor of voltages and temperatures, containing registers able to switch-off portions of the board. An external bus connects PADs and Splitters mounted on the same chamber, and is used to monitor and control Splitters. The remaining buses are all used for configuring and reading back the status of the devices.

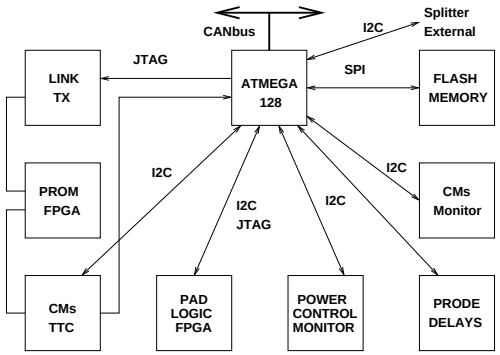

Figure 2: Local Node bus communication, controlled by the ATMEGA128 microcontroller.

SOFTWARE ARCHITECTURE

The Level-1 control software runs on two platforms communicating via the CANbus, the first platform is a linux-based PC running dedicated software based on the ATLAS Online and Dataflow framework. The second one is microcontroller-based, running custom software using the ELMB CANopen firmware framework [9]. Both platforms make use of a common set of CANopen commands (Object Dictionary), which has been customized to work in two different modes:

- remote handling of a single bus transactions;
- issuing complex commands like *Initialize* or *Check PLL locks*.

Communication is done through the exchange of Service Data Object (SDO) packets. The numbers of packets sent to complete a single transaction are shown for each kind of bus in Tab.1, while complex commands require only a single packet since their implementation is done inside the ELMB firmware.

Table 1: Number of SDO packets per local command, N is the size in bytes of the command data.

Bus transactions	No SDO packets
I2C register RW	$3 - 4 + (N \div 4)$
SPI memory RW	$3 + (N \div 4)$
JTAG block RW	$4 + (N \div 4)$

Integration with DAQ

Control and initialization of the level-1 muon system in the Barrel are carried out, into the ATLAS DAQ system, through the LVL1CTRL module. This application is able to react to commands coming from the Run Control (LOAD, CONFIG, START, UNLOAD) and issue the required actions to the on-detector electronics. Errors during configuration are reported via the Message Reporting System (MRS) to the DAQ console. Fig.3 shows the connections between LVL1CTRL and the DAQ and DCS systems. During data taking, the LVL1CTRL module can communicate with the DCS, via the DAQ-DCS Communication Software (DDC), sending periodic measurements and reporting the status of the system. No direct connection is foreseen between Level-1 control PCs and the ATLAS DCS system database (SCADA).

The online software needs to provide each control PC with the static maps of nodes connected to each communication channel.

SYSTEM CONFIGURATION

Configuration of the system can be done in two ways, either using a list of bus transaction commands executed by the remote PC, or using generic commands executed locally, implemented in the ELMB firmware. The first mode is used mainly for debug purposes while the second is used for fast initialization and control in the experiment. A standalone application is capable of handling all possible commands defined in the Object Dictionary, and to combine them for specific needs. A logging procedure is able to save on files the list of atomic commands issued to the CAN node during initialization, as an ordered set of command lists. Following the configuration command scheme described below, this file set can be optionally compiled in order to be stored locally in a binary format inside the PAD processor flash memery, and then be executed during initialization. The local flash memory size, of 8 Mbit, is large enough to contain more than one initialization type. Thus, during normal data taking, a single CAN bus transaction initialize the processor for different Cosmics or Beam run types, setting timing, thresholds, coincidence roads. Each configuration is stored in different locations of the local memory, and can be started with a single command of the Object Dictionary. Since the partitioning of the system permits to initialize all CAN buses in parallel, we expect a total fast initialization time of a few seconds for the full Barrel system.

Configuration command scheme

The structure of a binary configuration is shown in Fig.4. A configuration header is followed by a number of variable-lenght fields. Each field is a command line transformed by the microcontroller into a register access. The result of each individual access is stored and at the end of execution is available to the control PC.

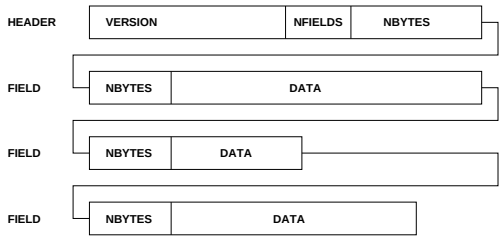

Figure 4: Structure of configuration stored in local memory.

CONFIGURATION DATABASE

Each configuration of the Level-1 Muon Barrel Trigger system is stored into a hierarchy of flat ascii files. The Configuration database manages these files, their binary version and the list of configurations currently loaded locally on the system. If the configuration required by DAQ during CONFIG is locally stored, a fast initialization will start, otherwise the Level-1 Controller will retrieve the required set of files, tagged by run type and time interval of validity, and a download will be issued to all nodes. The same procedure is required each time a change in the configuration is needed, for example after a new time calibration is processed. This operation is time consuming and should be done some time before the configuration is required, not to interfere with the data acquisition.

Configuration files structure

The hierarchy of the configuration files reflects the system architecture, organized in sectors, towers and PAD processors. At the lowest level each PAD processor is assigned a concatenation of device-specific configuration files. This structure is also functional to calibration programs, which need to treat specific parts of the current configuration, process calibration or normal data, to produce new subsets of configuration files.

SYSTEM MONITORING

An additional requirement to the Control system is the monitoring of the on-detector electronics during data taking. All PAD processors make available the following information:

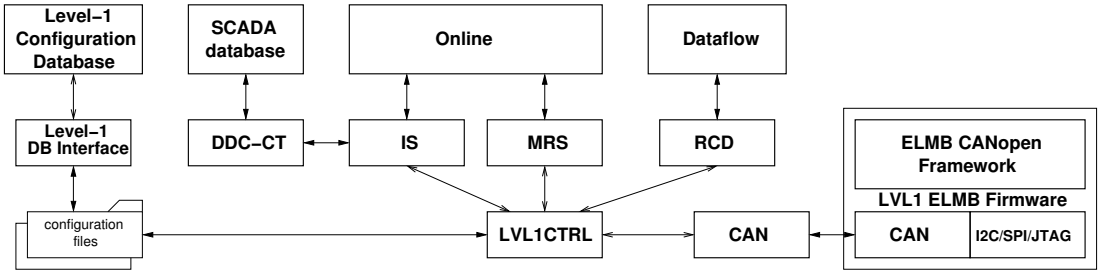

Figure 3: Block diagram of the interaction between DAQ, DCS, the LVL1 control Application (LVL1CTRL) and the PAD processor. ROD Crate DAQ (RCD) is part of the Dataflow software and is responsible for integrating detector-specific RODs into the data acquisition. Information Service (IS) is a communication tool to exchange data in the online software. The tool used to propagate the information from the DAQ to DCS has been developped within the ATLAS Online software Group, and it is called DDC (DAQ DCS Communication), it uses the infrastructure of IS. Condition (SCADA) database contains the system and detector status

- trigger rates on bending and non-bendig projections;
- status of filling of memories of the readout chain;
- main power supply voltages, all regulated voltage levels;
- temperatures of all critical devices either inside the PAD or Splitter boxes;
- alarm flags of ovecurrents due to Single Event Effects latchup;
- lock status of the TTC receiver, the CM ASICs, the FPGA, the delay chips and transmitter.

All this information has to be made available to the Condition Database, together with the RPC chamber working point.

SEU Tolerance

In order to stand the ionizing particle flux expected in the Muon Spectrometer, a number of measures have been taken or are foreseen. Each local controller monitors locally overcurrent flags and eventually turns off groups of devices. Since processors are organized in Trigger Towers connected via copper cables, it is possible to switch-off one microcontroller from the mate controller residing on the other board. These features are necessary to react to Single Event Effects which might arise from irradiation. Corruption of the CM configuration is checked by monitoring Single Event Upset (SEU) signals generated by the ASICs. Corruption of the FPGA configuration memory is also checked via read-back via JTAG. At power-up the FPGA is loaded with the content of the configuration PROM. This one can be checked, from time to time, against the content of the configuration present in the flash memory. If a difference is detected, it will start a new configuration either from the PROM or directly. A mechanism to resynchronize the affected Trigger Tower with the data acquisition flow is under study. The event building and data transmission will stop during reconfiguration and resume after successful bunch counter and event counter reset cycles.

STATUS OF THE PROJECT

A preliminary version of LVL1CTRL is currently used on ATLAS Muon cosmic-ray test stand and for the early commissioning phase. Firmware running on the local controller is complete. Integration in the Online and Dataflow ATDAQ systems is advanced, while the Database schema and access is under development now. Condition database connection is still in the design stage.

REFERENCES

[1] http://atlas.web.cern.ch/Atlas/GROUPS/MUON/TDR/Web/TDR.html.

[2] ANSI/VITA 1-1994; ANSI/VITA 1.1-1997.

[3] F. Pastore, E. Petrolo, R. Vari, S. Veneziano, Performances of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger, Proceedings of the 11th Workshop on Electronics for LHC Experiments, Heidelberg, Germany, 12-16 Sept 2005.

[4] *http://sunset.roma1.infn.it/muonl1/*.

[5] proj-qpll.web.cern.ch/proj-qpll/ttcrq.htm.

[6] A 4-channels rad-hard delay generator ASIC with 1-ns minimum time step for LHC experiments Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, Italy, 21-25 Sep 1998 (R.Vari).

[7] Controller Area Network (CAN); ISO 11898/11519.

[8] *http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/DCS/ELMB/ELMBhome.html*.

[9] *http://www.nikhef.nl/pub/departments/ct/po/html/ELMB128/ELMBfw.pdf*.

[10] IEEE 1149.1 standard.

[11] *http://www.semiconductors.philips.com/*

[12] *http://www.motorola.com/*