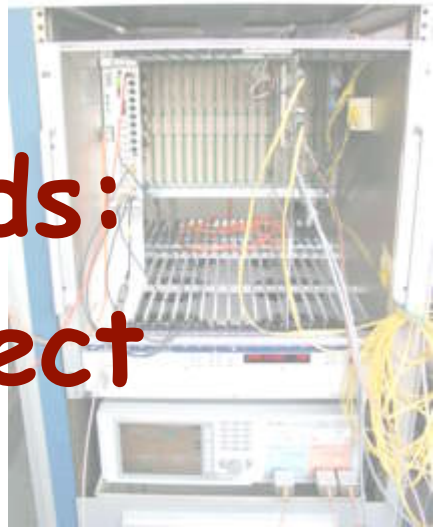
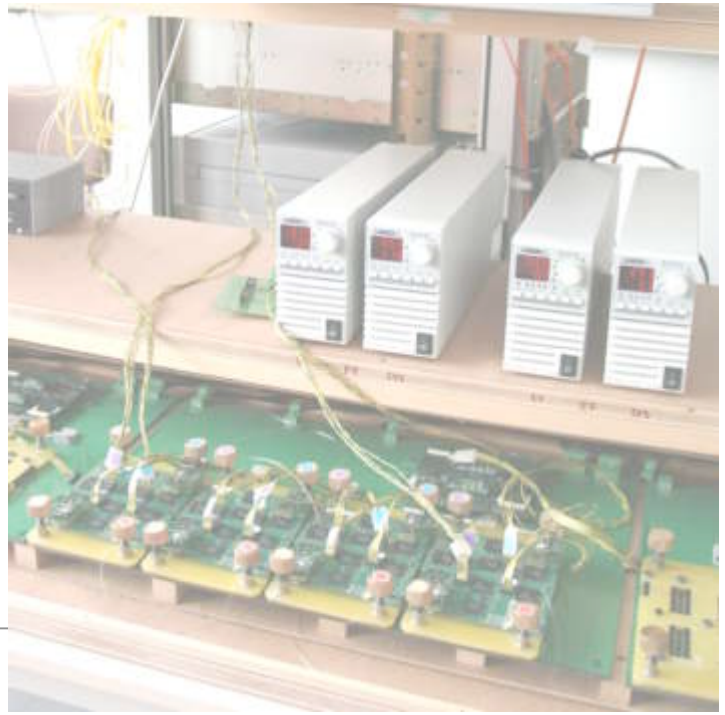
CMS ECAL Front-End boards: the XFEST project





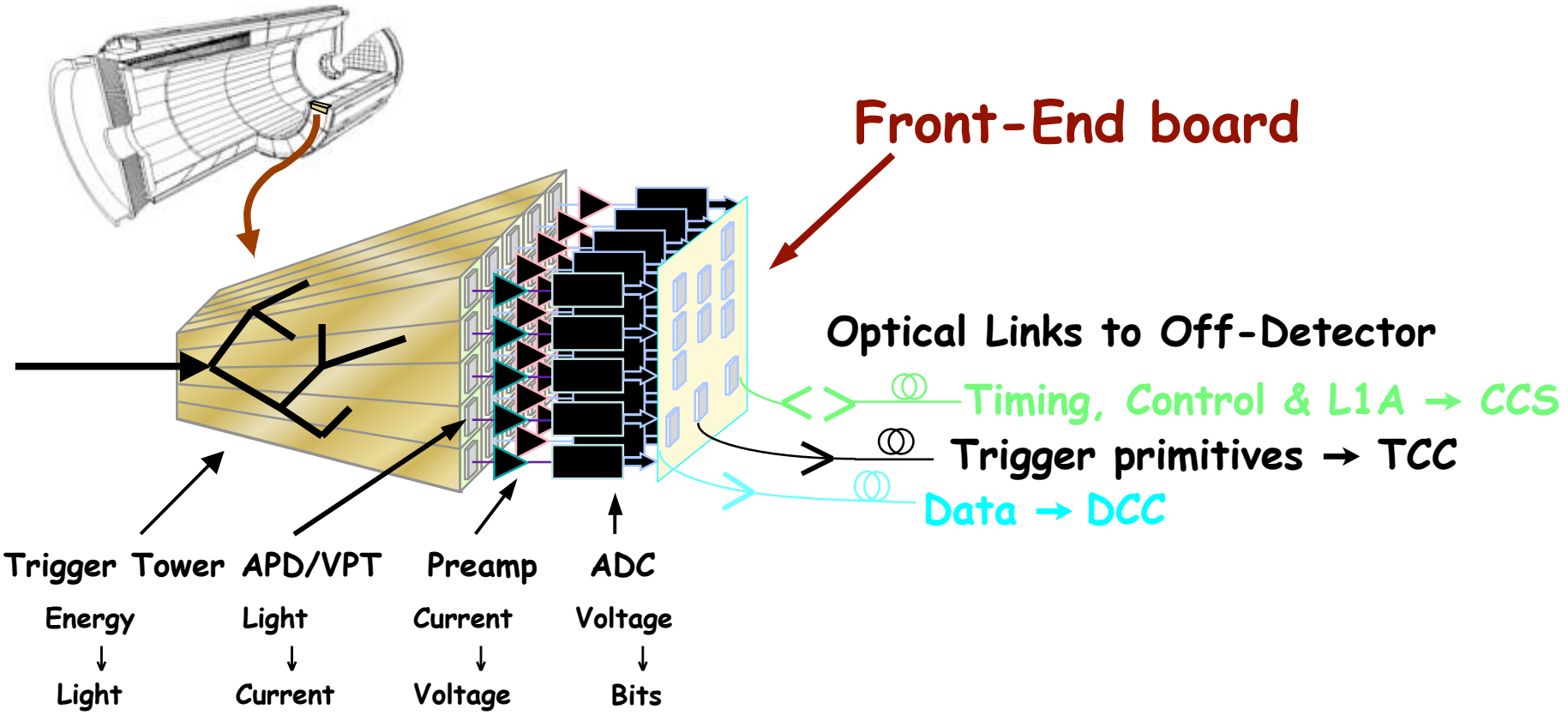
Caroline Collard
(LLR, Ecole Polytechnique)

Roadmap of the talk

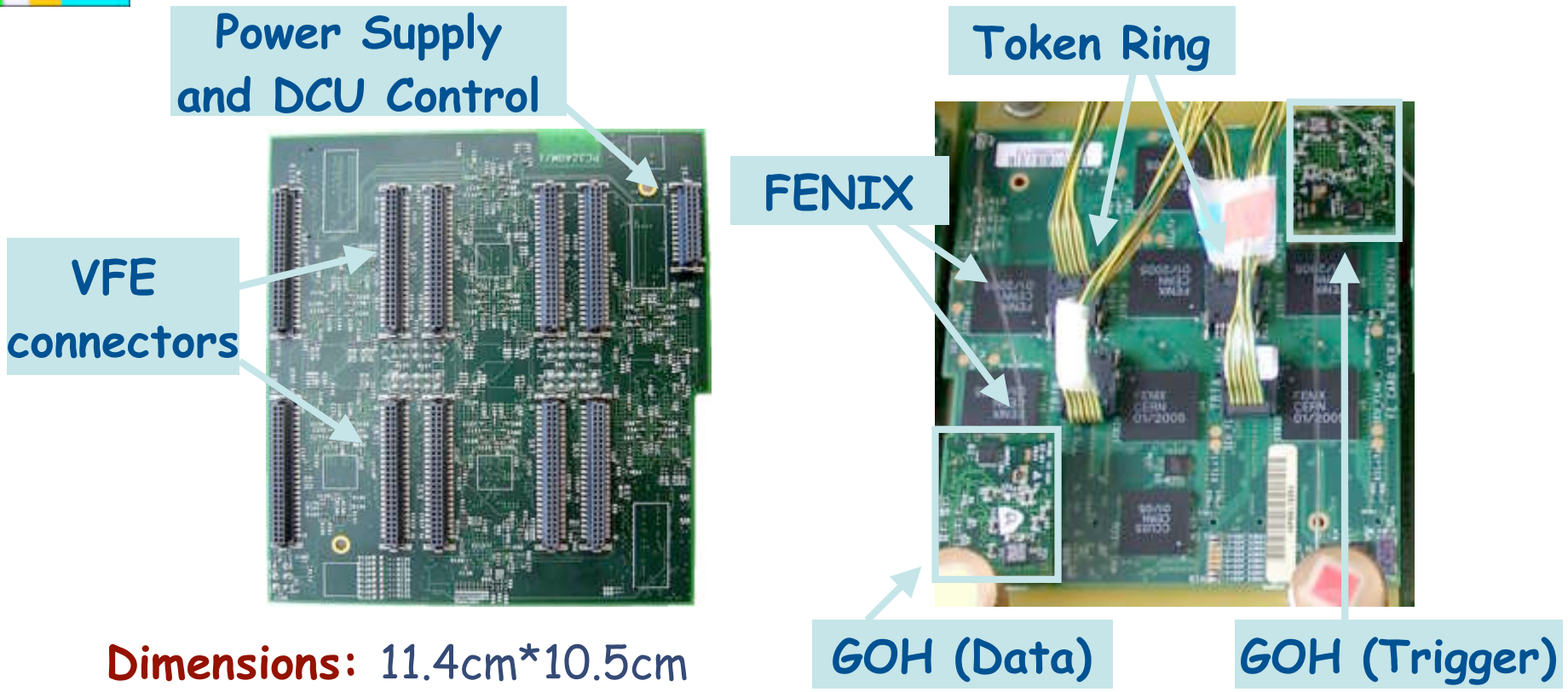
- Introduction
- The Front-End boards
  - Description of the board
  - Test of the boards
- The XFEST project
  - The pattern generator
  - The XFEST motherboard
  - The comparator
  - The "xfestd" daemon
  - Description of the testing procedure and results
- Conclusions

Introduction

CMS On-Detector Electronics



The Front-End board (FE)



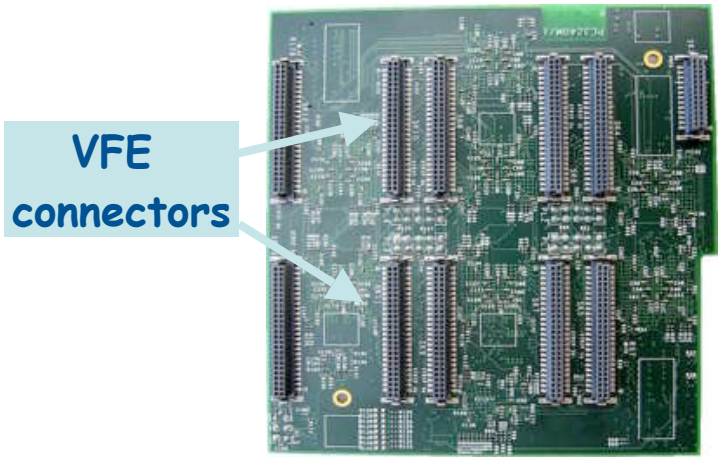
Dimensions: 11.4cm*10.5cm

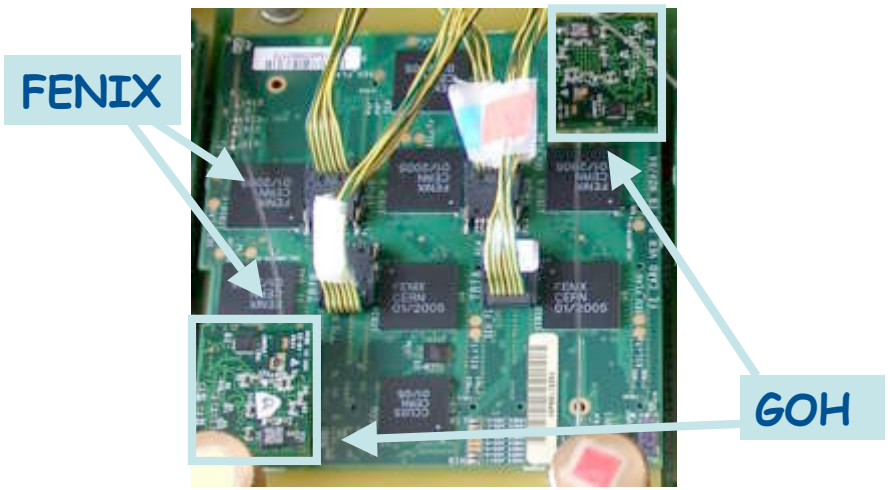
Power Supply: 2.5 V

Access to the board:

via Token Ring to the CCU and then via I^2C interface to internal registers (CCU, DCU, FENIX, GOH)

Functions of the FE board





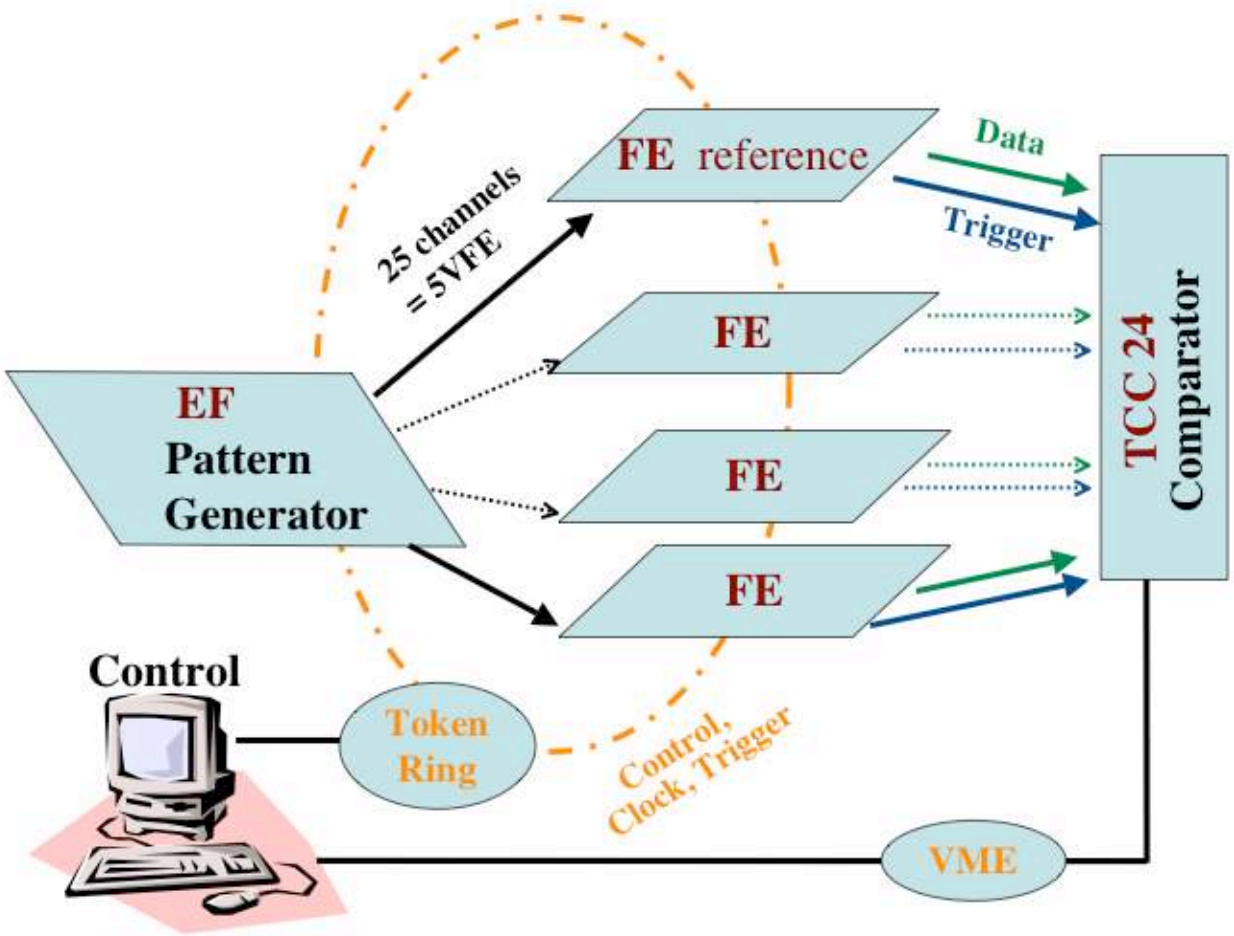
- **Reception** of the signals from 5 VFE boards
- **Storage** in FENIX chips, of the data during the Level 1 trigger latency (3.2 μs)
- **Computation** of the trigger primitive in FENIX chips
- **Sending** at 40 MHz of the trigger primitives to the TCC (via GOH chips with CIMT protocol)
- **Structuring and sending** of the data (via GOH with 8b/10b protocol) to the DCC board when it receives a Level-1 trigger accept signal

Production and tests of the FE

- **Production**
  - 1 batch (80 boards) by ELFAB & the rest by HITACHI
  - # Barrel=2800 (Jan-Aug 05) & EndCaps=596+spare (Spring 06)
- **Tests**
  - Functionality tests @ production site
    - 1 CMS Trigger Tower Set-up (5 VFE, 1 FE, power supply) with injection of test pulse in VFE
    - Tests: Register accesses, Ring A/Ring B, FE output control: noise measurement, signal quality, control of hit bits
  - Burn-in @ PSI
    - 80 boards power supplied, burned @ 60°C during 3 days
  - Extended test (XFEST) @ LLR

The XFEST project

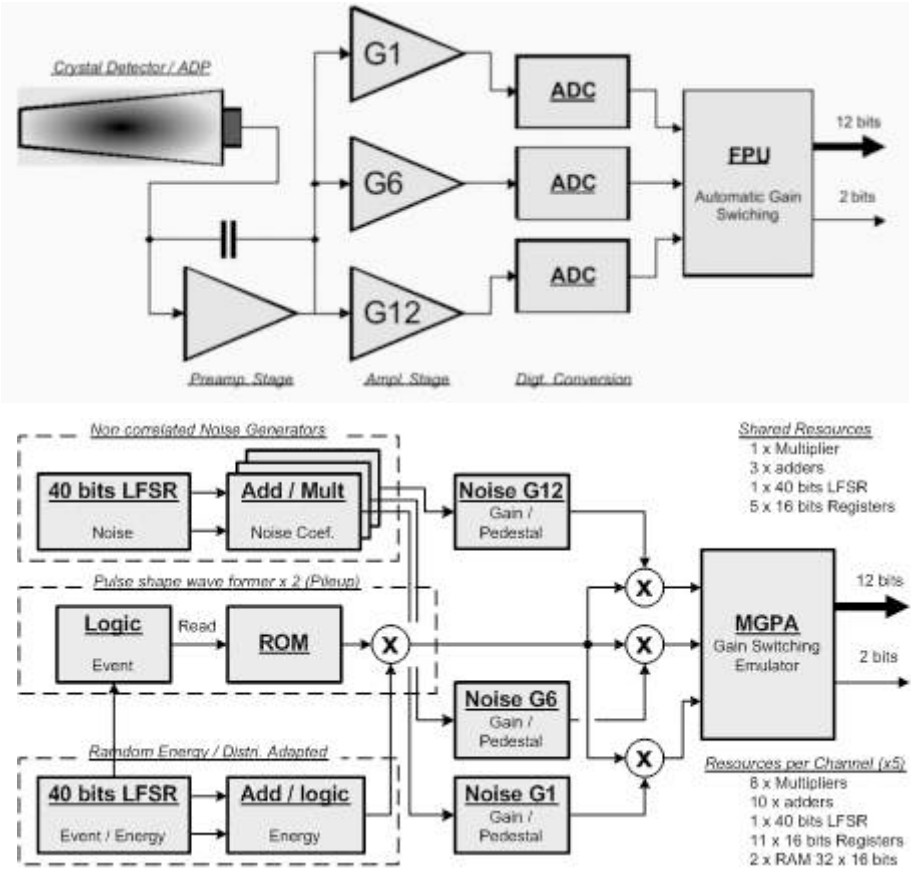
Test of 4 FE boards in parallel

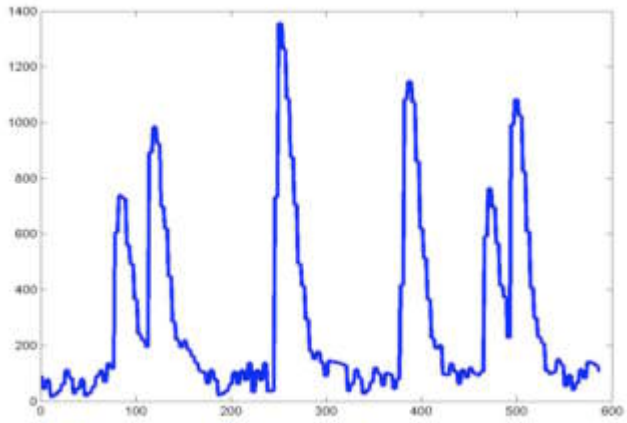


The pattern generation

EF board : FE prototype board working in "inverse mode"

➔ Reprogramming the FPGA to generate random patterns





Patterns on 25 channels of 14 bits @ 40 MHz

Pattern generation solution

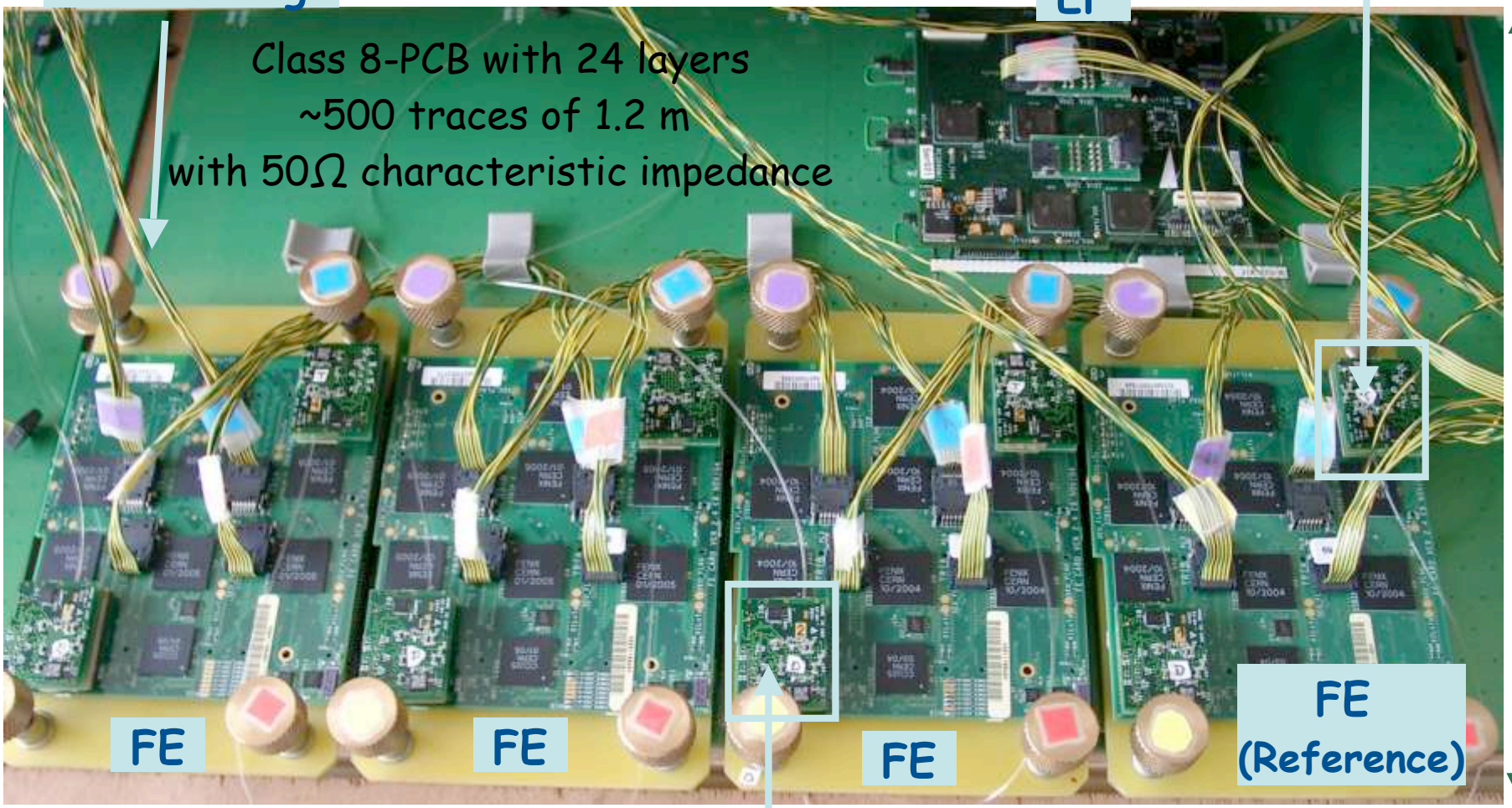
Fully digital model designed to emulate the VFE board digital input signals

- Use of a FE prototype board (EF) including 7 FPGA devices of one million logical gates
- Realistic and versatile data generation with:
  - I^2C slave interface for internal parameter access and setting
  - Specific signal amplitude model
  - Programmable range of signal amplitude
  - Digital waveform stored in ROM
  - Pileup capability
  - Non correlated noise for the 3 VFE gains
  - Fully programmable seed for noise sources
  - Fully programmable level for noise, pedestal and gain
  - MGPA dynamic gain switching emulator
  - Start/stop function under software control

See Th. Romanteau's poster for more details

The XFEST motherboard

Test of 4 FE boards in parallel



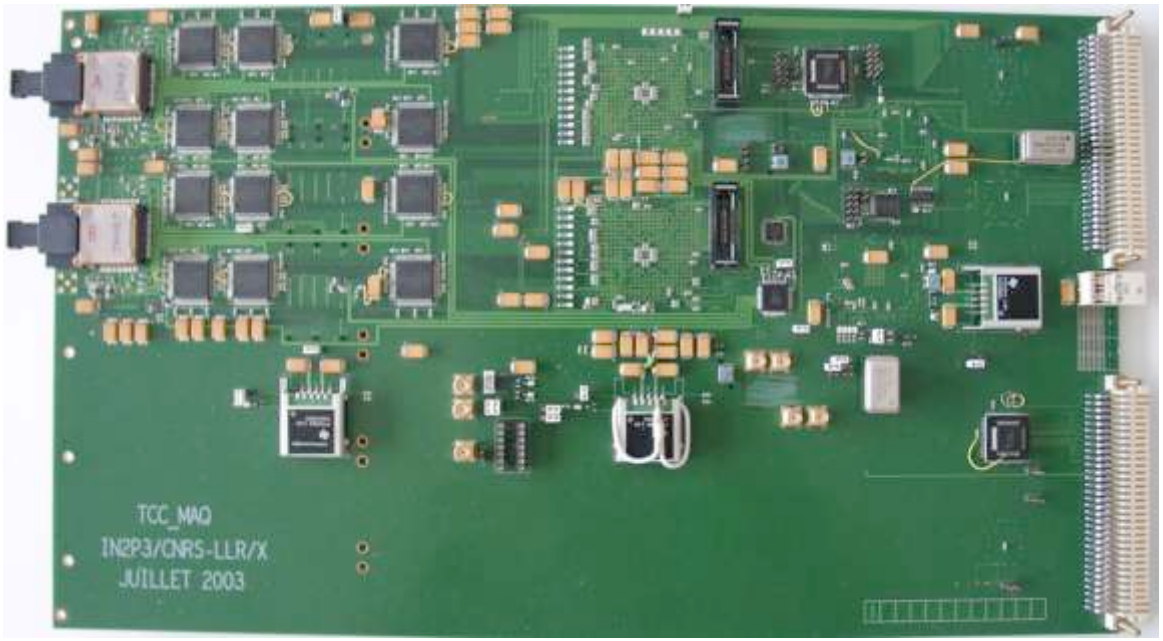
The output comparator

TCC24 (prototype of the TCC developed at LLR)

→ New VHDL code to use the TCC as a comparator for FE outputs (Trigger & Data)

2 optical outputs of the FE boards:

- **Trigger** (continuous flux)
- **Data** (when L1 Accept)



Comparison with respect to a reference:

- Count the error numbers
- VME interface, debug with ChipScope-Pro software

Trigger and Data Path Analysis

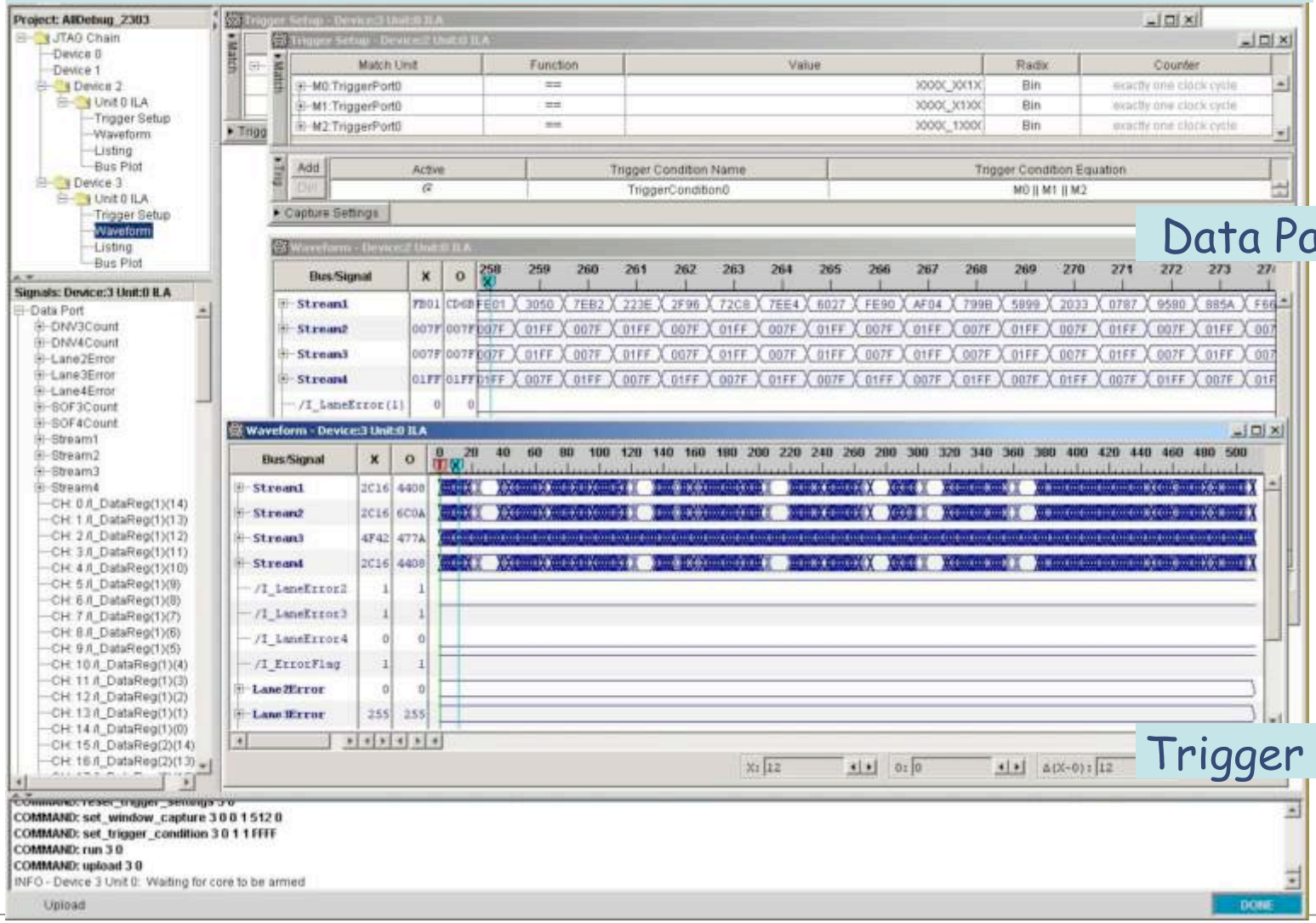
Comparison of Trigger and Data FE outputs

- Use of 1 FPGA per Path
- Dedicated solutions to aggregate and compare signals:
  - Work in an unique clock domain:
    Extracted clocks for each channel are written into self-addressing FIFO buffers. Then, all buffers can be read by the same local clock generated inside the TCC24.
  - Signal treatment:
    - Signal comparison in real time to avoid buffer controlling.
    - Real time state machine used for Data Path. Parameters inside Data stream are detected and extracted.
  - VME interface:
    Accessible registers: counts of comparison errors, transmission errors, serial link synchronization losses.
  - Internal debug solution based on "ChipScope-Pro" software

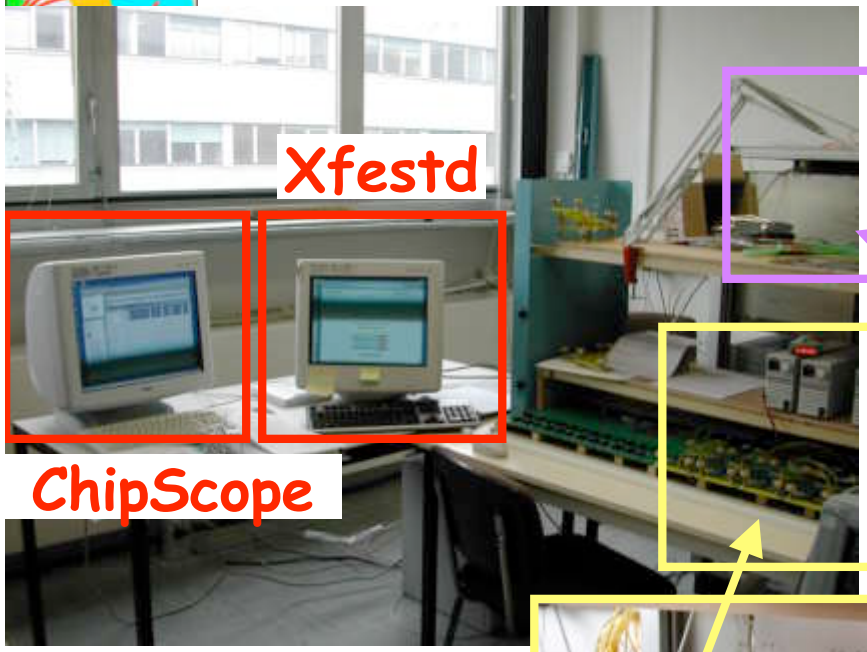
See Th. Romanteau's poster for more details

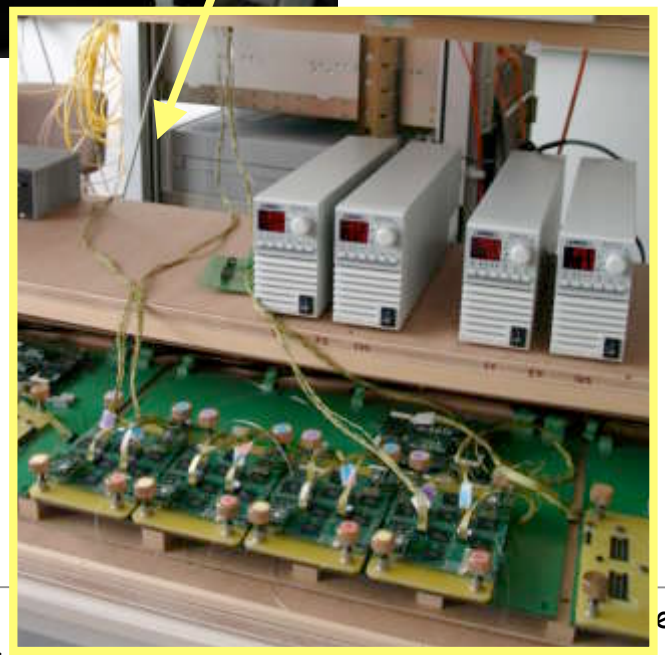
ChipScope-Pro

Control the number of errors in trigger and data mode



The whole Test Bench





SBS, TTCvi, TTCex, TCC24

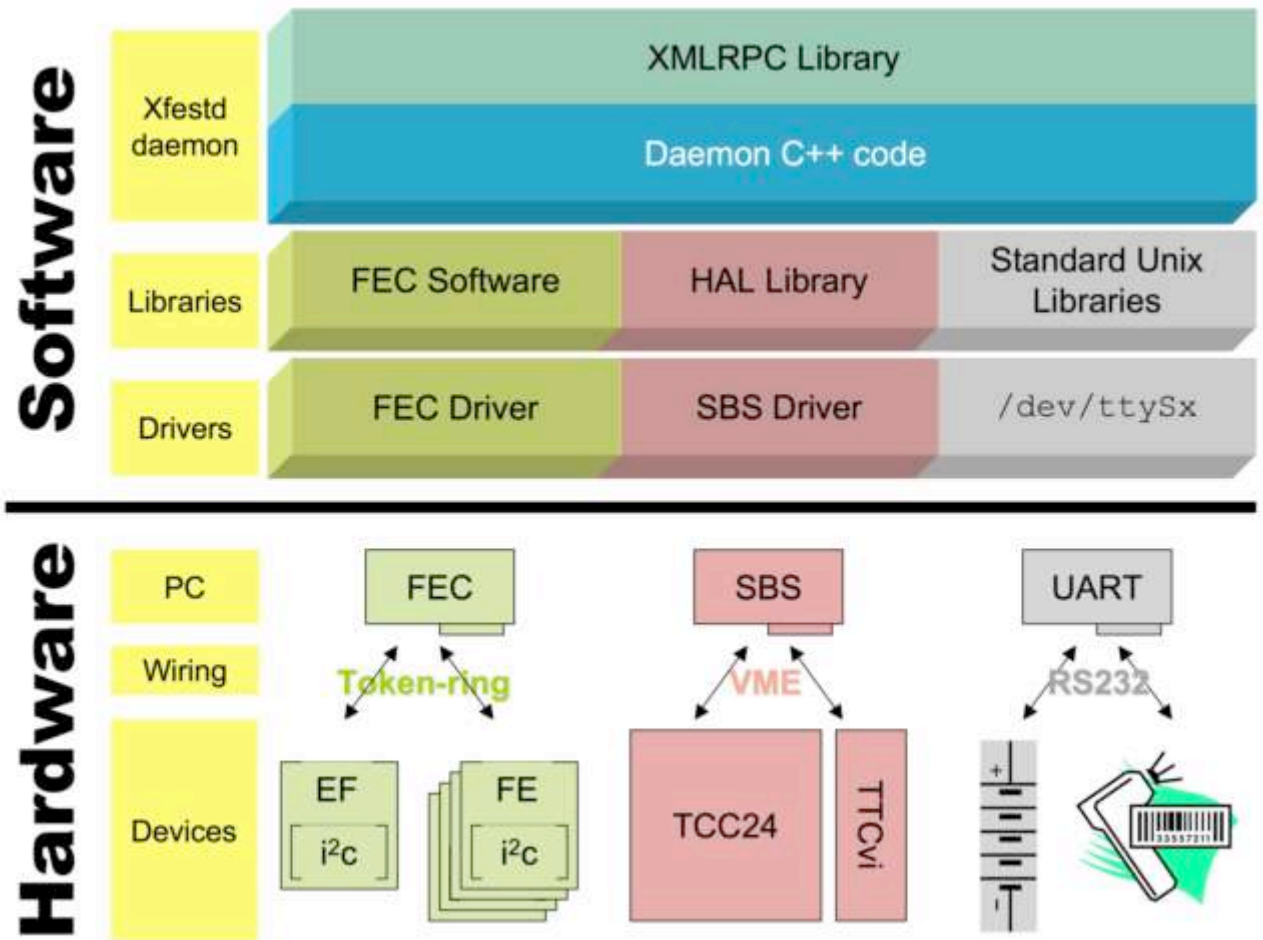
LHC clock emulator

Xfestd Daemon

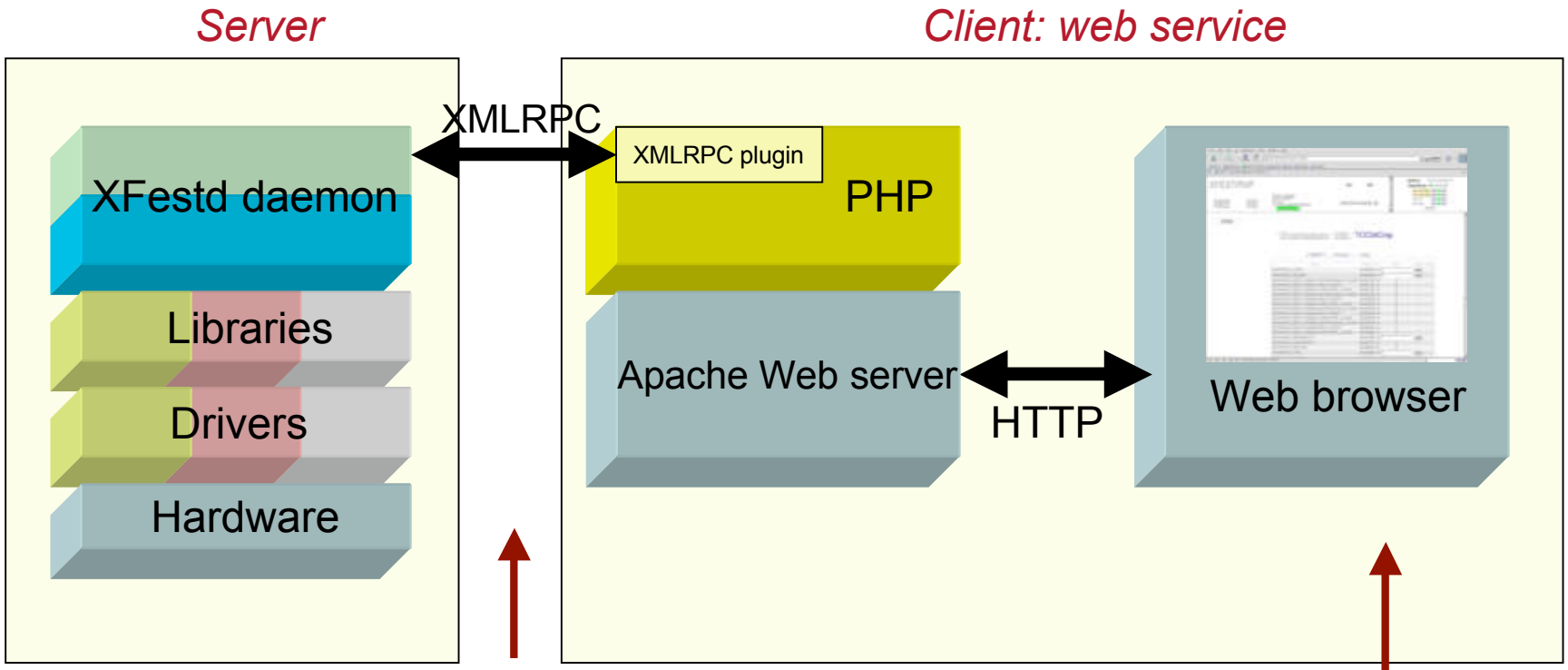
A daemon to control the test bench activity

Linux program written in C++

Based on CMS Hardware & Software



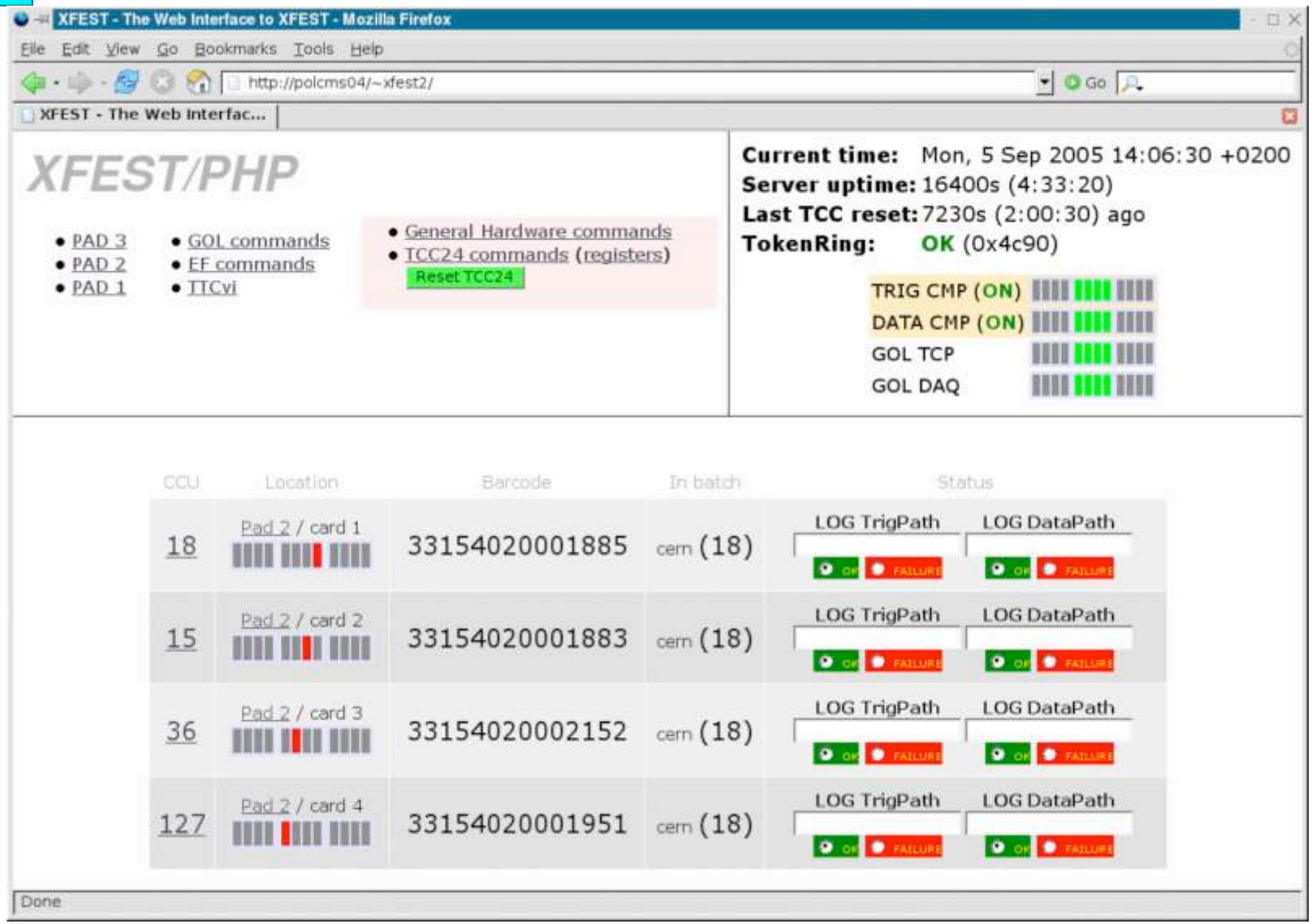
Client-Server approach



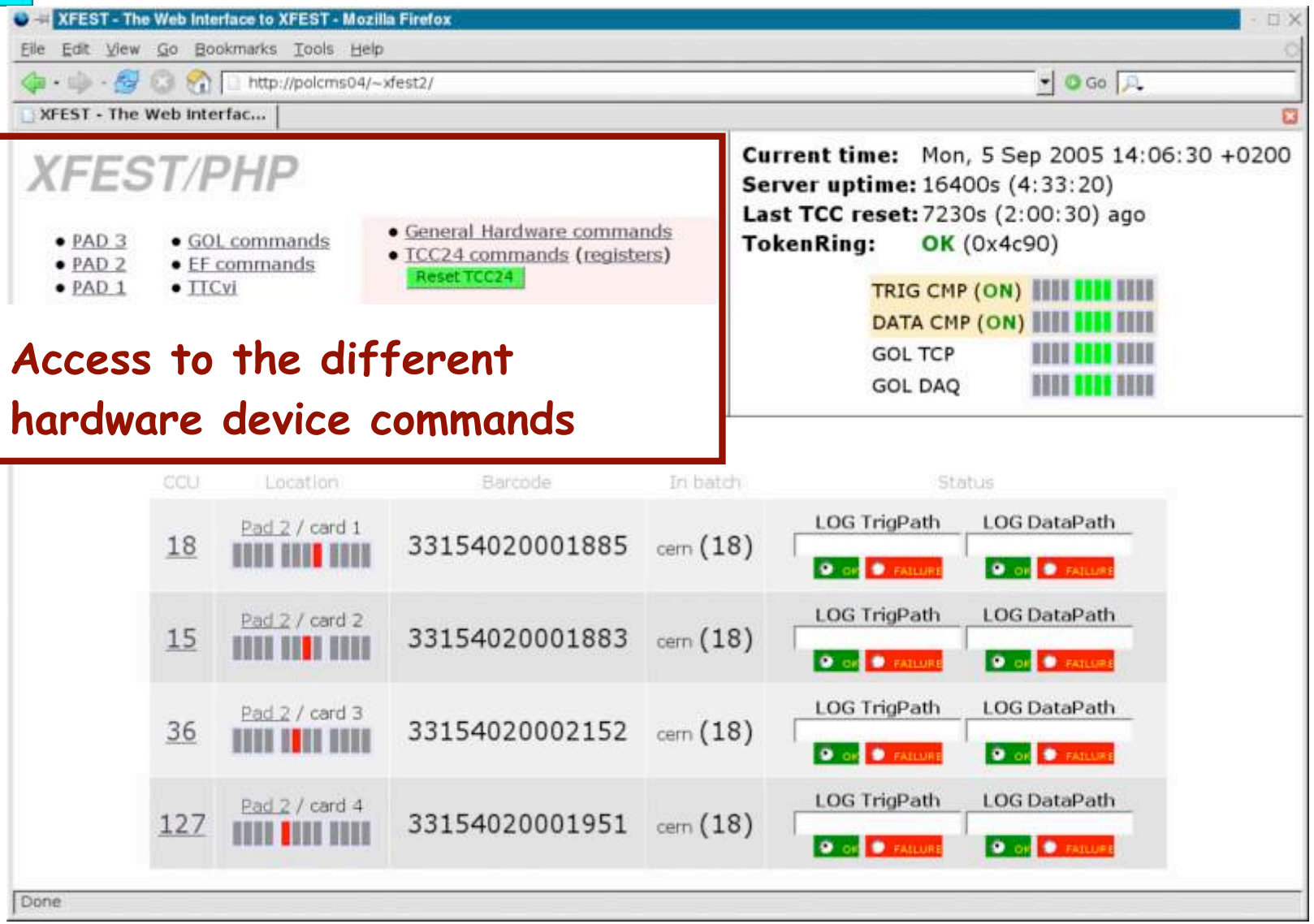
Internet (TCP/IP) connection based on the XML-RPC ("eXtended Markup Language - Remote Procedure Calls") protocol

The user only needs a classical web browser

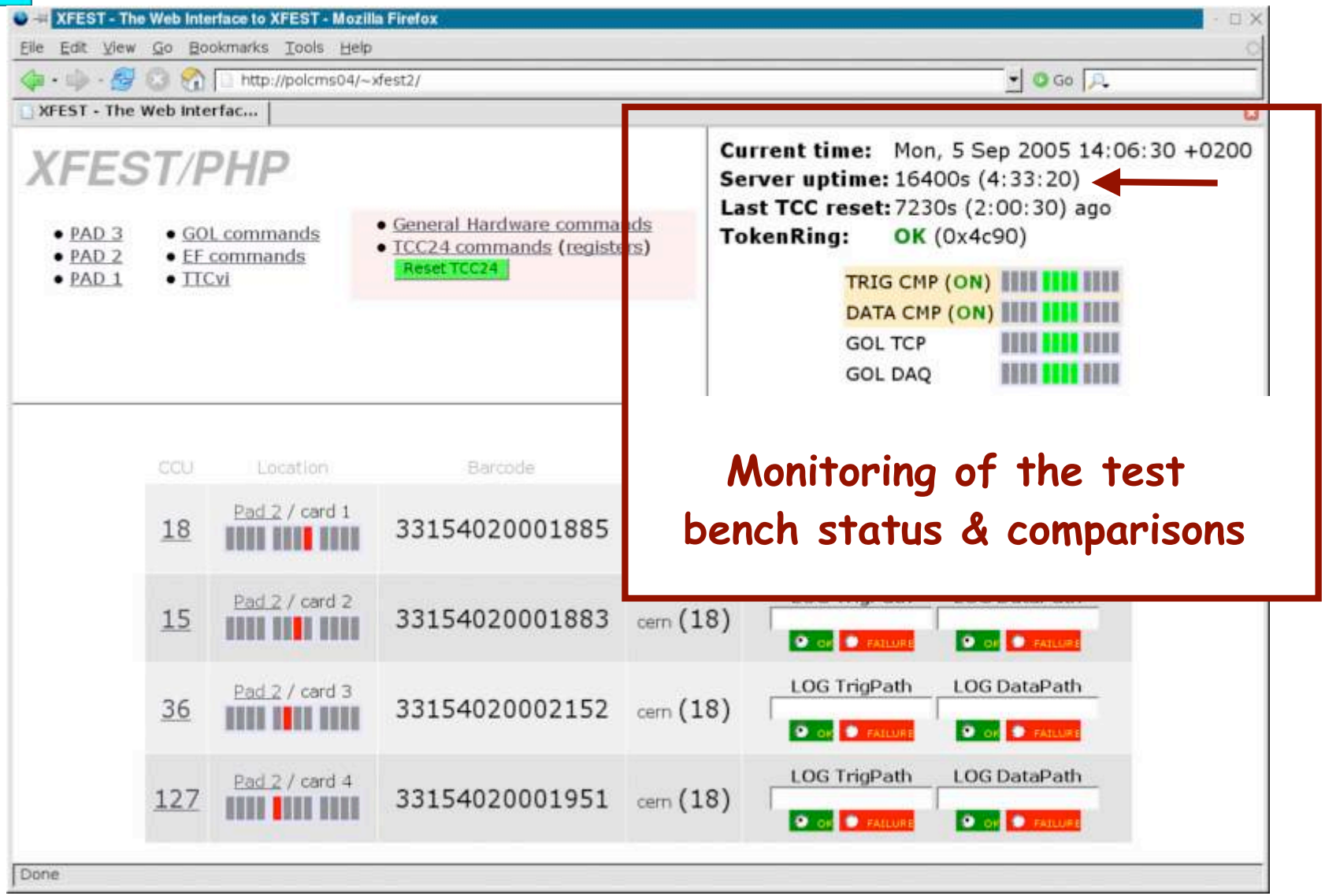
User Interface



User Interface

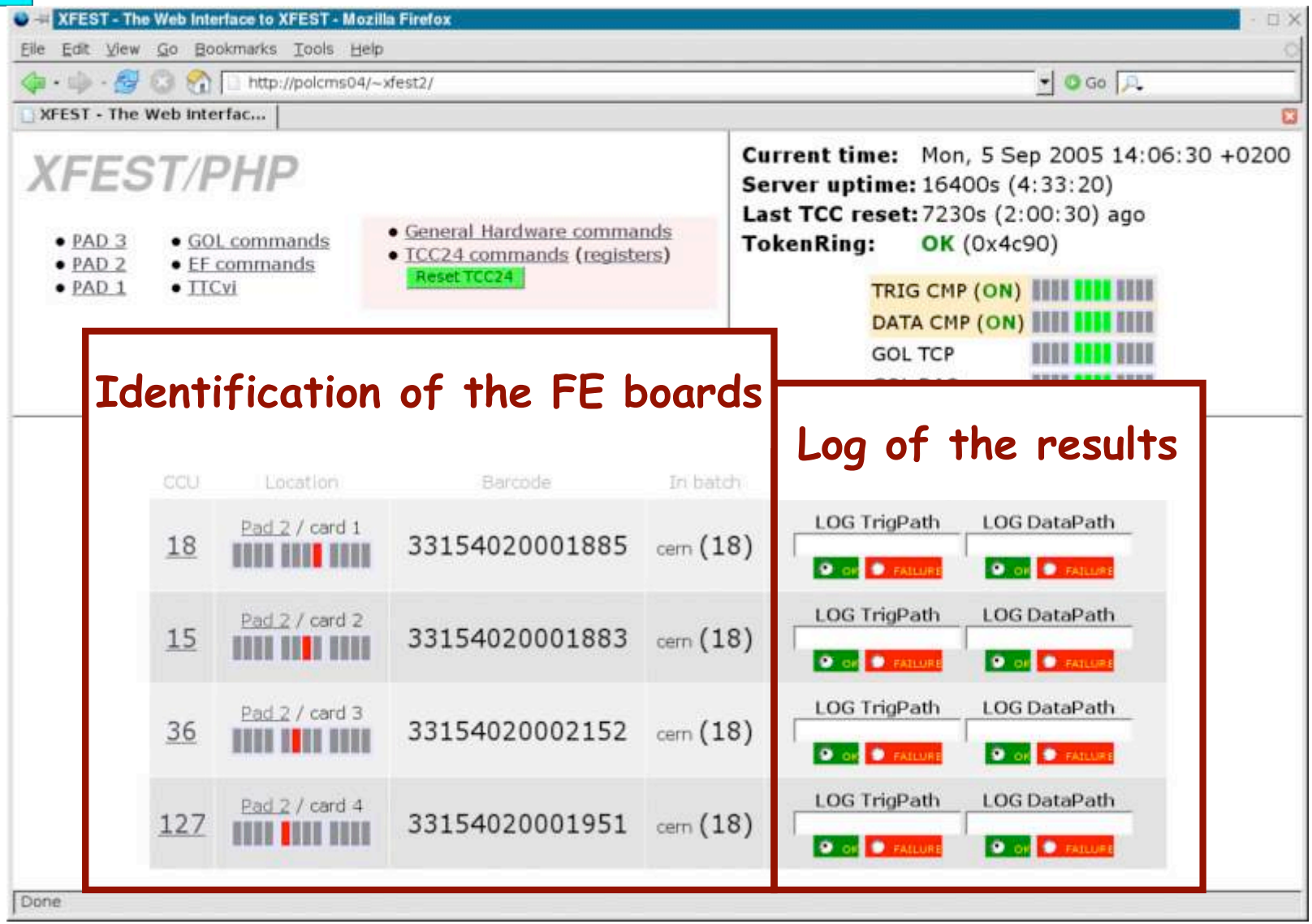


User Interface



Monitoring of the test bench status & comparisons

User Interface



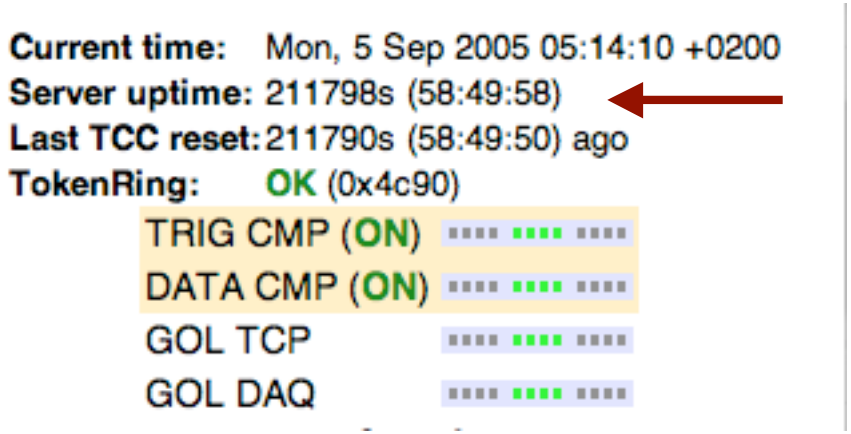
Remarks

- **Advantages of the Client-Server approach:**
  - Remotely control of the test bench → quickly react to test failure while not being urged to stay in the test bench room.
  - Development of the hardware control part in a language suited to this (C++), and the user interface in another language more suited to it (PHP) → speed in the software development.
- **Discussion about the choice of a web based interface:**
  - User quickly familiar to the test bench graphical interface (web browser) ☺
  - No spontaneous message display, like alarms (only reload of the web pages by itself or through user interaction) ☹
  - Change of web browsing habits: The "reload" button is not any more inoffensive! Pressing it could alter the general behavior of the test bench, possibly surprising the user !

Description of the testing procedure

- **Identify the FE** by their barcode and check the consistency of the CCU Id
- **Access to most registers** (for CCU, FENIX, GOH, …) of the FE boards via the I^2C interface (Default: ring A of the Token Ring)
- **Check the FE board ring B status**
- **Test the FE functionalities** by the comparisons of their outputs during approximately one hour (10^{13} patterns)

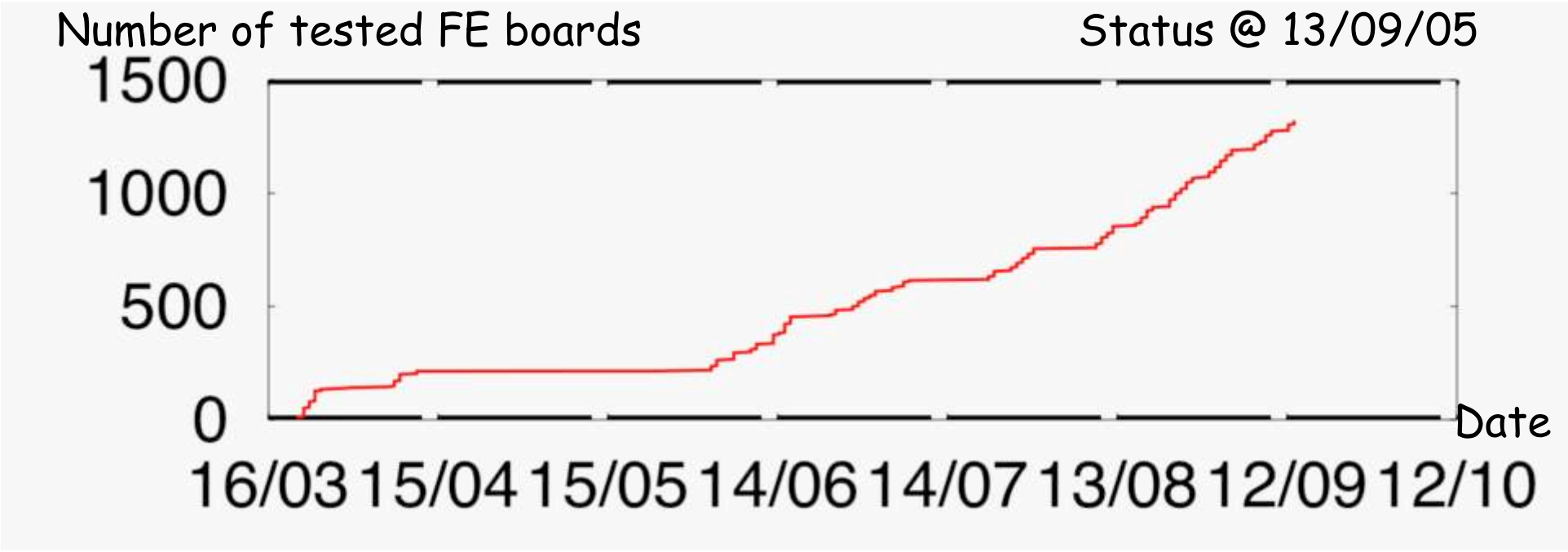
Most of the time the Data Path is running at 100 kHz trigger rate. A more extensive test (15 hours during nights and as much as 60 hours during the weekend periods) is also successfully carried.



Results of the tests

Test of 1322 boards

5 ELFAB & 20 HITACHI have encountered some problems related to CCU access, Trigger/Data Path defaults



Conclusions

- XFEST: Test bench designed to perform extended tests on the CMS ECAL FE boards

- Deep interactions between the software and hardware has been successfully achieved:
  - Use of CMS hardware components and software libraries.
  - Use of VHDL to produce FPGA firmware's
- Dynamical tests in realistic conditions corresponding to working detector conditions.

- XFEST project fully operational @ LLR: already half of the Barrel production tested up to now, the rest by end of 2005
- Outlook: EndCap FE Production validation (integration by Summer 2006)

Thanks

The XFEST team: Caroline Collard, Nicolas Regnault, Thierry Romanteau, Alain Debraine, David Decotigny, Philippe Busson, Ludwik Dobrzynski and Akli Karar

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