CMS ECAL Front-End boards: the XFEST project

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Abstract

The Front-End (FE) boards are part of the On-detector electronics system of the CMS electromagnetic calorimeter (ECAL). Their digital functionalities and properties are tested by a dedicated test bench located at Laboratoire Leprince-Ringuet, prior to the board integration in the CMS detector at CERN. XFEST, acronym for eXtended Front-End System Test, is designed to perform tests that can last several hours, on up to 12 FE boards in parallel. The system is designed to deliver 80 tested boards per week. This contribution presents the XFEST set-up and the results of the measurements on FE boards.

I. INTRODUCTION

The Large Hadron Collider (LHC) will enter in operation in 2007. This proton-proton collider will provide energy of 14 TeV in the centre of mass and a high luminosity of 10^{34} cm^{-2}s^{-1} with a bunch-crossing rate of 40 MHz. The Compact Muon Solenoid (CMS) [1] is a general-purpose detector in construction, which will be placed at one collision point of the LHC. The electromagnetic calorimeter of CMS (ECAL) [2] is a high-resolution calorimeter made of 75 848 lead tungstate (PbWO$_4$) crystals arranged in a Barrel (61 200 crystals) and two End-Caps (7 324 crystals each). It is optimized for the discovery of the Higgs boson in its decay in two photons.

The scintillation light from the crystals is captured by a photodetector, amplified and digitized in the Very Front-End boards (VFE). The signal enters then in the Front-End boards (FE), made with radiation resistant circuits, the last step of the "On-detector" electronics. In the FE boards, are partly computed the basic elements allowing the identification of electromagnetic showers by the Level-1 calorimeter trigger, called trigger primitives [3]. A second phase of the trigger primitive evaluation is realized by a dedicated VME 9U board called Trigger Concentrator Board (TCC) which belongs to the "Off-Detector" sub-systems [4] located outside the CMS cavern.

The FE boards are connected to the "Off-Detector" electronics by serial optical links working at 800 Mb/s over 90 m, with the CIMT protocol [5] to the TCC boards [4] and with the 8b/10b protocol to the Data Concentrator Board

(DCC) [4]. A total of 3 132 Front-End boards are necessary to manage the whole calorimeter. The industrial production of FE boards started in 2005. Such a production requires rigorous testing procedures especially for boards located inside the detector where no maintenance is possible.

This paper is organized as follows. In section 2, the Front-End board is presented in more details. Section 3 is dedicated to the XFEST project, describing the different steps.

II. THE FRONT-END BOARD

A. Description of the board

A FE board reads out 25 crystals by gathering the digital data (16 bits per channel) coming from 5 VFE boards. These 25 crystals correspond to a complete trigger tower in the Barrel. In the End-Caps, the 5x5 read-out crystals are called supercrystals and are divided into pseudostrips made up of 5 crystals with a variable shape. The End-Cap trigger tower is composed of several pseudo-strips and extends over several supercrystals and thus several Front-End boards.

The main functions of the Front-End board are:
- The reception of the signals from 5 VFE boards.
- The storage of the data during the Level 1 trigger latency (3.2 µs).
- The trigger primitive computation (evaluation of the transverse energy of a trigger tower and the fine grain veto bit in the Barrel and 5 partial sums of 5 crystals in the End-Caps).
- The sending at 40 MHz of the trigger primitives (as well as the bunch crossing assignment) to the TCC after conversion into a serial optical signal via GOL chips [6].
- The structuring and the sending of the data (via GOL) to the DCC board when it receives a Level-1 trigger accept signal, making the data available to the DAQ system.

The outputs of the FE board then correspond to 1 optical link to the DCC (Data path) and respectively 1 or 5 optical links to the TCC (Trigger path) in the Barrel or the End-Caps. While the data corresponding to the Data path are processed in a single dedicated radiation-hard asic called "Fenix", those of the Trigger path are processed by 6/5 Fenix chips respectively for the Barrel/EndCaps. The settings of the

internal registers of the Fenix as well as the control of the FE board are done via a Token Ring [7]. Reception and decoding of the control parameters is done in a rad-hard asic called "CCU" (Communication and Control Unit) [7].

B. Test of the boards

A first batch of FE boards has been produced by ELFAB [8]. The rest of the production is handled by HITACHI [9]. At the production site, a first test of functionality is applied to all boards. In the first production batches, CCU or Fenix problems (access to registers, bit loss, etc) have been identified on 8 to 10% of the boards. After the staving of all asics, the rate of deficient boards has decreased to 3%. The boards are sent by the manufacturer to the Paul Scherer Institute (PSI) [10], where a 3 days burn-in test at 60°C is performed to simulate an accelerated aging. The boards are then sent to the Laboratoire Leprince-Ringuet (LLR, Palaiseau, France) for additional long test. This paper describes the LLR test bench, which has to handle a minimum of 80 boards per week.

III.   XFEST: THE EXTENDED FRONT-END SYSTEM TEST

Between January and August 2005, 2 800 Front-End boards have been produced for the Barrel (2 536 for the detector and laser monitoring readout with some spare in addition). In 2006, the production of 596 boards will be launched for the 2 End-Caps. XFEST is a test bench designed to control the FE boards production after the burn-in phase.

Considering the very large number of possible input patterns (25x16 bits), it is not possible to cover the whole phase-space in a realistic time. Therefore, input patterns as close as what will be encountered in the experiment have been chosen. Besides, in order not to spend too much time per tested board, XFEST is designed to inject the same patterns to several FE boards on test. Therefore, the basic idea of XFEST is to inject realistic digital patterns into several FE boards in parallel and to compare their outputs to the ones of a FE board considered as a reference. Figure 1 displays a schematic view of XFEST for a set of four FE boards.
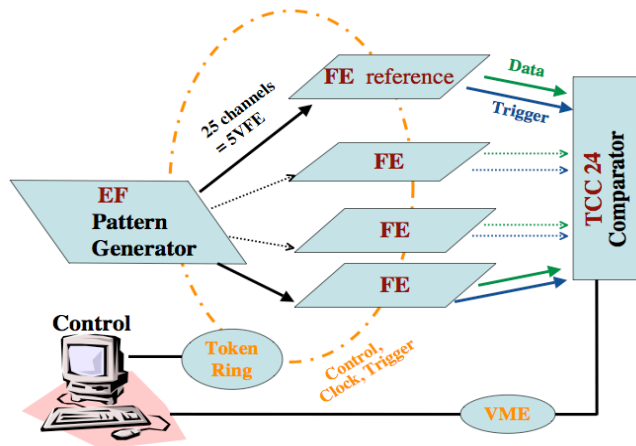

Figure 1:   Display of the XFEST test bench for a set of 4 FE boards

There are four main components: the pattern generator used to inject the signals to the FE boards, the motherboard for the distribution of the signals (input patterns, control, etc), the comparator and the daemon "xfestd" which controls the whole test bench.

A. The pattern Generator

The pattern generator used to inject the signals to the FE boards is an old FE board prototype working in reverse mode (producing 25 outputs in place of inputs) and called "EF". Its FPGAs have been reprogrammed to satisfy the XFEST requirements. A schematic view of the crystal channel signal modeling is shown in Figure 2 where the top view gives the detector signal flow and the bottom view the model used for XFEST.
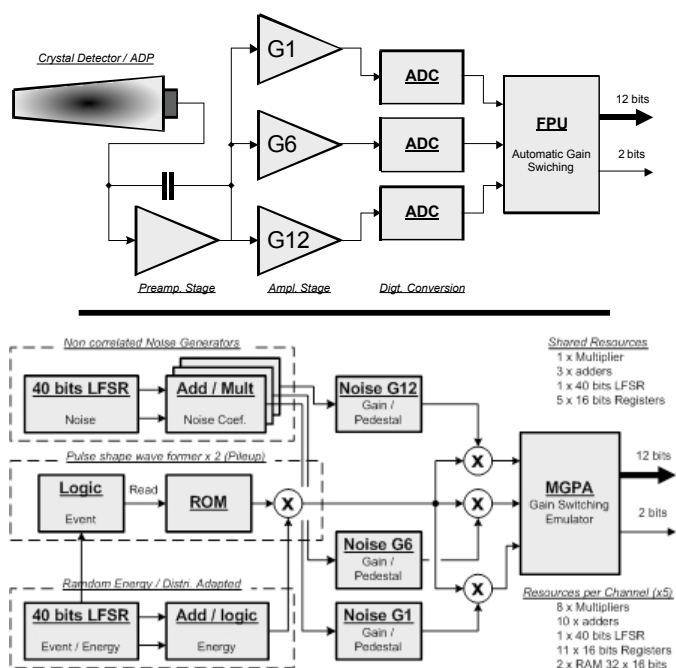

Figure 2:   A schematic view of the VFE detector signal flow (top view) and the model used for XFEST (bottom view)

The EF generates pulse signals with variable amplitude (a sequence of 40 bits LSFR is used) and (pseudo-) random noise. The multi-gain-pre-amplifier of the channels is emulated with its 3 gains and respective pedestals. The shape of the signal is loaded in a ROM. Pile-up events can be simulated by superimposing 2 signals. Details are given in [11].

B. The XFEST Motherboards

The main purpose of the XFEST motherboard is to distribute the same signals (25 channels) from the EF to several FE boards. It also supplies the power. The principle of XFEST relies on the comparison of the FE outputs assuming the same inputs. Therefore, the motherboard has been designed with a particular care to warrant the quality of the signal along the signal bus of the FE boards: long traces with characteristic impedance, large room between traces to avoid cross talk, etc.

A prototype has been first realized connecting the EF

board to 2 FE boards. The motherboard used for the production tests connects 4 FE boards as it is represented on Figure 3. The size of this final version is 58 cm x 30 cm. The PCB has 24 layers and belongs to class 8. There are about 500 traces of 1.2 m with 50 Ω characteristic impedance.

As in the current implementation of the "On-Detector" electronics, a Token Ring bus is used to link the different boards (FE or EF) to provide the clock and the trigger information. A double ring system allows to by-pass a deficient board, conserving a closed ring bus. Each board can also be controlled via an I^2C interface [12].
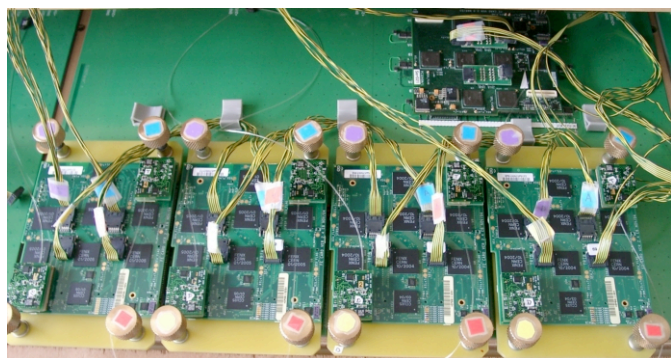

Figure 3: The XFEST motherboard equipped with the pattern generator board (EF) on the right top and four FE boards in the bottom line

C. The comparator

In the CMS experiment, the data and trigger outputs from the Front-End boards will be sent respectively to the DCC and TCC boards. In XFEST, the two optical outputs of the FE boards are sent to the TCC24 board, which is a prototype of the TCC developed at LLR (Figure 4). It requires that the GOL protocol for the Data path be switched from 8b/10b to CIMT.
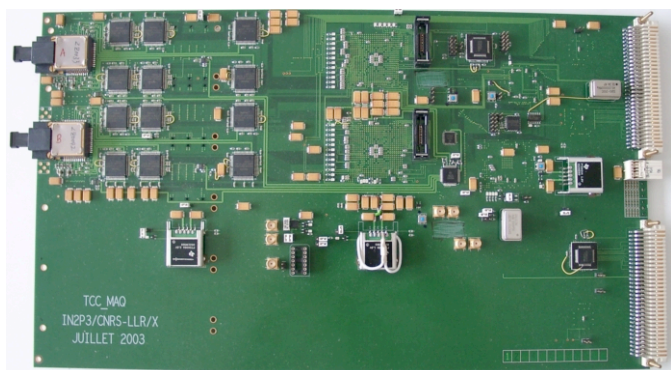

Figure 4: The TCC24 prototype

The TCC24 prototype, used as a comparator for the present project, can process 2x12 input channels at the same time. Any discrepancy at the bit level between one or several boards and the reference increments the error counters. Details about the comparator system are given in [11]. A detailed visual checking and debugging facility is based on Chipscope Pro [13] software facilities.

D. The control software and user interface

The activity of the test bench is controlled by a daemon, called "xfestd", using both the I^2C and the VME interfaces to access the hardware. This daemon runs on a Linux PC and provides the interface between the XFEST hardware devices and the user.

1) Access to the hardware and its supervision functions

As presented on Figure 5, the daemon handles:

- The access to the registers of the FE boards. The FE boards are accessed via a Token Ring bus using a "FEC" (Front End Control board) PCI board located in the PC. On each FE, the CCU serves as the interface to the local I^2C buses to access the registers of each functional unit (Laser driver, PLL, etc).

- The access to the registers of the pattern-generator board ("EF"), in the same way as the FE boards, but with a different set of registers.

- The access to the registers of the VME boards: the comparator ("TCC24") and the trigger generator board ("TTCvi") [14]. The VME bus is accessed from the PC through a PCI to VME bridge board produced by the SBS manufacturer [15].

- The control of the test bench power supplies. A serial connection (RS232) is used to dial with them. This basically consists in powering and shutting them down.
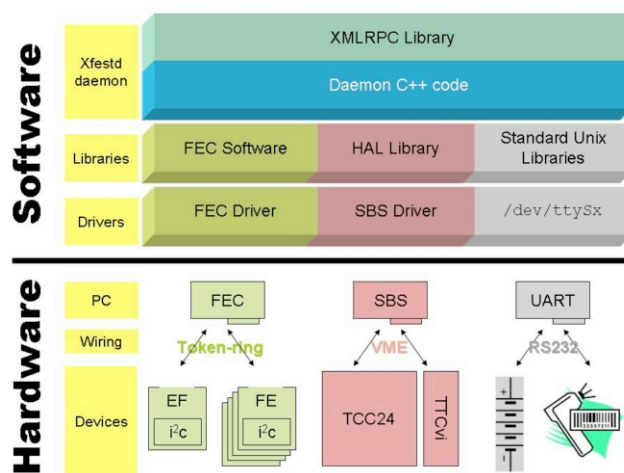

Figure 5: Interaction of xfestd with the hardware devices

The daemon maintains the mapping of the FE boards from the electronics identifier supplied at burn-in phase by PSI (CCU addresses), to their physical location on the test bench, and to their identifier in the CERN database. It uses a barcode reader for that purpose, since each FE board is uniquely identified by its barcode. The barcode reader is accessed by the daemon through a serial cable (RS232).

One of the main functions of the xfestd daemon is to log the most important test bench events: the start of a new test session, the normal or abnormal status of important devices (*e.g.* the status of the FEC or the SBS board), the state of the comparison, etc. For that purpose, the daemon automatically and regularly reads a set of hardware registers on the TCC24 board.

2) Interface with the user

The daemon is not completely autonomous. The user has to send commands such as "begin a new test", "stop the test", "read the barcode", etc. The user interface is dissociated from the hardware monitoring and control, in a client-server approach. The link between the hardware interface (the *server*) and the user interface (the *client*) is an Internet (TCP/IP) connection based on the XML-RPC ("eXtended Markup Language - Remote Procedure Calls") protocol. This protocol allows calling functions internal to the xfestd daemon from outside of the daemon itself. A schematic view of the software architecture is displayed on Figure 6.
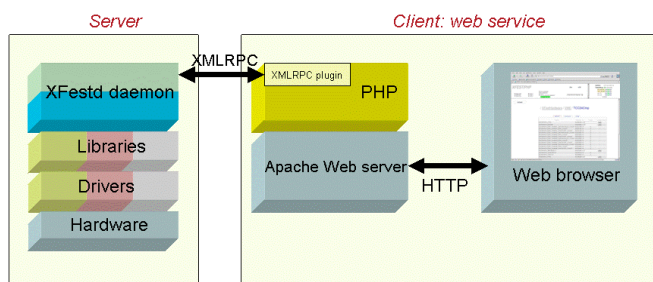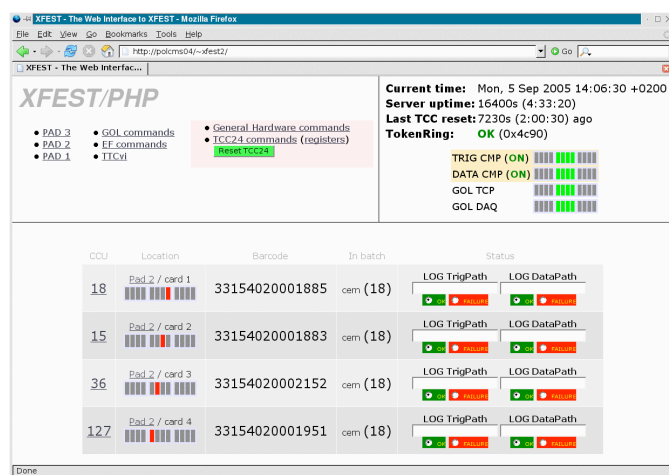

Figure 6: Software architecture

Figure 7: Home page of the web site user interface. The top left image shows the links to the pages of the hardware device commands. The top right one gives the current status of the test bench. Finally the bottom image presents the identification of the four FE boards and the place to provide the test results

The user interface takes the form of a "web service". A set of PHP scripts on a web server makes the interface between the daemon (XML-RPC) and the user interface (web pages written in HTML). The user only needs a classical web browser (Mozilla, Firefox, Safari, Internet Explorer, etc). He

navigates through the XFEST web pages with his web browser (see Figure 7 as example), which sends requests to the web server (plain HTTP protocol).

The web server scripts handle these HTTP requests and generate one or more orders to the xfestd daemon (XML-RPC), which responds afterwards to them (XML-RPC). The scripts process the XML-RPC response(s) from the xfestd daemon and present then the results as HTML pages returned to the user's web browser (HTTP).

3) Implementation choices

Both the hardware and user interfaces try to reuse a maximum of software tools and code (web browser, XML-RPC library, etc).

The daemon is a Linux program written in C++. It depends on several software layers to operate:

- The Linux serial device interface to access the power supplies and the barcode reader.
- The "FEC Software" [16] developed at IRES and CERN, which consists in a Linux driver responsible for controlling and accessing the FEC board, and in a function library made up of a set of C++ classes to ease the interaction with the Linux driver.
- The "HAL" (Hardware Access Library) [17] developed at CERN, which consists in a set of C++ classes to access the VME bus through the SBS PCI to VME Bridge. For that, the HAL depends on the Linux driver for the SBS board.

The HAL library allows the description of the VME board registers in a very simple way through a bare XML file. This prevents from having to write tons of error-prone repetitive C++ code. During the development of the TCC24 board, this had the advantage, by an update of the XML file, to simplify the synchronization of the register list accessible through the daemon with the hardware implementation.

4) Pros and cons

The client-server approach has a bunch of immediate advantages. First, it allows to remotely control or observe the (in) correct behavior of the test bench. One can quickly react to test failure while not being urged to stay in the test bench room. Second, this type of architecture allowed to develop the hardware control part in a language suited to this (C++), and the user interface in another language more suited to it (PHP). The addition of new functionalities and the modification of the "aesthetic" aspect of the interface have been easy to do. The software development has thus been sped up.

The choice of a web based interface has been a sensible choice for a test bench. Most importantly, the user is quickly familiar to the test bench graphical interface because he is already familiar with the tool to manipulate it (a web browser). However, for real hardware supervision and monitoring, a web based interface has some drawbacks. First of all, it can not display spontaneous messages, such as alarms: it can only reload the web pages by itself or through user interaction. And also, some web browsing habits have to

be somehow changed. For example, when a user presses the "reload" button on a "classic" web page, it is generally inoffensive; on the contrary, on hardware-impacting pages this simple action could alter the general behavior of the test bench, possibly surprising the user.

E. *Description of the testing procedure and results*

Four FE boards plugged on the XFEST motherboard are tested at the same time, one of them being used as the reference. The testing procedure is the following:

- All FE are identified by their barcode and connected to a database to check the consistency of the CCU chip Id.
- The accesses to most of the registers (for CCU and Fenix chips) of the FE boards are tested via the I^2C interface. By default, the ring A of the Token Ring is used.
- The status of the ring B of the FE boards is then validated.
- The functionalities of the FE boards are currently verified by the comparisons of their outputs during approximately one hour (10^{13} patterns). Most of the time the Data path is running at 100 kHz trigger rate. A more extensive test (15 hours during nights and as much as 60 hours during the weekend periods) is also successfully carried.

At LLR, since the beginning of the tests in March 2005, 1290 boards have been tested: 90 from ELFAB and 1200 from HITACHI. Five out of the 90 from ELFAB and 17 out of the 1200 from Hitachi have encountered some problems related to the CCU access, Trigger and/or Data path comparisons. The deficient boards have been sent to CERN for deeper investigations.

IV. CONCLUSIONS

The XFEST project is fully operational at LLR. The hardware and the software architecture have been developed at LLR using CMS hardware components and software libraries. XFEST is designed to test dynamically the FE boards in the more realistic conditions corresponding to working detector conditions. About half of the Barrel production has been up to now tested. The Barrel boards will be validated by the end of 2005. The test bench will then be updated in order to be ready for the End-Cap FE boards validation, which will be delivered for the integration by Summer 2006.

V. REFERENCES

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[5] For CIMT and 8b/10b protocols: http://hmuller.home.cern.ch/hmuller/high_speed_links.htm

[6] For GOL and GOH: http://cms-tk-opto.web.cern.ch/cms-tk-opto/ecal/components/goh.html

[7] For Token Ring and CCU: http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/2002/Tracker/A48.pdf

[8] For ELFAB AG: http://www.elfab.ch/

[9] For Hitachi: http://www.hitachi-computerproducts.fr/

[10] For PSI: http://www.psi.ch/

[11] T. Romanteau et al, "A real-time electronics emulator with realistic data generation for reception tests of the CMS ECAL Front End boards", contribution paper to the current conference.

[12] I^2C stands for Inter-IC bus from PHILIPS. It is a serial control bus that provides in a system the communication link between integrated circuits.

[13] ChipScope-Pro, real time debug and verification tool from XILINX: http://www.xilinx.com/ise/optional_prod/cspro.htm

[14] For TTCvi: http://ttc.web.cern.ch/TTC/

[15] For SBS: http://www.sbs.com/

[16] For the FEC software: http://proj-fec-ccs.web.cern.ch/proj-FEC-CCS/

[17] For HAL: http://cmsdoc.cern.ch/~cschwick/software/documentation/HAL/index.html