Design and Performance of the CMS Pixel Detector Barrel Modules

C. Hörmann

University of Zürich, Physics Institute, Winterthurerstr. 190, 8057 Zürich, Switzerland

Paul Scherrer Institute, 5232 Villigen PSI, Switzerland
christoph.hoermann@psi.ch

Abstract

The basic building block of the barrel part of the CMS pixel detector is a module. A module has a sandwich structure and its sensitive area has a size of 66.6mm * 18.6mm. The performance of prototype modules has been evaluated in detail in the laboratory. Furthermore there was a high rate beam test at the Paul Scherrer Institut (PSI) to validate the performance of the modules exposed to a particle rate comparable to Large Hadron Collider (LHC) conditions.

The structure of the modules and laboratory measurements including results are described. More over first results from the beam test are presented.

I. Introduction

The CMS pixel detector is the innermost tracking device of the CMS experiment at the LHC at CERN. It consists of three barrel layers and two sets of two endcap disks (see figure 1).

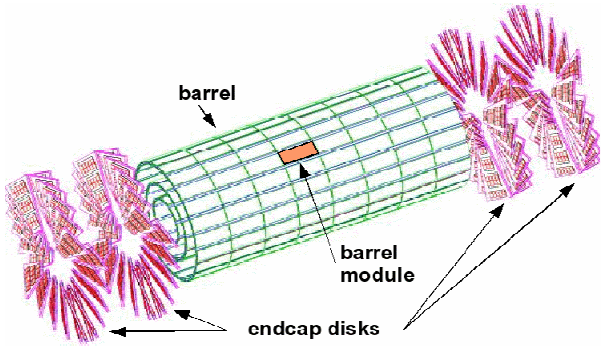

Figure 1: The CMS pixel detector consists of three barrel layers and two sets of two endcap disks.

The radii of the barrel layers are 4.4cm, 7.3cm and 10.2cm. The layers are planked with 128, 224 respectively 320 full modules in addition to 32 half modules per layer. In total the pixel detector will consist of 672 full modules and 96 half modules. The entire area covered by the three layers will be ~0.90m^2 (see table 1).

Table 1: CMS pixel detector barrel

Radius [cm]	# Modules	# Chips	# Pixels [*10^6]	**Area [m^2]**
4.4	128 + 32 ½	2304	9.6	**0.18**
7.2	224 + 32 ½	3840	16	**0.30**
10.2	320 + 32 ½	5376	22.4	**0.42**
Total	**672 + 96 ½**	**11520**	**48**	**0.90**

At LHC, bunch crossings will occur in 25ns intervals (40MHz) with several hundred charged particles produced inside the acceptance of the pixel detector at each crossing. The expected track density is 40MHz/cm^2 for the 4cm layer at high luminosity of 10^{34}cm^{-2}sec^{-1}. The first level trigger rate will be up to 100kHz. Because of the high track density, the innermost layer is expected to be exposed to a fluence of 3 * 10^{14}n$_{eq}$/cm^2 in one year. For more information see [1].

In section two the architecture of the pixel barrel modules is presented. The main components of the modules are described in subsection A. In subsection B the overall features of a barrel module are given.

The third section explains the intra module crosstalk investigations, performed in the laboratory. In subsection A the column drain mechanism is described. The approach of the measurement is shown in subsection B. The results of the intra module crosstalk investigations are presented in subsection C.

Section four describes a high rate pion beam test setup (subsection A) and shows some of the first results (subsection B).

II. CMS Pixel Detector Barrel Module

The structure of the pixel barrel module is shown in figure 2. The main components are the Kapton cable, the power cable, the High Density Interconnect (HDI), the sensor, the Read Out Chips (ROC) and the base stripes.

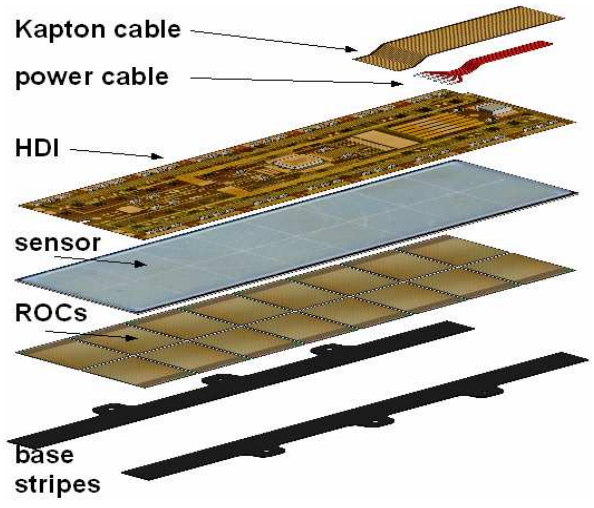

Figure 2: Pixel Barrel Module: Kapton cable, power cable, High Density Interconnect, sensor, Read Out Chips, base stripes

A. Components of the barrel module

1) Kapton cable:

The main purpose of the Kapton cable is to transmit the control signals from the endring print to the module. Furthermore it brings the analog information from the module to the endring print. Most of the signals are transmitted differentially by the Kapton cable which has 21 traces. To suppress crosstalk a solid metal layer is placed on the backside of the cable. The signal cable is glued on the HDI and connected by wire bonds.

2) Power cable:

The power cable provides the module with the analog, digital and bias voltages. Additionally the corresponding ground potentials are transmitted. Therefore it consists of six copper coated aluminium wires which are laminated to a flat power cable. The power cable is soldered to the HDI.

3) High Density Interconnect:

The HDI is a low mass, flexible printed circuit board, which distributes the control signals and the power to the 16 ROCs. The HDI is realized in a three metal layer design with 6µm metal and 10µm Kapton for insulation. The top and the middle layer are used for routing of the signals. The third layer is used for power distribution. The power layer is designed as a grid structure to lower the coverage of the area with Copper. The HDI is fitted with passive components like capacitors for decoupling of the power for the ROCs. The Token Bit Manager chip (TBM) [2], which organizes the operation and the read out of a group of ROCs, is also mounted on the HDI. After assembling the components, the HDI is glued onto the backside of the sensor.

4) Sensor:

For the sensor of the pixel detector the 'n-in-n' concept has been chosen. Electron collection has the advantage that after irradiation induced type inversion, the highest electric field is located close to the collecting electrodes. This ensures operation of partly depleted sensors. In addition the double-sided processing of these devices allows the implementation of guard rings only on the p-side of the sensor, keeping all sensor edges at ground potential. Due to the superior performance after irradiation and the possibility to implement a bias grid for testing reasons, the moderated p-spray technique was chosen. To improve the post irradiation behavior, oxygen enriched silicon (DOFZ material) is used. The breakdown voltage exceeds safely the required value of 600V. The thickness of the sensor is 285µm±15µm. The sensor is segmented into pixels of the size 100µm * 150µm in order to match the pixel size of the ROC. The sensor performance remains acceptable until a particle fluence of 6 * $10^{14} n_{eq}/cm^2$, which corresponds to two years of operation at high luminosity for the innermost layer. A more detailed description of the sensors is beyond the scope of this paper, see however [3] and [4].

5) Read Out Chip:

The most important parts of the full module are the 16 ROCs PSI46 v2.1. The size of the ROC is ~10mm * 8mm.

A single ROC consists of three major parts of different functionalities: the sensitive pixel array, the periphery of the pixel array and a global part of the ROC.

The pixel array is organized in 26 Double Columns (DC) and 80 rows, which add up to 4160 Pixel Unit Cells (PUC) per ROC. The size of a PUC is 100µm * 150µm (rφ * z). Each pixel cell contains an analog part with pre-amplifier, shaper, sample-hold mechanism and a comparator with an adjustable threshold. The input of the pre-amplifier is bump-bonded to the sensor. In addition to the analog part there is a digital part with four trim bits for a fine adjustment of the global threshold and a calibrate mechanism to inject charge into the pre-amplifier. The total amount of transistors per PUC is 251.

The DC interface is between the pixel array and the global part of the ROC. It contains 32 data buffer cells and 12 time stamp buffer cells per DC. Furthermore the DC interface contains the column drain mechanism which copies the data from the pixel array to the periphery [5].

The global part of the ROC holds the control interface block, which organizes the communication to the ROC, the 27 programmable Digital-Analog-Converters (DAC) and six programmable power regulators. For connection the ROC has 35 wire bond pads.

The ROC needs two supply voltages (V_{dig}=2.5V and V_{ana}=1.5V). In total the ROC contains 1.3 million transistors. The ROC is processed in Deep-Sub-Micron (DSM) CMOS technology, which is also used by conventional chip industry. The DSM technology can be designed radiation tolerant. The smallest feature size is 0.25µm and the process provides five metal layers for routing and metal-insulator-metal-capacitors. Compared with the former used DMILL technology, DSM provides higher speed and lower power consumption (half supply voltage and half current). A more detailed description of the architecture of the ROC can be found in [6].

6) Base stripes:

In order to reduce the material budget the solid base plate was replaced by two single stripes of 250µm thick Silicon Nitride (Si_3N_4), which is CTE matched to Silicon. The base stripes are needed for mounting the module on the cooling structure.

B. Features of the Module

The overall dimensions of the module sensor are 66.6mm * 18.6mm and the dimensions of the base plate are 65mm * 26mm. One module has 66560 pixels. The weight of the module is ~2.2g without cables and ~3.5g including both cables. The power consumption of one module is ~2W, which corresponds to ~120mW per ROC or ~28µW per pixel.

III. Laboratory Measurements

The focus is on the intra module crosstalk measurement. This measurement is important, because it gives an answer to

the question how the threshold is shifted by continuous data taking and simultaneous read out operation on the module.

A. Intra Module crosstalk

1) Column Drain Architecture:

The goal of the column drain architecture is to store pixel hits in a columnwide data buffer. There is a suppression of hits performed, which are not confirmed by triggers. The outputs of the comparators in the PUCs (see section II.A.5) form a hard wired column *OR*. The appearance of the column *OR* signal in the DC periphery initiates two tasks: the value of a 40MHz gray code counter (WBC) is written to a time stamp buffer cell and the address and analog pulse height of the hit pixels are copied to the periphery and stored in a data buffer. An average of two clock cycles is needed to copy down the data of one hit pixel. The data are kept in the periphery for the level one trigger latency: the time stamps are compared to a second gray code counter (SBC), which runs parallel to the WBC with an offset corresponding to the level one trigger latency. If there is equality between a stored time stamp and the SBC value, the system checks, whether an external *trigger* signal is active. If not, the corresponding data buffer is cleared. Otherwise the DC is marked ready for being read out.

2) Intra Module Crosstalk Measurement:

For this measurement 15 ROCs of the module are programmed with a trigger latency of value *latency_1*. In these 15 ROCs a number of pixels are enabled and prepared to get a *calibrate* injection by the ROC internal mechanism. For the ROCs with *latency_1* no appropriate *trigger* signal is given, which means, that the data buffer is cleared after *latency_1*. The 16th ROC gets a longer *latency_2* and only one test-pixel is enabled, but this pixel does not get a *calibrate* signal. In contrast to the other ROCs, the test-pixel gets an appropriate *trigger* signal and the data are read out after the *token* signal has arrived. Because of the fact that this test-pixel gets no *calibrate* injection, the read out data are caused by crosstalk from the other activities on the module or by noise. To make this measurement more sensitive for crosstalk, a threshold scan for the single pixel was made. By varying the *trigger* position with time and performing at each position a threshold scan, the intra module crosstalk could be quantized at each stage of the column drain mechanism. The baseline for this investigation was taken with zero pixels enabled in the 15 ROCs.

3) Crosstalk by Setting Up the Column Drain Mechanism:

After the calibrate injection the column drain mechanism is started. The crosstalk caused by starting up of this mechanism is plotted in figure 3 versus the VIColor DAC values. This regulator limits the current for the double column periphery notification. The positive crosstalk caused by the setting up of the column drain mechanism increases the threshold for some cycles. It depends on the number of pixels enabled in the 15 ROCs. For a realistic scenario (six columns per ROC, each 3 pixels enabled), the crosstalk is less than ~20 electrons. For a unrealistic scenario (40 pixels/DC enabled in 15 ROCs), the crosstalk is ~2000 electrons.

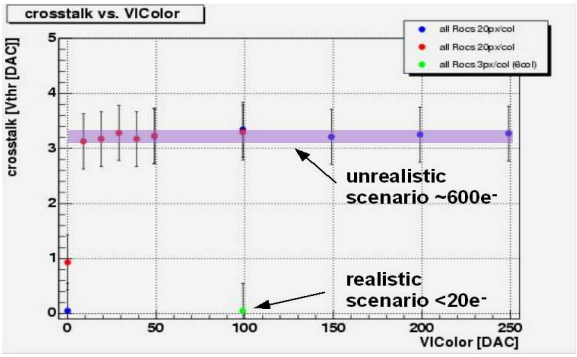

Figure 3: Crosstalk induced by setting up the column drain mechanism (200e-/Vthr [DAC]) vs. current limitation for column drain. For realistic scenario it is negligible (<20e-).

4) Column Drain induced threshold shift:

To investigate the negative pickup of the column drain mechanism, the single test-pixel with *latency_2* gets a *calibrate* injection too. By doing this, the method got sensitive for negative pickup (lowering the threshold). Without this *calibrate* signal, the pixel is already in the noise and it is not possible to see the effect of a lower threshold. The result of this measurement can be seen in figure 4.

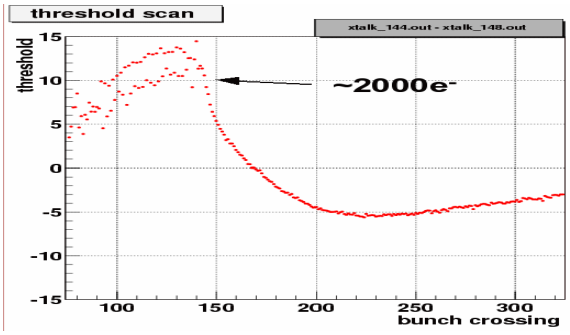

Figure 4: Crosstalk induced by the column drain mechanism. A quarter of the pixels of 15 ROCs is enabled. The crosstalk is 2000e- (200e-/Vthr [DAC]).

For this measurement 40 pixels per DC were enabled in the 15 ROCs. The length of the column drain is therefore ~80 cycles (calibrate signal is given at bunch crossing ~70). The crosstalk for this unrealistic scencario is ~2000 electrons. For a realistic scenario the crosstalk is less than ~200 electrons (see figure 5).

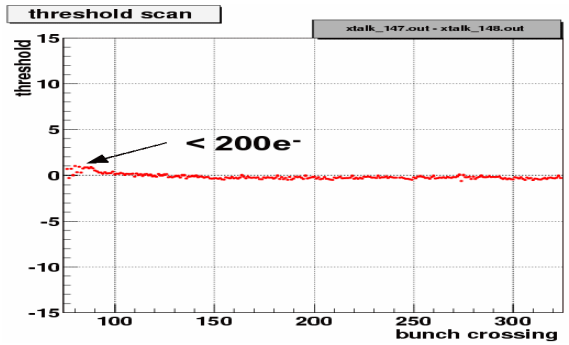

Figure 5: Crosstalk induced by the column drain mechanism. 6 columns with each 3 pixels are enabled. The Crosstalk for this scenario is ~200e- (200e-/Vthr [DAC]).

5) Read out induced threshold shift:

To investigate the threshold, shifted by a running read out operation, an appropriate trigger for the 15 ROCs with *latency_1* is given, too. After the confirmation of the hits by the *trigger* signal, the read out starts when the *token* arrives at the ROC. By moving the *calibrate* injection and the *trigger* for the test-pixel in time, the crosstalk during the read out can be investigated. In figure 6 the crosstalk is shown. No significant pickup during the read out and the data buffer reset at the end of the read out can be seen. In addition to the threshold shift the slope of the s-curve is also shown.

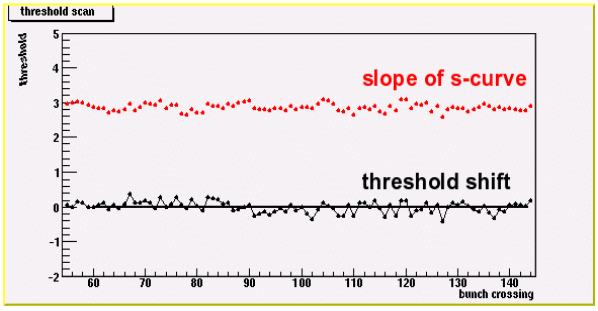

Figure 6: Crosstalk during the running read out of 15 ROCs. There is no significant pickup in the test-pixel of ROC 16 during read out and data buffer reset.

IV. High Rate Beam Test

The goal of the beam test was to operate a final pixel barrel module under LHC equivalent conditions before the mass production of the modules starts. LHC like conditions are a track density up to 40MHz/cm^2, which corresponds to the expected flux for the 4cm layer at high luminosity (10^{34}cm^{-2}sec^{-1}). The expected first level trigger rate will be up to 100kHz and the time between bunch crossings is 25ns.

A. Test Setup

The beam test was performed at the PSI. We used 300MeV/c pions (π+) with a variable intensity up to 100MHz/cm^2. The bunch structure was 50MHz and we operated the modules with a synchronized 40MHz clock. Triggers have been allowed only every 4th bunch crossing (CMS ≥ 3 cycles separation). In contradiction to the CMS experiment, there was no B field. Figure 7 shows the test setup.

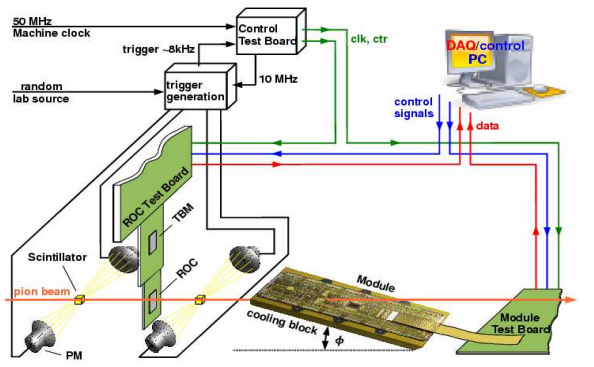

Figure 7: Beam test setup

We operated in parallel a single ROC and a module in the beam. To simulate various positions of the module in the barrel, the module was mounted on a cooling block, which could be tilted. To control the ROC and the module, a ROC test board and a module test board were used. A central control test board was used to synchronize the two other test boards. For trigger reasons we have built a beam telescope with two small scintillators (2*2*2mm^3). They have been read out with 4 Photo-Multiplayer-Tubes (PM) which were brought into coincidence. Because of the 50MHz bunch structure, every 5th bunch crossing coincides with every 4th clock cycle of the 40MHz clock and can be used for trigger confirmation and eventual read out. This has been achieved by synchronizing the PM coincidence output with a 10MHz clock deduced from the 50MHz machine clock. To generate a random trigger signal, there was an additional coincidence with the signal from a nuclear source. The trigger rate was adjustable from 1 – 25kHz. A trigger rate of 25kHz from a scintillator covering about 7 DC (width of 2mm), corresponds to a trigger rate of about 100kHz for the entire ROC.

B. First Test Results

Figure 8 shows a hitmap of the single ROC. It is a superposition of 30000 events, taken at an intensity of 1MHz/cm^2. The beam covered the entire ROC and module. For each triggered event, one should get a hit in an area, which is similar in size to the scintillator size. Due to random coincidences, there are also hits outside the trigger shadow. Moreover there are two empty pixels in the region of the scintillator shadow and one noisy pixel outside this region.

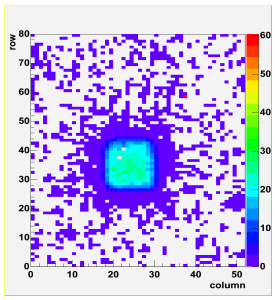

Figure 8: ROC hitmap: intensity 1MHz/cm^2; superposition of 30k events

In figure 9 the hitmap of the module for the same run is shown. The shadow of the scintillator trigger is blurred due to the beam divergence.

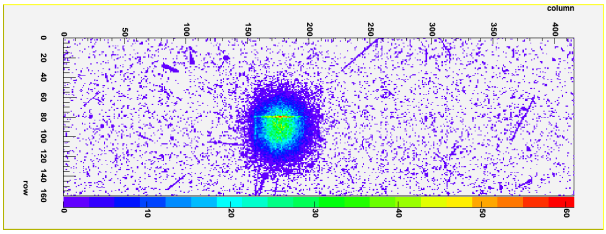

Figure 9: Module hitmap: intensity 1MHz/cm^2; superposition of 30k events

A module hitmap taken at an intensity of 47MHz/cm^2 and a trigger rate of 18kHz is shown in figure 10.

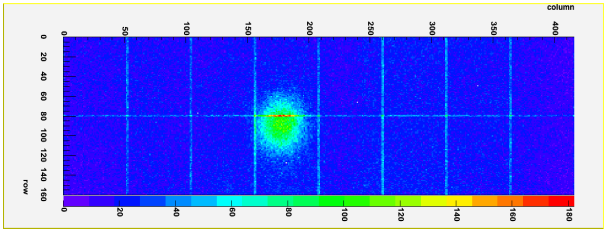

Figure 10: Module hitmap intensity 47MHz/cm^2; superposition of 30k events, trigger rate 18kHz

Compared to Figure 9 the number of random coincidences is higher due to the higher intensity. The higher rates at the edge pixels of the ROCs can be explained by the area of these pixels, which is double the size of regular pixels.

The analog pulse height distribution of single pixels is plotted in figure 11. The energy deposited by the pions corresponds to the energy of Minimal Ionising Particles (MIP). The pulse heights are corrected by using the internal calibration signals. Due to the fact, that the internal calibration mechanism saturates at large charges (~two MIPs), the correction for large pulse heights has large errors. The pulse height spectrum is cut for small pulses by the discriminator threshold. These thresholds vary from 3000e$^-$ to 6300e$^-$.

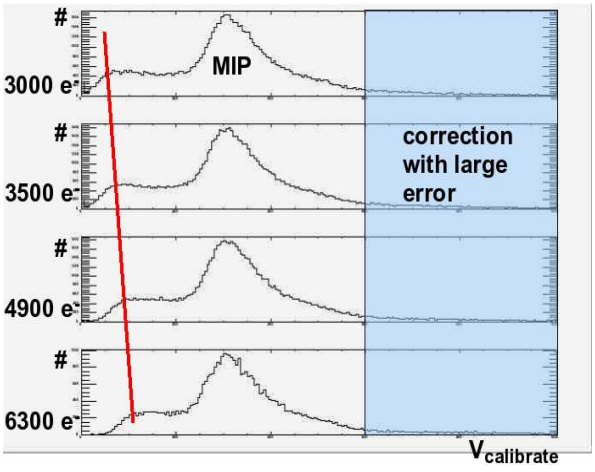

Figure 11: Corrected pulse height distribution of single pixels for different discriminator thresholds

The cluster charge for various tilting angles of the module is plotted in figure 12. The first peak in the plots is due to an artefact in the cluster recognition software. The cluster charge is proportional to the thickness of the sensor divided by the sine of the angle. The individual pixel charge decreases with the angle.

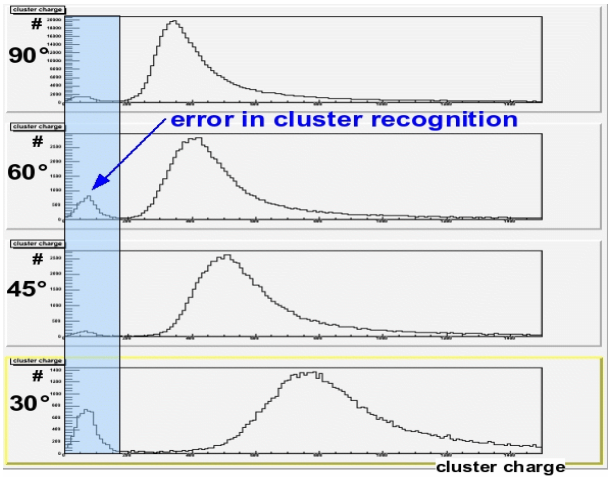

Figure 12: Cluster charge for various tilting angles

V. Conclusion and Outlook

A pixel barrel module of the final design for the CMS experiment has been tested in the lab and in a high rate LHC-like test beam. There is evidence for intra module crosstalk for continuous data taking and simultaneous read out operation but for realistic scenarios the crosstalk is negligible. During the read out no crosstalk has been seen. In the beam test the module was operated at a threshold of 3000 – 4000e$^-$. The cooperation of the token bit manager chip and the PSI46v2.1 ROCs worked without any problems. The analysis of the high rate data is still ongoing.

VI. References

[1] CMS Tracker Project, Technical Design Report, CERN/LHCC 98-6, chapter 2

[2] E. Bartz, “The 0.25µm Token Bit Manager for CMS pixel Read out“, talk given at this workshop.

[3] A. Dorokhov et al. Test of silicon sensors for the CMS pixel detector. Nucl. Instrum. Methods, A 530:71-76, 2004.

[4] T. Rohe, “Fluence Dependence of Charge Collection of irradiated Pixel Sensors”, arXiv: physics/0411214

[5] H. C. Kästli, “Design and Performance of the CMS Pixel Read Out Chip”, in Proc. 8th workshop on electronics for LHC experiments, page 125, CERN-LHCC-2002-34.

[6] M. Barbero, “Design and Test of the CMS Pixel Read Out Chip”, Nucl. Instrum. Meth. A 517 (2004) 349-359