SPD Very Front End Electronics

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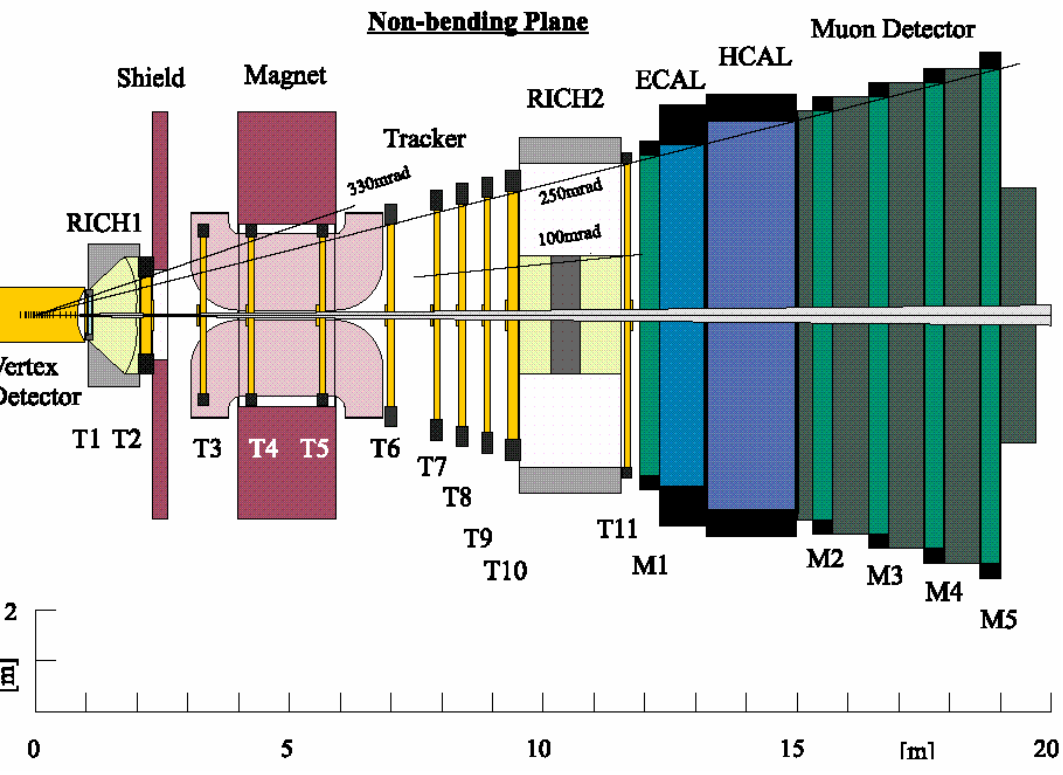
System



LHCb Calorimeter is composed by four subdetectors:

- SPD,
- PreShower,
- Hadronic Calorimeter and
- Electromagnetic Calorimeter.

Scintillator Pad Detector (SPD) Introduction(I)

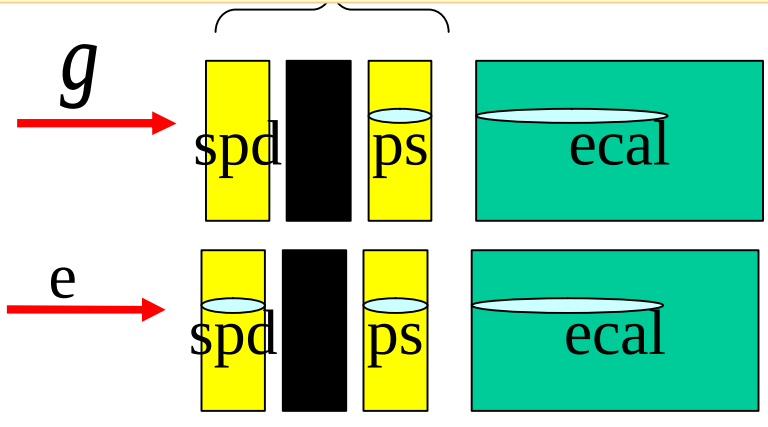
The SPD is designed to distinguish electrons and photons for the LHCb first level trigger. Process:

This detector is a plastic scintillator layer, divided in about 6000 cells of different size in order to obtain better granularity near the beam.

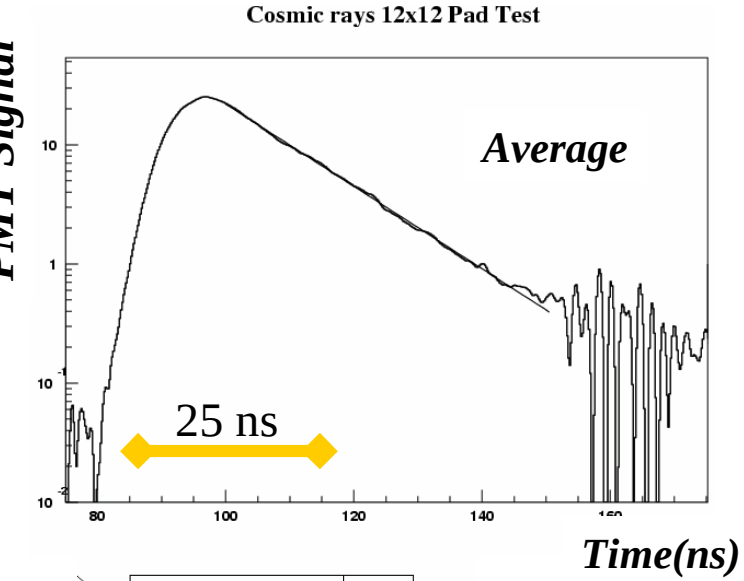
Charged particles will produce, and photons will not, ionization on the scintillator.

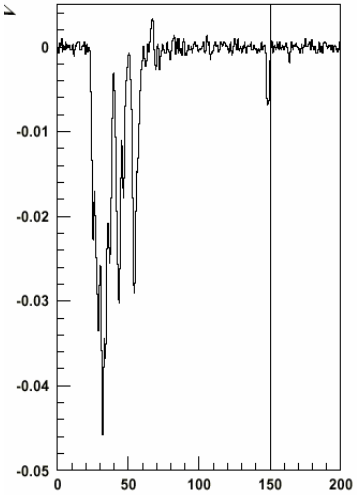
This ionization generates a light pulse that is collected by a WaveLength Shifting (WLS) fibber that is twisted inside the scintillator cell.

The light is transmitted through a clear fibber to the readout system.



Scintillator Pad Detector (SPD) Introduction(II)





MIP Single Event

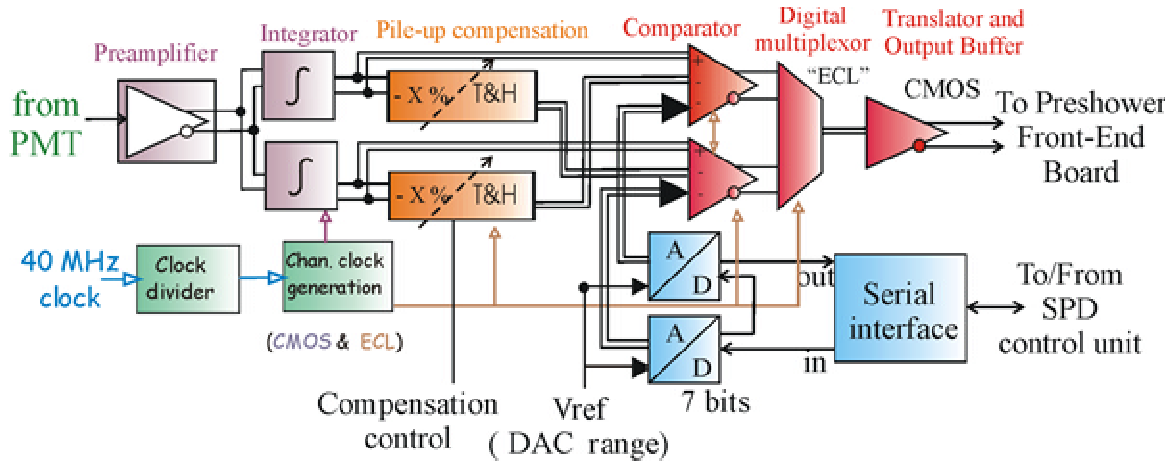
Signal Characteristics outing the PMT:

- Low photo-statistics: 20-30 phe.
- Only ~80 % of signal in 25 ns -> Pile Up Correction is needed
- No dead time on integration

Electronics Functional Solution (I)

The analog signal processing of the PMT signal is performed by an *ASIC* whose working frequency is 40MHz divided in two subchannels that work at 20MHz. The processing involves:

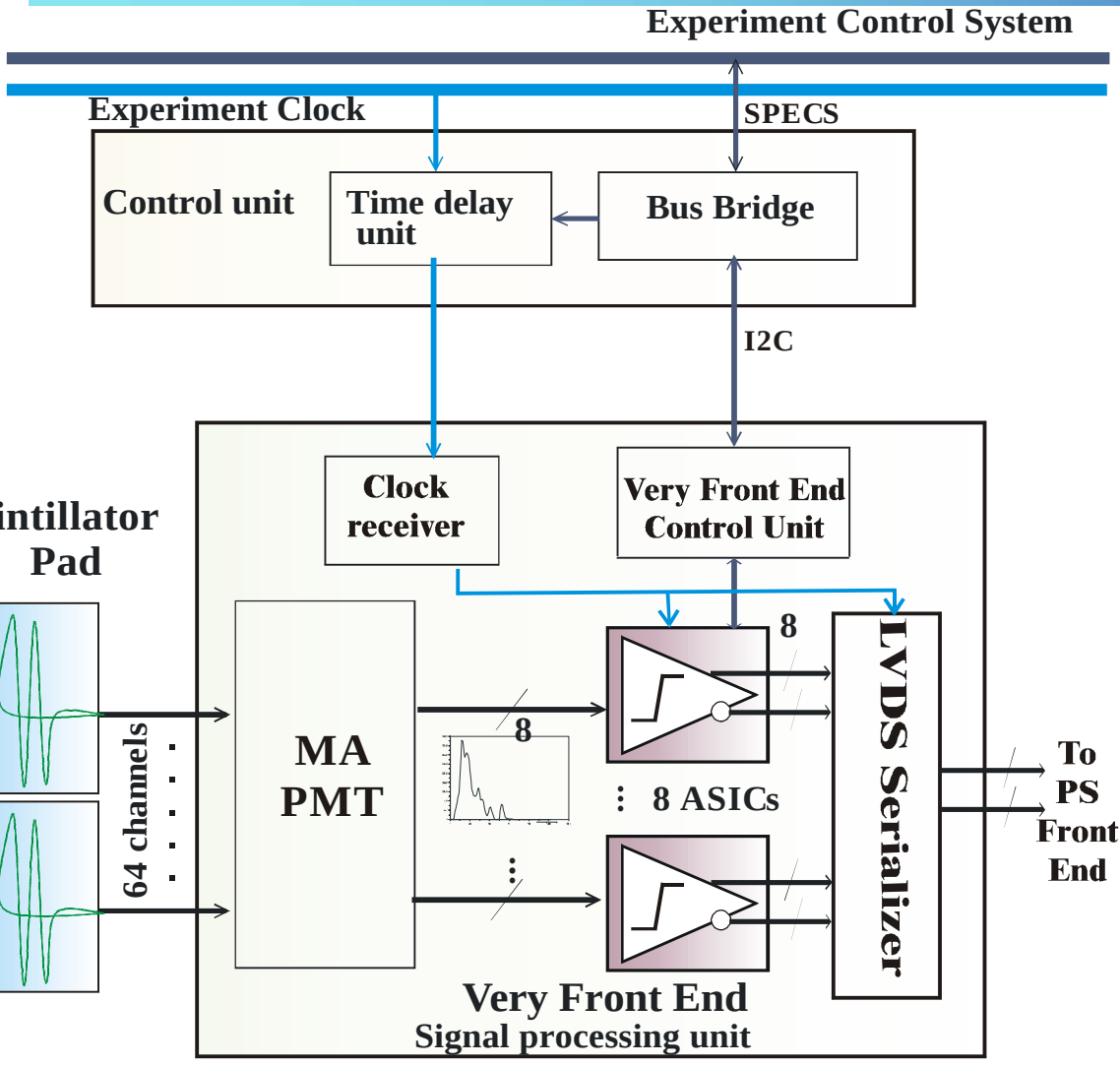
- integrating each signal,
- subtracting and adjustable fraction of the charge integrated in the previous 25ns period to perform tail correction ,
- comparing the result to programmable thresholds for each subchannel a digital output is obtained: ’1’ if above the threshold, ’0’ otherwise.



Electronics Functional Solution (II)

- Each subchannel has its own programmable thresholds in order to take care of pad size, PMT gain and non-uniformities.
- Threshold values are fixed by internal DACs sharing a common external reference.
- The programmable substractor is also set by an external reference.
- Radiation tolerant design
  - Guard rings for SEL prevention
  - Triple Voting Register (TVR) for SEU.

Electronics Functional Solution (III)



Functional design for the SPD readout is split into :

•*Very Front End board* hosting a PMT with its corresponding 8 ASICs

• *Control board* sitting at the calorimeter front end crates and interfacing the experiment control system and the VFE cards

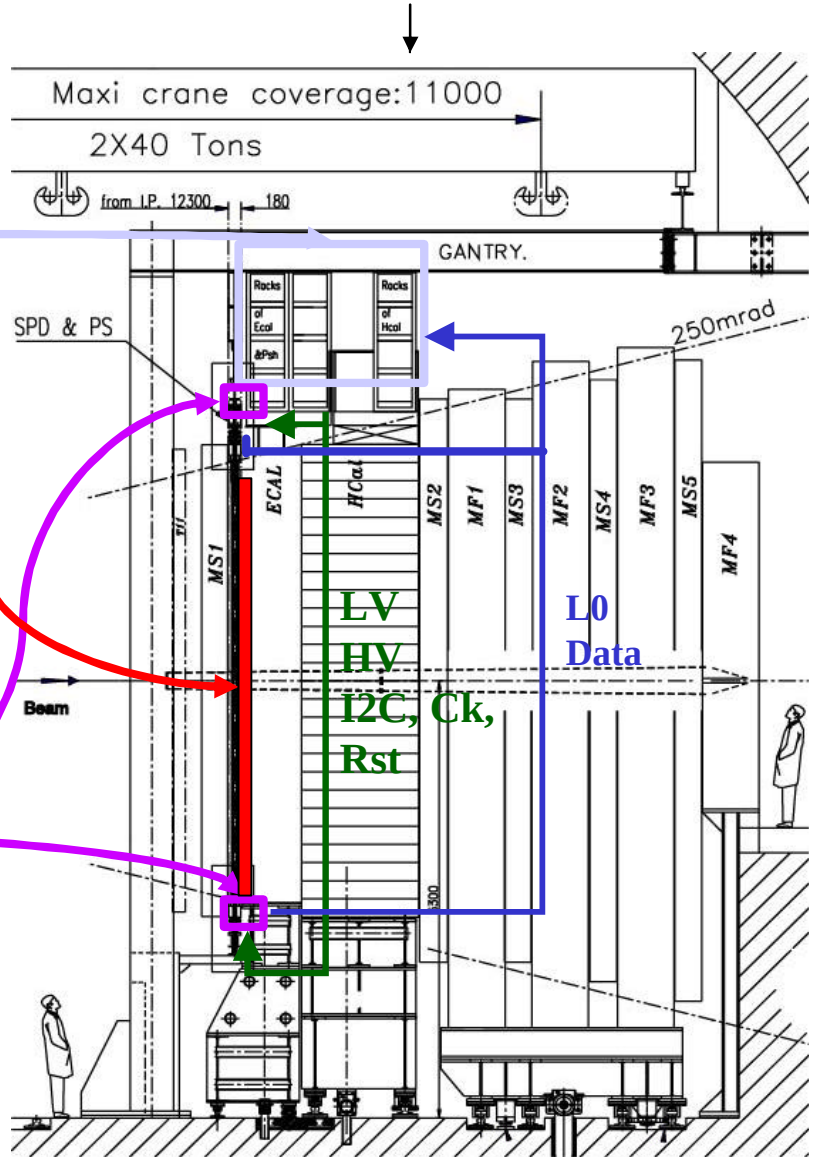
• *LV Regulator Board* that feeds the VFE Card

Situation

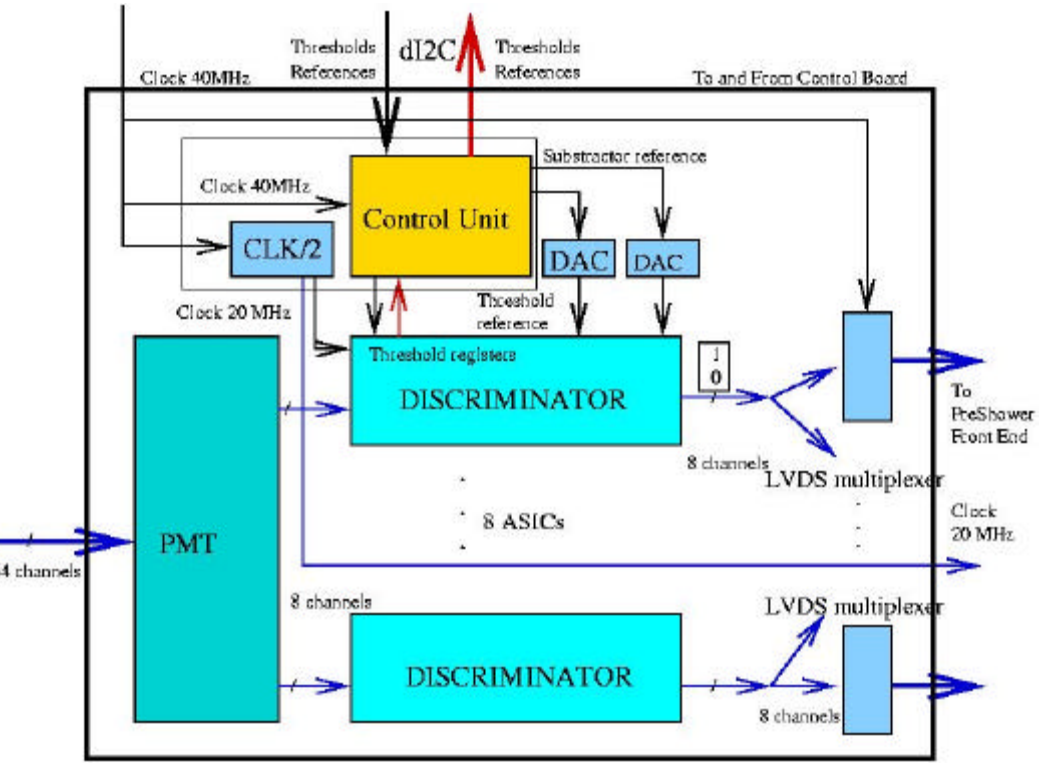
Front-end Racks: L0 Front-End Cards, Power Supplies (HV and LV) and SPD control cards

Scintillating Pad Det (SPD)
Scint. Pad + Fibres+ MaPMT
Preshower (PRS)
Pb +
Scint. Pad + Fibres+ MaPMT
5953 cells each

VFE SPD
Metalic boxes: top and bottom ends of the detector
a) VFE units:
b) Regulation cards



VFE Design Solution (I)



VFE Diagram Block

VFE board involves :

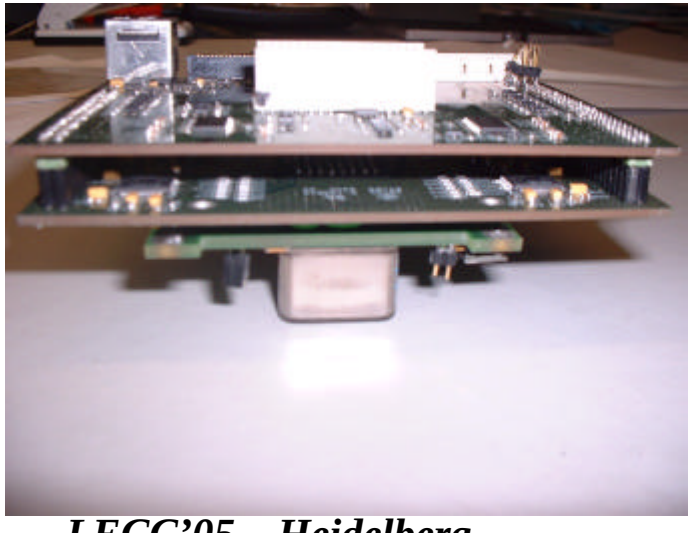
- **Changing from light signal to electrical signal** with PMTs, processing the analog electrical signal from PMTs with ASICs
- **Communication with Control Board** in FE crate in order to get the initial conditions from the ECS as programmable thresholds,
- **Multiplexing the ASIC's outputs** in time by factor 7 in order to reduce the number of output cables.

VFE Design Solution (II)

The most important components are:

- The multianode photomultiplier that is in charge of converting light to analog signal,
- ASICs (discriminator), that convert the analog signal to a digital one,
- The FPGA (Control Unit), its function is to communicating with Control Card and programming thresholds and pile-ups corrections (The FPGA is an Actel, APA300, ProAsic family, flash based)
- LVDS Transceivers, converting LVDS signal to CMOS ones,
- LVDS Serializers that prepared the ASICs digital outputs to be transmitted to the high speed LVDS (25 meters long) link.

SPD VFE Final Prototype



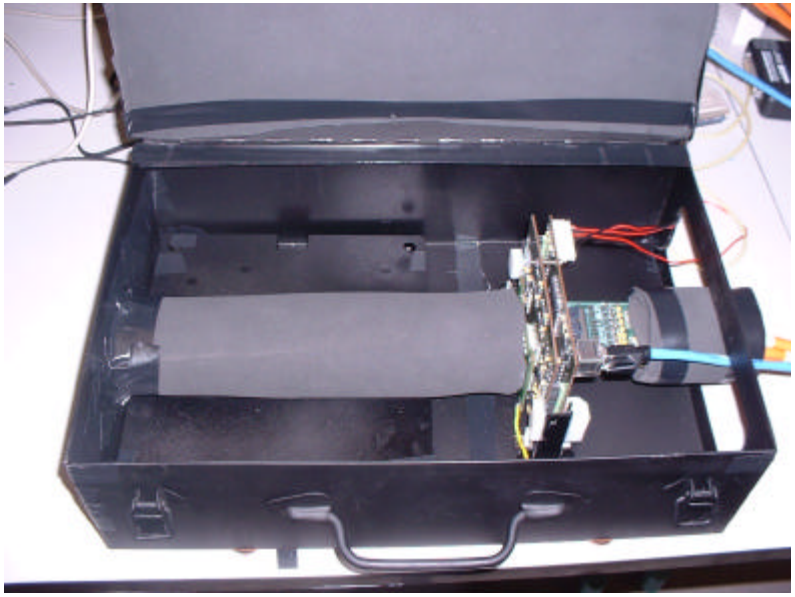
As a first attempt, the original design was only one 15cmx15cm size. As a result of the mechanical problem(MAXIMUM SIZE 12x9cm) and the functionalities added, the design has been split to three different cards:

•*Base card* which contains MAPMT[8], and the active base of the MAPMT.

•*ASICs card* which involves the 8 ASICs (discriminator in the figure) and all the analogue part (subtractor reference for compensating the pile up, threshold reference for the whole card).

•*Serializers card* which contains the LVDS serializers, for the multiplexed LVDS link mentioned before, the FPGA as a control unit, LVDS transceivers.

Laboratory Tests(I)

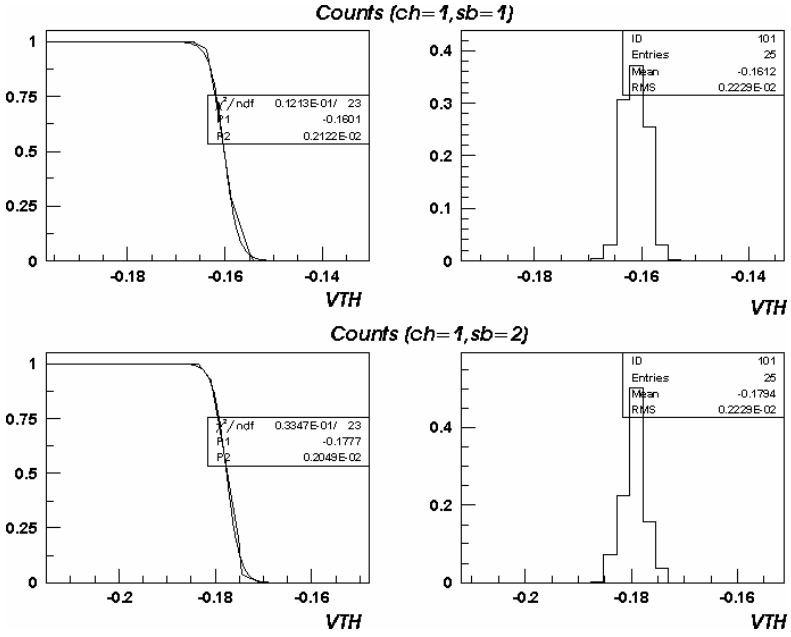


Laboratory Set Up

Functionality tests show the good performance of the card. The items tested:

- Programming internal threshold references for each subchannel in ASICs
- Programming DACs for external threshold reference and subtractor reference (pile up compensation)
- Power consumption. It is important to notice that the consumption of the card is an important point for the design of the whole system : a regulator card is needed to feed each VFE.

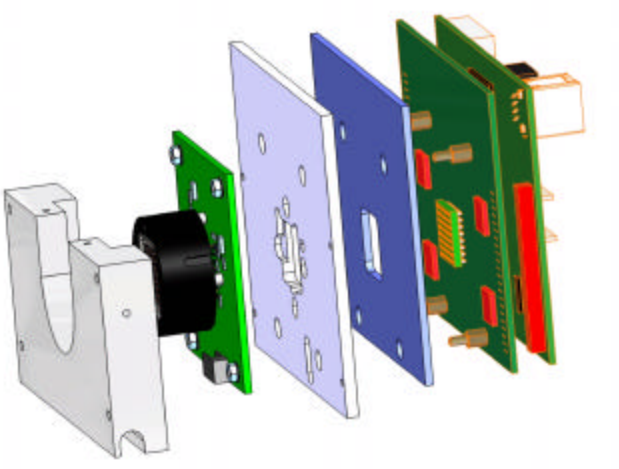
Laboratory Tests(II)

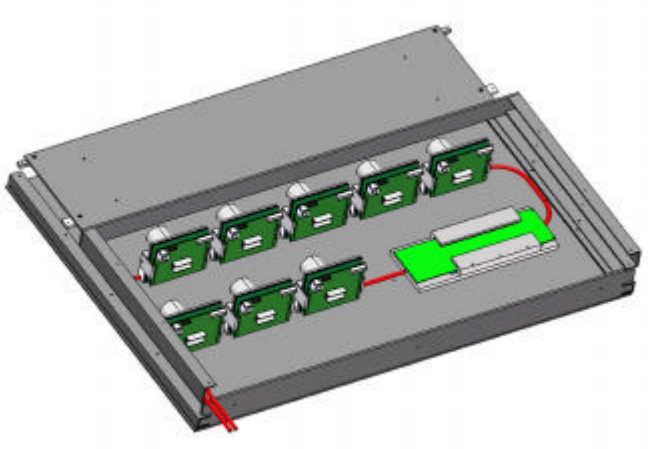


Results

- Mapping. The SPD is not a subdetector alone, it belongs to the LHCb Calorimeter, and map each PMT channel from the Photomultiplier to the other detector has become a tedious task, as a result of the asymmetry of the detector itself.
  - Noise. Its value is around 2mV and it is acceptable.
  - Clocks. The shape of the signal has been checked in order to control de jitter.

SPD VFE Cooling Tests (I)

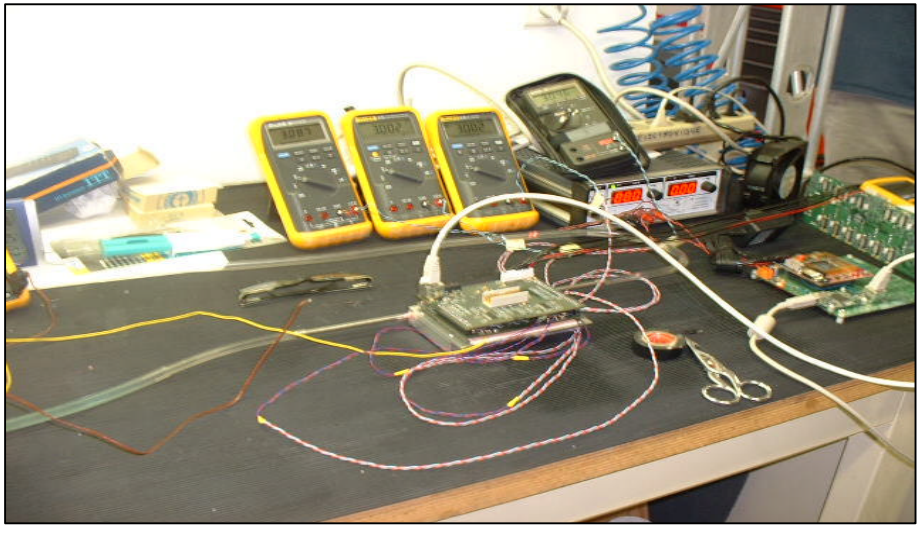




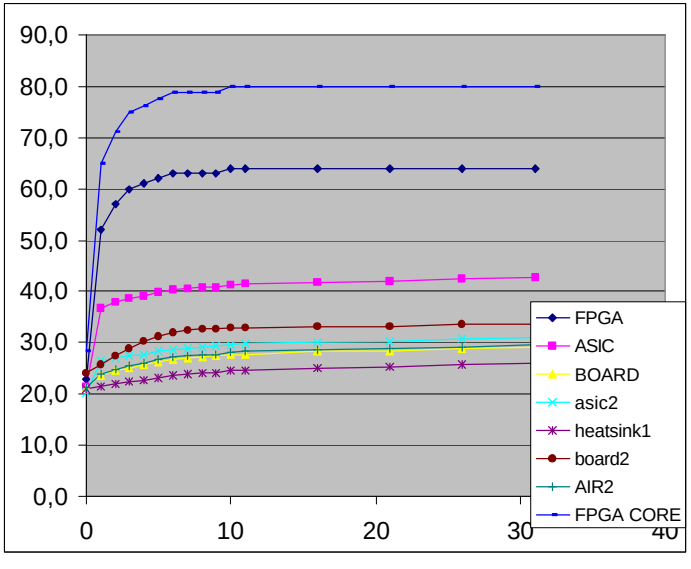
Cooling is made by a cool water circuit around boards. A conductive material of hot is put on the cards and it is in contact with an aluminium platform that contains the water circulating on.

Cooling Tests at Clermont Ferrand performed during 26-27th July 2005.

SPD VFE Cooling Tests (II)



Cooling Test Set Up



Results with water Flow from the beginning

FPGA core temperature: Coefficient 0,8 (Typical)