

SPD Very Front End Electronics

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Abstract

It is presented the readout electronics of the Scintillator Pad Detector (SPD), the front layer of the LHCb Calorimeter. SPD is in charge of distinguishing charged from neutral particles for the level 0 Trigger.

Signal from scintillator pads is converted by 64 channel Multianode Photomultiplier and processed by a full custom ASIC which delivers a single bit per channel. Those bits are sent over 25 meters through a high speed LVDS connection. Signal characteristics call for variable comparator levels and pile up correction.

I. SPD INTRODUCTION

LHCb Calorimeter [1] is composed by four subdetectors: SPD, PreShower, Hadronic Calorimeter and Electromagnetic Calorimeter. Their position is shown in figure 1. The system provides high energy hadrons, electron and photons candidates for the first level trigger (Level 0 Trigger).

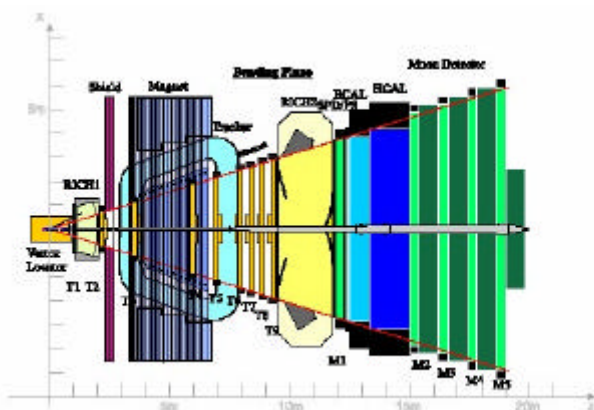


Figure 1: Layout of LHCb spectrometer

The SPD is designed to distinguish electrons and photons for the LHCb first level trigger. This detector is a plastic scintillator layer, divided in about 6000 cells of different size in order to obtain better granularity near the beam [2]. Charged particles will produce, and photons will not, ionization on the scintillator. This ionization generates a light pulse that is collected by a WaveLength Shifting (WLS)

fiber that is twisted inside the scintillator cell. The light is transmitted through a clear fiber to the readout system.

Ideally only charged particles would generate a signal. However, high energy photons can create an electron through secondary processes such as Compton effect or pair production. This phenomenon produces an energy spectra with a maximum at 0 but with a small tail for high energies (see figure 2) (provoking that some photons are identified as electrons [10]). Applying a threshold at 1.4 MeV (≈ 0.7 MIP) is a good compromise to reject the photons with not too bad efficiency for the trigger. The resolution of the discriminator must be better than 0.05 MIP in order to keep the energy resolution given by photostatistics in this threshold area. The maximum average current that can be used to avoid a fast aging limits the gain of the PMT. For the cells with higher occupancy the MIP signal will be limited to 100fC. Active bases shall be used to keep acceptable linearity at low HV (high voltage).

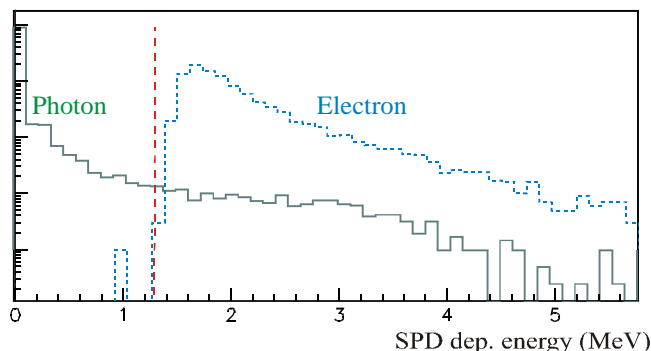


Figure 2: Deposited energy at SPD.

The signal outing the SPD PMTs is rather unpredictable as a result of the low number of photostatistics, 20-30 photoelectrons per MIP, and due to the response of the WLS fibre, which has a decay time of around 12 ns (figure 3). This “slow” decay time means also that the signal spreads over more than one clock period. According to present data about the 80% of the signal is in the first period. This fact causes another bothering trouble: the potential tail of a high amplitude event could cross the threshold and provoke a fake trigger. Thus, pile-up correction is needed. A range of at least 5 MIP is required to be able to perform this compensation.

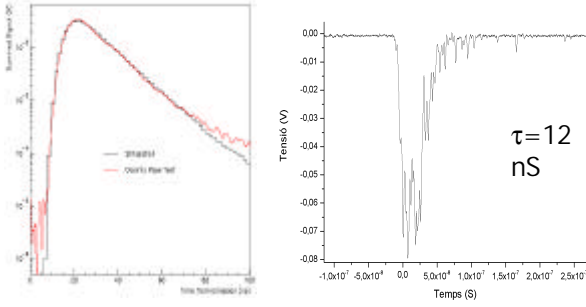


Figure 3: Typical MIP signal shape: (left) average and (right) pulse shape

Although the fiber response creates a pole at $\approx 30\text{MHz}$, events with single photoelectron components can be observed due to the low photostatistics. Thus the bandwidth of the system must be higher than the PMT one (about 100MHz). Temperature drifts must be taken into account. A band gap current source is the base reference for all the blocks, to have good temperature stability. The linearity error must be smaller than 5% of the full scale.

II. ELECTRONICS FUNCTIONAL SOLUTION

The analog signal processing of the PMT signal is performed by an ASIC whose working frequency is 40MHz divided in two subchannels that work at 20MHz [9] (See figure 4). The processing involves:

- integrating each signal,
- subtracting and adjustable fraction of the charge integrated in the previous 25ns period to perform tail correction,
- comparing the result to programmable thresholds for each subchannel a digital output is obtained: '1' if above the threshold, '0' otherwise.

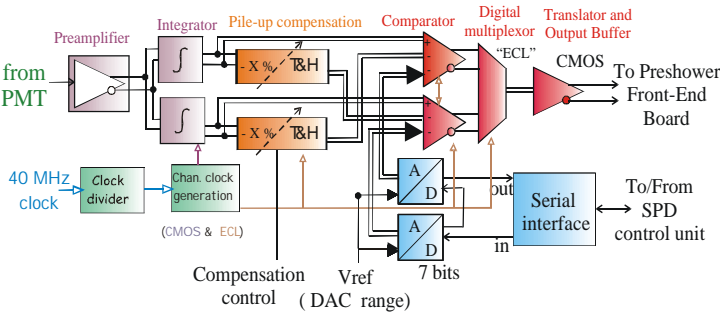


Figure 4: Functional diagram of a discriminator channel.

Each subchannel has its own programmable thresholds in order to take care of pad size, PMT gain and non-uniformities. Threshold values are fixed by internal DACs sharing a common external reference. The programmable subtractor is also set by an external reference. Final implementation, where each ASIC encapsulates 8 channels, is made using $0.8\ \mu\text{m}$ BiCMOS technology. Bipolar transistors are needed for

the analog parts, specially to reduce offsets, and MOS transistors are used as switch elements as well as to reduce power consumption in the digital parts. To improve radiation tolerance, ring guards protect analog transistors and digital operations are implemented using a triple voting system.

From those elements, functional design for the SPD readout is split into a Very Front End board hosting a PMT with its corresponding 8 ASICs and a control board sitting at the calorimeter front end crates and interfacing the experiment control system and the boards, as depicted in figure 5. Very Front End boards shall be located in boxes sitting on the top and the bottom of the detector, limiting the area of the VFE board to $9 \times 9\text{cm}^2$.

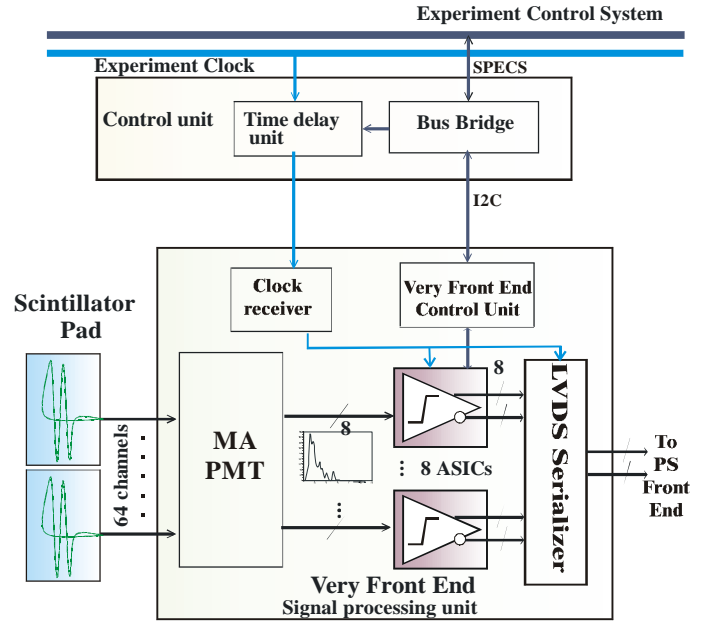


Figure 5: SPD readout system

In order to save connector space data shall be sent to the PreShower front end card by a multiplexed LVDS link.

Threshold values shall be dynamically fixed from the experiment control system through the control board, which shall also provide the system clock.

III. VFE DESIGN SOLUTION

Very Front End Cards are the heart of the readout electronics since they are in charge of the pad signal processing and the sending of the resulting bits to the Preshower Front End Card[1].

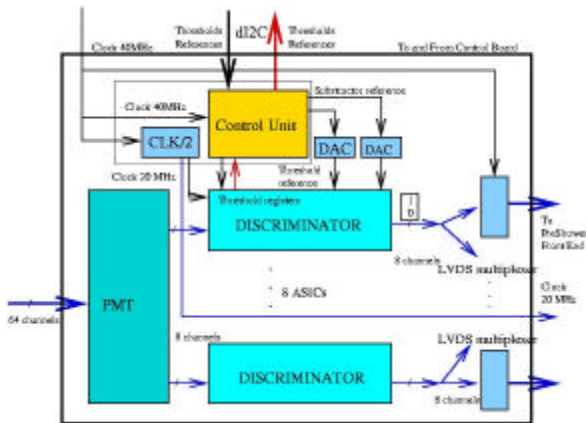


Figure 6: VFE Diagram Block

The most important components are:

- The multianode photomultiplier that is in charge of converting light to analog signal,
- ASICs (discriminator in the figure above), that convert the analog signal to a digital one,
- The FPGA (Control Unit), its function is to communicating with Control Card and programming thresholds and pile-ups corrections,
- LVDS Transceivers, converting LVDS signal to CMOS ones,
- LVDS Serializers that prepared the ASICs digital outputs to be transmitted to the high speed LVDS (25 meters long) link.

All of the components have been irradiated in order to pass the radiation qualification[6] (Single Event Effects and Cumulative Effects). Some useful components had to be discarded because they do not support the levels of radiation (E.g. DS90CR494, 64-channel LVDS multiplexer).

One of the challenges that the design of VFE board has it is the voltage levels of components. For e.g. ASICs voltage supply is (+/-1.65V), and the output of the board should be 3.3V (in order to communicate the PreShower[1] FE board-to SPD VFE board). This implies that it has to be a voltage level adaptation between both boards. This adaptation is made by a passive circuit (2 PIN diodes and 2 resistors).

A. Prototype

In the first design, all this functions were designed to be in the same card. After this first attempt, for mechanical constraints, VFE board has been splitted into three different boards:

- PMT Base Board
- ASICs Board
- Input Stage/ Control Unit / Output Stage Board

1) PMT Base Board

For compatibility and cost reduction, this card is the same as Pre-Shower one[1] .

2) ASICs Board

This board contains the connection to the PMT Base Board, the eight ASICs and its associated circuitry and the part of threshold reference and subtractor reference.

It is a ten-layer card, with components on both boards, top and bottom layer.

The figure below shows the card with PMT Base card.

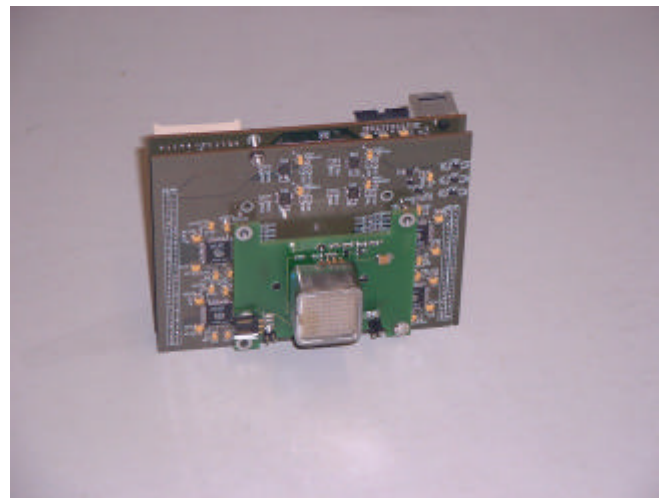


Figure 7: Boards

3) Input Stage/ Control Unit / Output Stage Board

The board contains the input stage (connectors, transceivers, adaptation), the control unit (FPGA) and the output stage (asic's output adaptation, serializers and output high speed LVDS connector).

The figure 8 shows the card:

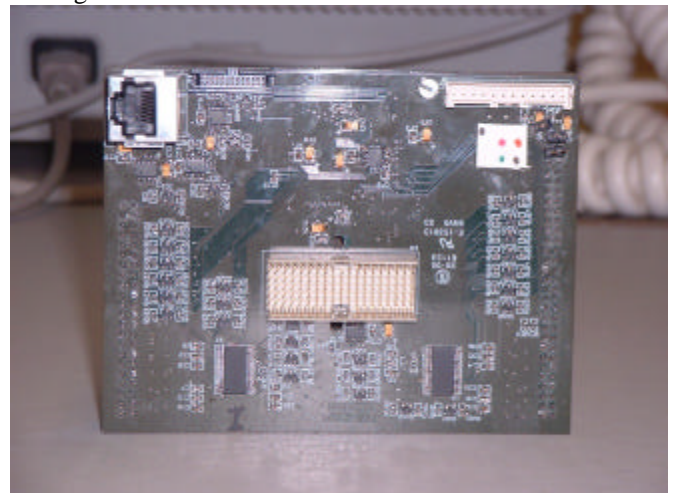


Figure 8: Serializer's Board

B. Test and Preliminary Results

As a preliminary results on a test beam at CERN performed on July 2004 with an old prototype (without FPGA inside the card) , the system worked properly, its functionality was correct and nothing seem not to work.

Laboratory tests of the final prototype have been done about functionality and cooling.

The functionality tests show the good performance of the card. The items tested:

- Programming internal threshold references for each subchannel in ASICs
- Programming DACs for external threshold reference and subtractor reference (pile up compensation)
- Power consumption. It is important to notice that the consumption of the card is a relevant constraint for the design of the whole system: a regulator card is needed to feed each VFE.
- Mapping. The SPD is not a subdetector alone, it belongs to the LHCb Calorimeter [1], and mapping each PMT channel from the Photomultiplier to the other detector has become a tedious task, as a result of the asymmetry of the detector itself.
- Noise. Its value had been measured and it is around 2mV and it is acceptable.
- Clocks. The shape of the signal has been checked in order to control the jitter.

The cooling tests, has been done in Clermont-Ferrand at LPC (Laboratoire Physique Corpusculaire) last July.

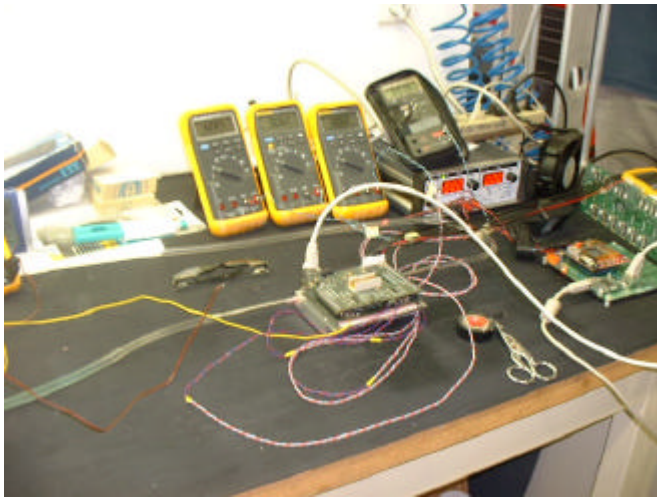


Figure 9: Cooling Test

The cooling is made by a cool water circuit around boards. A conductive material of heat is put on the cards and it is in contact with an aluminum platform that contains the water circulating on.

The results showed that the maximum temperature achieved is near the limit of the maximum value of temperature for the FPGA.

On one hand, FPGA consumption tests are been done at the moment, showing a lower power consumption than in the test, and on the other hand, more work has to be done in cooling in order to have some tolerances in temperature.

This prototype has been reviewed on a FDR (Final Design Review).

IV. ACKNOWLEDGMENTS

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