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A Silicon Strips Detector Readout Prototype Chip in 180 nanometer CMOS Technology

A 16-channel readout chip for Silicon strips detectors has been designed in 180 nanometer CMOS technology and tested. It includes low-noise amplification, pulse shaping, sampling and threshold detection. An input referred noise of 190 + 12 electrons/picoFarad for an integration time of 3 microseconds has been measured, leading to an overall signal to noise ratio of 30 and a dynamic range of 75 Minimum Ionizing Particles at +/- 1.5 linearity, for a 60 centimeter long strip. Power dissipation is 350 microWatt per channel, area is 0.05 square millimeter.

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