Contribution ID: **23** Type: **Poster**

A real time electronic emulator with realistic data generation for reception tests of the CMS ECAL front-end boards.

The electromagnetic calorimeter (ECAL) of the CMS experiment is equipped with ˜3000 front-end boards (FE) performing both trigger and data readout functions. Prior to their integration at CERN in the ECAL detectors the FE boards are tested using a dedicated test bench located in Laboratoire Leprince-Ringuet. This test bench, called XFEST, was designed and built for testing as much as 12 FE boards at the same time. The tests are performed by injecting the same digital input patterns with a 40 MHz rate on the 12 FE boards and by comparing their 24 output signals. Failures in the behavior of bad FE boards are signalled by different output signals from those of a reference FE board. This contribution describes the solution developed in order to create a real time emulator of realistic digital input patterns at 40 MHz rate as well as the implementation of a real time comparison of the 12 FE boards output streams.

Summary

Each ECAL front-end board receives 25 digital signals of 14 bit at a 40 MHz clock frequency from the very front-end electronics (VFE). These signals are processed by seven dedicated asics called FENIX. In order to emulate the 25 digital input vectors a prototype version of the FE board equipped with commercial programmable circuits in place of the FENIX asics has been used. This board called EF is installed on a motherboard designed and developed at LLR. The main role of this motherboard is to insure the duplication of the 25 digital signals in order to feed four FE boards. There are three motherboards in total each one equipped with one EF board in order to test at the same time 12 FE boards. The output digital signals of the four FE under tests are shipped by optical fibers to a prototype of the Trigger and Concentrator Card (TCC) in the same way as the final ECAL lectronics. The TCC is also equipped with commercial programmable circuits. In order to perform the real time comparison between the FE output signals the TCC firmware has been modified.

- For the 25 VFE signal's emulators, the analogue shape and the pileup characteristics of these signals have been implemented. Noises and pedestals are digitally emulated, the trigger occurrence distribution and energy amplitude are randomly generated according to pseudo Gaussian distributions. Amplitude gains, energy range, level of noise or pedestals are all programmable via an integrated I2C interface.
These capabilities imply a great flexibility and very efficient way to tune specific parameters.
- For the comparison system, the main issue is to aggregate and compare in a same clock domain all data from different clock time buckets. The real time computing of all input data is a key point to solve buffer control problems. Parameters setup like reference card selection is possible with an embedded VME interface. Diagnostic and error counting are included in the design.
This presentation will describe a solution to efficiently test a large set of complex electronic cards with many input ports and high throughput data rate. Algorithm to emulate the VFE signals is embedded in field gate programmable array circuits. The test bench will also be presented.

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