Evolution of the TRT backend and the new TRT-TTC board

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Abstract

The Transition Radiation Tracker, made of 370000 cylindrical straws, is a combined tracking and electron identification detector, which is part of the ATLAS Inner Detector at the CERN LHC. The TRT on-detector electronics is made of 2 types of custom asics, handling the analogue signals from the straws, providing a ternary encoded output (ASDBLR), binning the incoming tracking discriminator signal into 3.25ns bins and storing up to 6 microseconds of level 1 storage (DTMROC). This on-detector electronics is joined to the off-detector electronics via patch-panels in charge of data distribution.

The off-detector is comprised of three types of modules: the Timing, Trigger and Control (TTC) module, the ReadOut Driver (ROD) and the ReadOut Buffer (ROB).

TRT readout system was already described [1],[2],[3]. The status of the final system for ATLAS application will be given.

I. ATLAS/TRT READOUT

A. Overview

An overview of the TRT read-out system is shown in Fig. 1. The TRT on-detector active electronics consists of the ASDBLR and DTMROC custom chipset. The ASDBLR handles analog signal processing from 8 channels (8 straws) and provides a ternary encoded differential output of both tracking and transition radiation discriminators to the DTMROC. The DTMROC, handling 16 channels, bins the incoming tracking discriminator signal for each channel into 3.25 ns bins, provides about 6 microseconds of Level 1 storage, a 42-event output buffer (derandomiser), and various support functions like threshold settings and test pulses for the ASDBLR's. The event data are serialised and send on a single LVDS link at 40 Mbits/s when a level-1 accept signal (L1A) occurs. These ASICs are detailed in [4].

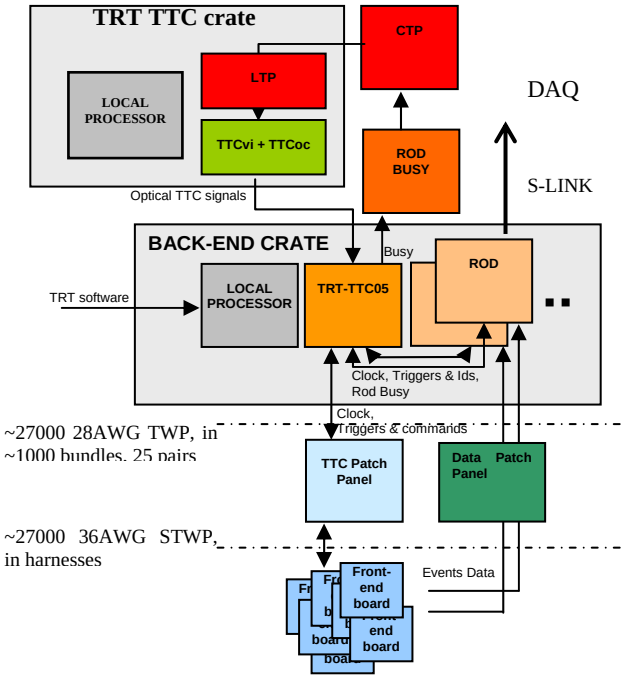

Figure 1: TRT readout system

The chips are arranged on detector mounted printed circuit boards in modular groups of 10 to 18 DTMROCs depending

upon the particular geometry of each region of the TRT detector. Each group (or board) is then linked via cables to the off-detector electronics.

The on-detector electronics are joined to the off-detector electronics via a Patch Panel which repeats the LVDS signals and sends them to the RODs via 28-gauge, 50-pair twisted pair cables that run approximately 100m. The same cables are used for bringing the control from TTC module.

The off-detector electronics is comprised of the Timing and Trigger Control (TTC) module, the Readout Driver (ROD) and the Readout Buffer (ROB). The readout system provides timing and control signals to the front end with timing information distributed to a precision of 0.5 nsec. In response to a trigger, the system reads event data from the front-end modules and must function with minimal deadtime up to the ATLAS LVL1 trigger rate of 100 kHz. Each ROD reads out 104 DTMROC's (1664 channels); it receives 104 serial links running at 40 Mbits/s, check data integrity, compresses the data and builds a complete event to be sent to the ROB module via an ATLAS standard Gbit link (S-link). The system must be partitionable such that subsets of the electronics can provide data acquisition needs during fabrication of the detector modules and such that different portions of the TRT or Inner Detector can operate autonomously during the commissioning and debugging phase of the experiment. To satisfy these requirements, the off-detector readout and control system is a modular, VME-crate based solution. Groups of TTC and ROD modules are placed in VME crate together with a Single Board Computer (SBC) and module able to introduce dead-time in case of ROD buffers overflow (BUSY module). The four TTC partitions of the TRT (Barrel A and C, End-cap A and C) are driven from one TTC crate providing trigger, timing and control signals. Each partition contains a Local Trigger Processor (LTP), a TTCvi, a TTCex and a TTCoc [6],[7] for generating TTC protocol and sending signals over optical link.

B. Modifications

The possibilities of state-of-the-art FPGAs and the necessity of reducing the overall system cost, lead to increase the density of channels per VME board by factor two. Thus a ROD module is now serving 240 links (DTMROC chips) which corresponds to 1/32 of an endcap side or 2/32 of a barrel side. The TTC module is now serving 40 TTC links which corresponds to 2/32 of endcap or 4/32 of barrel. One TTC module and two ROD modules communicates over a custom P3 backplane and form the basic readout unit of the TRT. Five to six such units are placed in one VME crate, and the whole TRT is readout by 10 VME crates.

Copper twisted pair links from data Patch Panel 2 (PP2) to the RODs are replaced by 1.6Gbit/s optical links. Each optical link on PP2 concentrates data from up to 30 40Mbit/s links (miniature individually shielded twisted pair) from the front-end. Such a step requires to add a control to data PP2 via an I2C interface using standard CAT5 Ethernet cables and I2C master on the ROD. Thus approximately 24000 twisted pairs were replaced by 800 optical fibres.

The TTC PP2 contains clock fan-out with fine delay adjustment of 0.5 ns, temperature measurement for the detector and the front-end boards and a programmable FAST OR generation for building cosmic trigger. The fine delay setting is done over an I2C interface from the TTC module using free twisted pair lines in the TTC link bundle and while the other control functions are done over a CANBUS interface and an ELMB module [15] mounted in PP2.

Transmission of 40 MHz signals over long distance cables (up to 100 meters) requires some care. Passive cable equalizers are now replaced by active ones, which provided lower jitter and better signal quality. Fig. 2 shows the eye diagram of LVDS 40Mbits/s signal after 100 meters of TWP28AWG and passive filter and Fig. 3 shows the eye diagram of LVDS 40Mbits/s signal after 100 meters of TWP28AWG and an active filter.

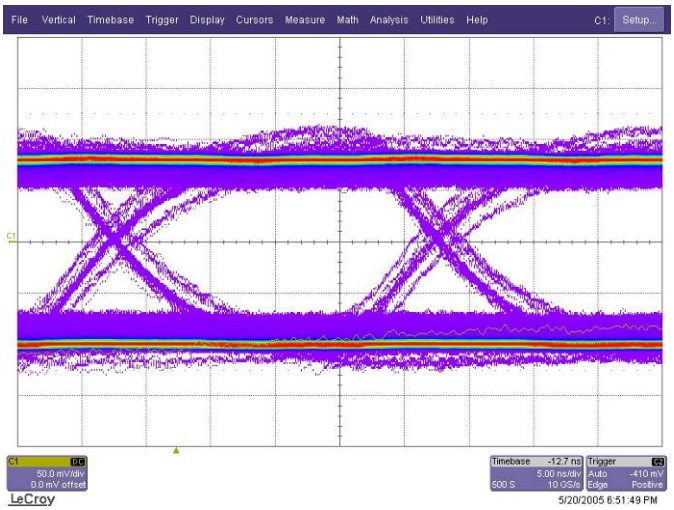

Figure 2: LVDS signal after 100 meters of 28AWG twisted pair and passive filter

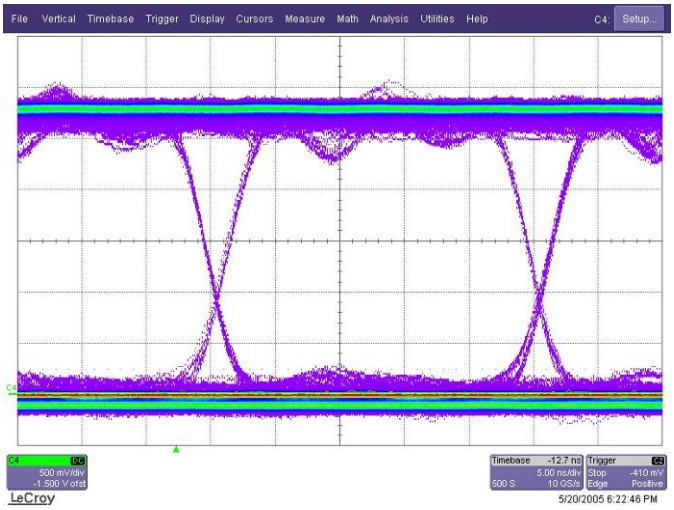

Figure 3: LVDS signal after 100 meters of 28AWG twisted pair and active filter

Short summary of the most important changes are given in Table 1.

	Initial system	Final system
Number of RODs	256	96
Number of links per ROD	104	240
Number of TTCs	96	48
Number of links per TTC	18	40
Number of RODs per TTC	3	2
Number of links from PP2 to USA15	24000 TWP	800 optical
Link speed	40 Mbit/s	1.6 Gbit/s
Number of VME crates	22	10
TWP equalizers	Passive	Active
Data compression	Content based	Huffman
Cosmic trigger	No	Yes

Table 1: summary of modifications

C. *Partitioning*

The TRT detector is divided to 4 main partitions; end-cap side A and C, and barrel side A and C. There is a VME rack assigned to each partition. Each end-cap partition is readout by 3 VME crates, each barrel partition by 2 VME crates. Each crate contains five to six readout modules composed of 1 TTC module and 2 ROD modules. Patch panels are located at 6 positions around ATLAS servicing 3/32, 5/32 and 8/32 of TRT. They are arranged in boxes, each box containing all patch panels for 1/32 of detector side. There are 2 TTC patch panels connected to TTC module and 4 data patch panels connected to 2 ROD modules per PP2 box.

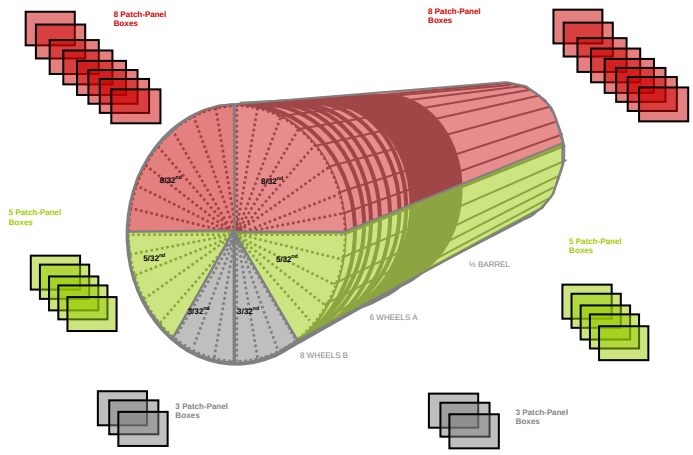

Figure 4: Patch panels boxes for one side of TRT

II. VME BACKEND MODULES

A. *TRT-TTC module*

This module is used to implement TTC [6] and TRT specific command functions and parameter loading for front-end electronics. It receives one encoded TTC signal over an optical line from the TTC modules [7] and a TTCrx chip [8] decodes this signal. It extracts the clock (BC), the L1A, the bunch counter reset (BCR) and the event counter reset (ECR) commands and receives trigger type information. Through the custom lines it downloads parameters to the front-end electronics. There are 40 TTC links arranged on 4 connectors served by the module in total. It distributes the clock and commands both to the front-end electronics and the ROD modules. All lines to the front-end electronics have adjustable delay. For test beam and system tests purposes it can receive commands from the front panel (NIM). For dead time monitoring purposes it measures the duration of the BUSY signals generated by the S-LINK and the on-board buffers control. A combined BUSY signal is sent to the Central Trigger Processor through a BUSY module [7]. 9U VME prototype is in Fig. 5.

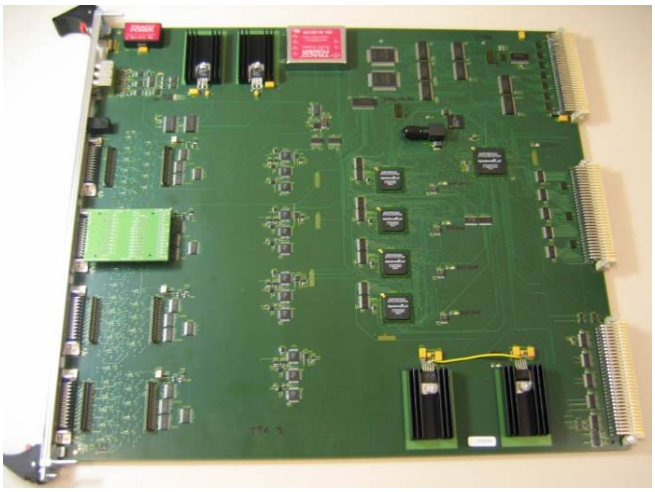

Figure 5: TRT TTC VME module

TTC module provides number of different modes for writing and reading back parameters and status to/from the front-end. The basic one is the direct access from VME bus which is adequate for system test. For downloading all parameters to the detector this mode would be too slow, so a so-called INIT mode is implemented. Upon receiving this command, TTC module writes all parameters to the front-end on all TTC links simultaneously; parameters are stored in the board memory. Optionally, in this mode the board can read-back the parameters and compare them with expected values. During data taking, it is expected that some register content on front-end electronics would be corrupted due to the radiation effects (single event upsets). The TTC module provides either a polling mode for checking the content of all registers or a refreshing mode for periodical refresh of all registers. For these modes, the LHC beam structure is used.

The beam gaps assigned to TRT detector are used for accessing TTC links which must be otherwise free for sending triggers and TTC commands.

DTMROC chips could be switched to Fast OR mode for cosmic trigger purposes. In this mode, TTC modules receives Fast OR signals on parameter read-back lines and forms a trigger using a simple on-board logic. For a more complicated trigger building it further propagates Fast OR lines to VME P2 connector where a dedicated extension module can be plugged.

B. ROD module

It receives inputs from 240 DTMROCs mounted on the TRT detector and clock/control signals from the TRT TTC located in the same VME crate.

The ROD is responsible for checking the synchronization of the data and compressing them. After processing, the data are sent out to the ROBs via the SLINK transmitters mezzanine.

A fraction of this data will also be stored in a spy buffer (FIFO) which will be readable from VME. This allows the crate SBC to spy on the data for monitoring purposes. Since the encoding scheme used is completely lossless there is no need to have separate buffers to contain the uncompressed and compressed data. Note also that the spy buffer will contain fully-built events exactly as they are present to the SLINK output.

The current design uses a lossless, entropy-based encoding (Huffman encoding). The idea behind the compression is that for each straw, we readout 27 bits of data. Though there are 2^27 different possible bit patterns, only a relatively small number have physical significance. The relative frequency of the 500 most common 27- bit patterns are shown in Figure 6, based on Monte Carlo simulations for both 10^{33} and 10^{34} cm^{-2} instantaneous luminosity. Huffman's encoding algorithm, in which common patters are given short codes, while rare patterns have long codes, comes very close to the theoretical limit of the fewest bits needed to represent the information in the data stream (based on the entropy of the data), as shown in Table 2.

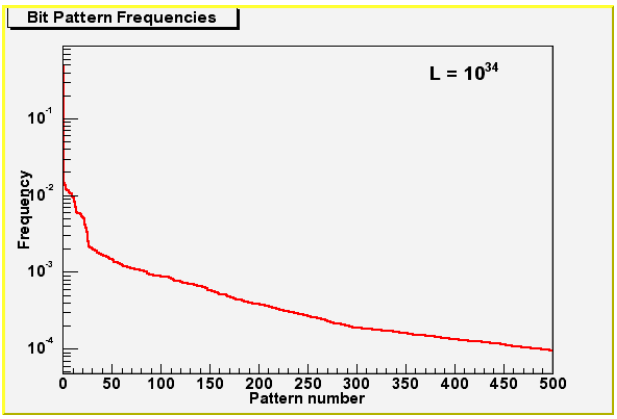

Figure 6: The relative frequency of the 500 most common 27- bit patterns

Luminosity	Occup.	Information/straw	Encoded bits/straw
10^{33}	7.2%	1.02 bits	1.65 bits
10^{34}	52.5%	6.15 bits	6.18 bits

Table 2: effective number of bits of information each straw holds, compared with the number realized by a Huffman encoding.

III. PATCH PANELS

Patch panels boards installed in PP2 boxes are TTC, data and power supply patch panels.

TTC patch panel serves 20 TTC links from TTC module. For each LVDS line it provides signal repeater to refresh signals after 100 meters of 28AWG twisted pair. It provides fine delay adjustment in steps of 0.5ns controlled via I2C interface from TTC module. The links are regrouped on patch panel to match detector partitioning. For cosmic trigger purposes it provides programmable Fast OR on incoming lines from the front-end electronics. Temperature measurement for both detector and front-end electronics is provided through ELMB module (CANBUS interface).

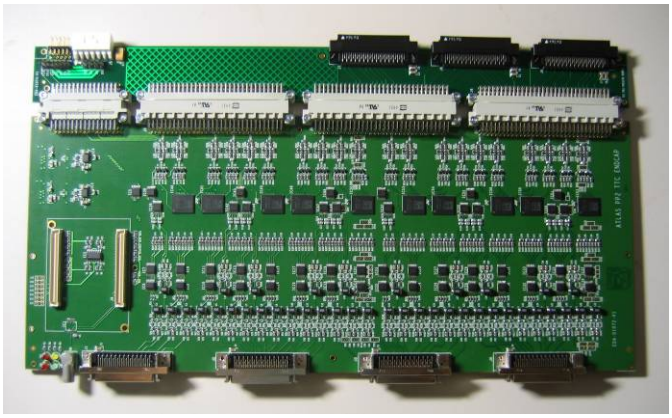

Figure 7: TRT TTC patch panel

Data patch panel receives 120 data links 40Mbit/s from DTMROC chips. After phase alignment it combines data from 30 links. These data are serialised at 1.6 Gbits/s by the GOL chip [13], which output feeds a radiation tolerant VCSEL connected to an optical fibre. Bunch crossing clock and I2C control are transmitted over CAT5 Ethernet cable. The clock for GOL chip is further cleaned by the phase locked loop of the QPLL ASIC [14].

IV. CONCLUSIONS

The final TRT readout system should be ready for system tests during the fall of 2005. Important changes have been introduced, leading to the reduction of number of VME boards by factor 2. A big part of the copper readout cables from PP2 to the RODs have been replaced by smaller number

of fast optical links. The new system is modular and scalable to allow partitioning of TRT detector for ATLAS application.

V. REFERENCES

[1] ATLAS Technical Proposal , CERN/LHCC/94-43 LHCC/P2 , 15 December 1994

[2] The ATLAS TRT Readout System, P.Lichard, LEB 1996

[3] The new ATLAS TRT Readout System, P.Lichard, LEB 2000

[4] DTMROC Project Specification v.2.1.3, ATLAS TRT Technical Note

[5] Backend VME Module for ATLAS TRT Readout System, P.Lichard, LEB 1998

[6] TTC Distribution for LHC Detectors, IEEE Trans Nuclear Science, Vol.45, No.3, June 1998

[7] Timing, trigger and control distribution and deadtime control in ATLAS, P. Gallno, LEB 2000

[8] TTCrx Reference Manual, J. Christiansen, A. Marchioro, P. Moreira, T. Toifl, RD12 Project

[9] Grounding and Shielding of ATLAS TRT, M.Mandl, ATLAS TRT Technical Note, March 2000

[10] Akesson et al. NIM A367(1995)143-153

[11] Akesson et al. NIM A372(1996)70

[12] Akesson et al. NIM A412(1998)200

[13] GOL data sheet, CERN PH-EP/MIC group

[14] QPLL data sheet, CERN PH-EP/MIC group

[15] ELMB documentation, http://elmb.web.cern.ch/ELMB/elmb128.html