The Front-End Electronics System for the CMS Electromagnetic Calorimeter

N. Pastrone on behalf of the CMS ECAL Group

I.N.F.N., Via P. Giuria 1,10125 Torino, Italy
Nadia.Pastrone@to.infn.it

Abstract

CMS designed an high precision electromagnetic calorimeter, to be operated reliably in the high radiation environment of the CERN Large Hadron Collider (LHC), inside the 4 T magnetic field. Innovative solutions were developed to place the front-end electronics within the detector with the advantage of minimizing external noise, while reducing the number of optical links to send data to the off-detector readout. The final system architecture will be reviewed in detail. High resolution, over the wide energy dynamic range, was obtained with studies in an electron test beam.

I. INTRODUCTION

A very high performance, homogenous electromagnetic calorimeter (ECAL) [1], in Figure 1, is part of the general purpose Compact Muon Solenoid (CMS) [2] experiment, built to study the 14 TeV proton-proton collisions at LHC with nominal luminosity of 10^{34} cm $^{-2}$ s^{-1}.

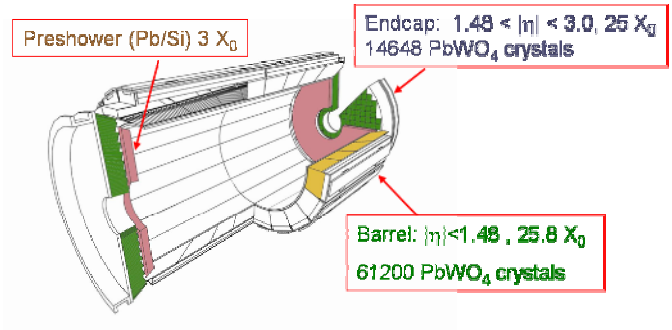

Figure 1: View of the CMS electromagnetic calorimeter: subdivided in 36 SuperModules of the barrel and 4 Dees of the endcaps

ECAL was designed to precisely measure energy and position of e, γ and π^0. To be able to detect the narrow width signal such as Higgs boson decay H→γγ (m_H<150 GeV/c^2), the best energy resolution, $\frac{\sigma(E)}{E} = \frac{a}{\sqrt{E}} \oplus b \oplus \frac{c}{E}$, is required:

- *a*, the stochastic term, including shower fluctuation, photodetectors statistics and transverse shower leakage, should be a ~ 2.7% GeV$^{1/2}$ in the barrel.
- *b*,, the constant term, dominant at high energies, due to mis-calibrations, non-uniformities, instabilities in the temperature and high voltage, is aimed to be b ~ 0.55%.
- *c*, the noise term, due to electronic noise, incremental dark current with irradiation and pile-up, is aimed to be in the barrel c ~ 155(210) MeV for low (high) luminosity.

The major challenges to be faced are the ability to operate in a strong magnetic field of 4 T and under unprecedented radiation levels, the LHC bunch crossing rate of 40 MHz, the need of a precise energy measurement over a very large dynamic range (from ~ 50 MeV to more than 1 TeV), and the high reliability required of the full on-board readout chain which will be inaccessible during the full data taking.

To achieve such requirements, crystals of lead tungstate ($PbWO_4$), with fast scintillation light emission (80% collected in 25 ns), have been chosen as active medium. The short radiation length X_0=0.89 cm and the small Moliere radius R_M=2.19 cm, allow for a compact design to fit into the 4 T solenoid and high granularity. Radiation hardness is sufficient to operate in the severe radiation environment (0.15-0.3 Gy/h in the barrel and 0.3-15 Gy/h in the endcap). A laser monitoring system tracks the evolution of light transmission with radiation, which affects crystal transparency.

The relative low light yield of $PbWO_4$ (~ 50 photons/MeV), also strongly temperature dependent (-2%/^{0}C), requires the use of photodetectors with internal gain.

In the central barrel region, with the magnetic field normal to the crystal axis, avalanche photodiodes (APD by Hamamatsu Photonics) operate with gain 50 and Q.E.~75% at $PbWO_4$ peak emission wavelength (420 nm). The stability of the gain, strongly dependent on bias voltage (3%/V) and on temperature (-2.2%/^{0}C), contributes to the resolution constant term, through intercalibration effects. Two APDs in parallel cover ~ 7% of the rear surface of each barrel crystal, resulting in a yield of 4.5 photoelectrons/MeV. In the endcaps, where higher radiation level forbids APDs, and the magnetic field is tilted by 8^0 to 26^0 with respect to the crystal axis, vacuum photo triodes (VPT) with gain 8-10 and Q.E. ~ 20% are used.

In order to minimize external noise contributions, much of the readout chain must be mounted within the detector. Severe constraints are imposed to the design. The high radiation environment of LHC requires high radiation tolerance by all components, which must be also insensitive to the 4 T magnetic field. To be able to control and stabilize temperature with a precision of 0.1 ^{0}C, due to the overall crystal light yield and APD gain dependence of ~5%/^{0}C, low power consumption is required for the readout chain (~2 W/channel) in order to reduce the thermal input to the system.

II. READOUT SYSTEM ARCHITECTURE

The desired ECAL performances require readout electronics with a demanding combination of wide dynamic range, good resolution, high speed and low power.

The photodetectors convert the light coming out from the crystals into an amplified current signal. Precise energy measurement over the very large dynamic range (90 dB), from 50 MeV to more than 1 TeV, corresponds to almost 16 bit accuracy in digitization. To achieve this resolution level, the architecture of the very front-end readout has been designed using multiple gain ranges.

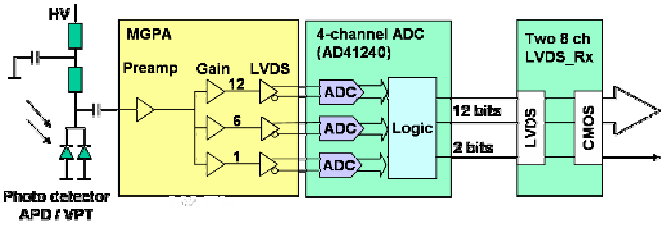

Figure 2: Very Front-End architecture

Inputs to the three, 12 bit ADCs are generated in parallel by three amplifiers (x1, x6, x12) with different gains, connected to the same detector signal (see Figure 2). By overlapping the input ranges of the three channels, this configuration allows to expand the dynamic range, keeping the same resolution and speed. The selection logic brings to the output bus the data from the first ADC that is not saturated. While a 40 MHz sampling is required to allow the fitting of the whole pulse as shaped in the preamplification stage, the input signal has a bandwidth of about 5 MHz.

The electronic noise must not exceed 50 MeV/channel, with a required LSB ~ 30 MeV. To be able to reject pile-up, with 40 MHz LHC bunch crossing , the peaking time must be ~ 45 ns. The energy reconstruction over the wide dynamic range requires a good linearity and pulse shape matching within and across gains, while the correlated noise and the cross talk must be minimized.

After digitization, the ADC output together with the information of the amplifier gain (14 bits) are stored into a pipeline waiting to be read from DAQ, on receipt of the Level 1 trigger accept. The data acquisition systems aims to be dead time free for a trigger rate up to 100 kHz.

On each group of 25 crystals, trigger primitives are generated (see the On-detector readout chain in Figure 3) and sent to the Off-detector Trigger Concentrator Card (TCC) at 40 MHz, using high speed optical links (800 Mb/s). After final calculation and synchronization of the trigger primitives, trigger data are sent to the Regional Trigger System. If the event passes the level 1 trigger, the Front End (FE) sends the crystal data to the Off-detector readout [3] (Figure 4) with another set of high speed optical links (800 Mb/s). The Data Concentrator Card (DCC), after verifying integrity, reduces data, then finally formats and transmits them to the CMS DAQ through an S-link 64. In the DAQ system, event size is limited to 2 kbytes, corresponding to a transmission data flow of 200 Mb/s. To obtain an average suppression factor of 20, DCC implements both a Zero Suppression and a Selective Readout method, using energy information thresholds on a 3x3 trigger tower matrix basis.

Bi-directional optical links at 40 Mb/s connect the On-detector system and the Off-detector Clock and Control System (CCS). Those links carry clock and control signals and the level 1 accept signal from Timing Trigger and Control (TTC) board and the Trigger Control System (TCS).

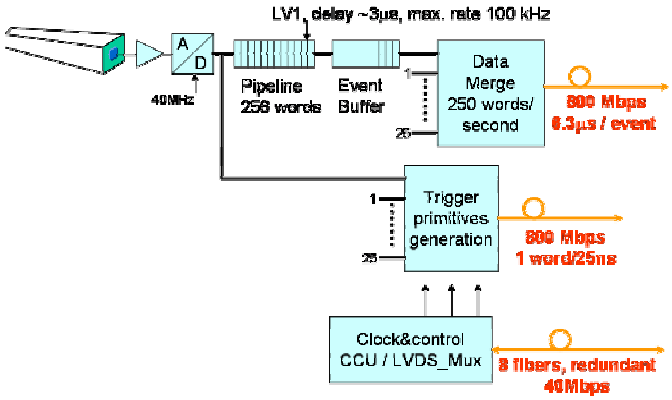

Figure 3: The On-detector readout schematics

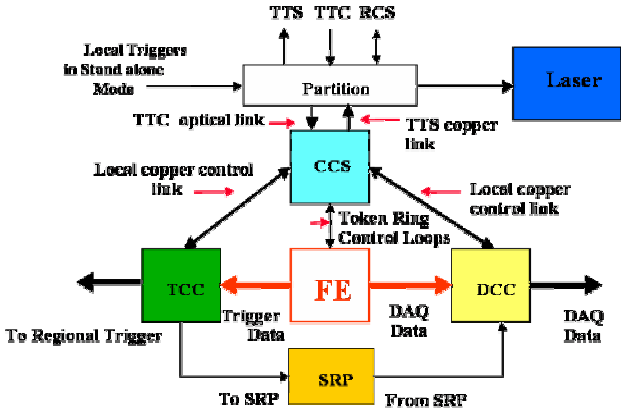

Figure 4: Off-detector electronics system

III. THE TRIGGER TOWER

For trigger purposes the crystals are organized in matrices of 5x5, forming a Trigger Tower (TT) in the barrel and a Super-Crystal in the endcaps. Therefore the basic element of the readout architecture is the 5x5 matrix, were 25 channels are read, digitized and stored into a pipeline to be transmitted to the DAQ at a Level 1 Trigger accept.

The barrel trigger tower, shown in Figure 5 consists of:

A. MB (Mother Board)

Placed on top of the crystal enclosure, one Mother Board distributes bias voltage (HV) to the photodetectors and low voltage from the LVR (Low Voltage Regulator) Board to the five VFE cards. Flexible kapton ribbon PCBs are used to connect the card to the 1700 crystals forming one of the 2x18 Super Modules (SM) of the barrel calorimeter.

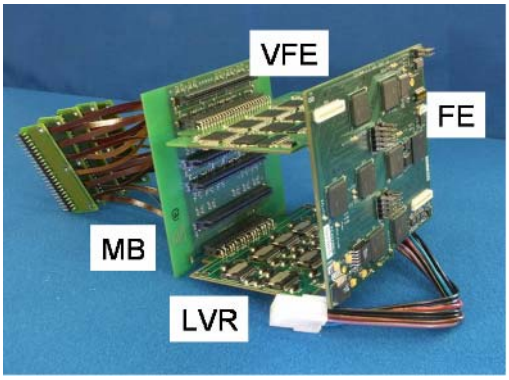

Figure 5: The barrel trigger tower

B. LVR (Low Voltage Regulator) Board

This card houses the 11 linear voltage regulators (ST LHC4913PDU) needed to supply the power to the complete front-end system. Three Detector Control Units monitor input and output voltages and the card temperature.

C. VFE (Very Front-End) Board

A VFE board houses five identical readout channels. Each channel consists of a Multi Gain Pre Amplifier (MGPA), an Analog to Digital Converter (AD41240) and a Buffer to adapt the low voltage differential signals (LVDS) outputs of the AD41240 to the single ended inputs of the FE board. The buffer also receives and distributes the 40 MHz LHC clock. A Detector Control Unit (DCU) measures the APD leakage currents, the crystal temperatures (one out of 10 carries a 100 kΩ thermistor with dR/dT = -4%) and the VFE temperature.

1) MGPA (Multi Gain Pre-Amplifier)

The MGPA [4] is a three gain channel amplifier matched to the noise and linearity requirements of CMS-ECAL. A choice of external feedback components to the first stage amplifier allows the chip to be used both for barrel and endcaps. It consists of a low noise pre-amplification stage (24 mV/pC), followed by three gain (1/6/12) channels where the signal is amplified and shaped (output pulse peaking time of ~ 50 ns). Power consumption is approximately 600 mW. Specifications are summarized in Table 1: linearity and pulse shape matching are demanding.

Table 1: MGPA Specifications

	Barrel	Endcap
Full scale signal	60 pC (1.7 TeV)	16 pC (3.5 TeV)
Noise level	10000e, 1.6 fC	3500e, 0.56 fC
Input capacitance	~ 200 pF	~ 50 pF
Gain ranges (tolerance)	1:6:12 (∓10%)	
Integral nonlinearity	< ± 0.1% full scale (each range)	
Pulse shape matching	< ± 1%(within and across ranges)	

An I^2C interface is used to programme the individual pedestal levels for each gain. A test pulse facility is included on the chip where charge magnitude is determined by a simple DAC.

2) ADC: AD41240

The AD41240 [5] is a CMOS, 4 channels, 12 bit 40 Ms/s ADC with low power consumption (150 mW/channel), designed for the needs of CMS ECAL. For low noise generation, the output data bus uses LVDS signalling. It is 14 bit wide: 2 bits indicating the selected channel and 12 bits for the value digitized by the corresponding ADC. Measured characteristics [7] are DNL=0.4 LSB, INL=0.7 LSB and ENOB=11 bit. At gain 12 the ADC LSB is 35 (71) MeV in the barrel (endcap). A digitally controlled hysteresis mode facilitate measurements of pulses extending over different ranges of amplitude: the tail of a pulse signal can be measured on the same range as the peak.

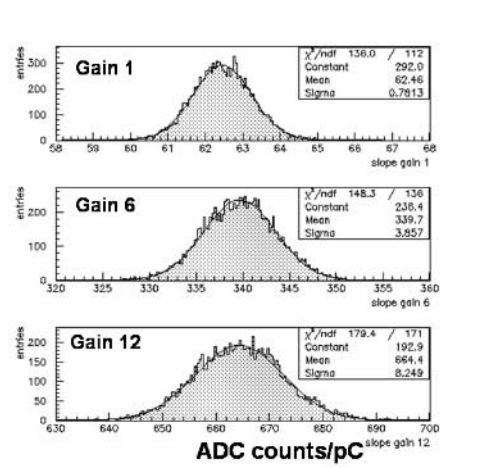

Figure 6: Measured slopes of 2500 VFE boards

To be able to reach the ECAL required performance and resolution VFE boards are carefully tested, after a power-on and a burn-in phase, in order to get a careful calibration of all the parameters over the full data ranges of the three gains. Different charges are injected for each gain with overlapping point to cross-calibrate.

Offsets and slopes (Figure 6), measured over a sample of 2500 boards, show a dispersion of ~ 1%, without any calibration. In Figure 7 the gain ratios show the good stability of the measurements over a six months period. Measured gain ratios are adequate.

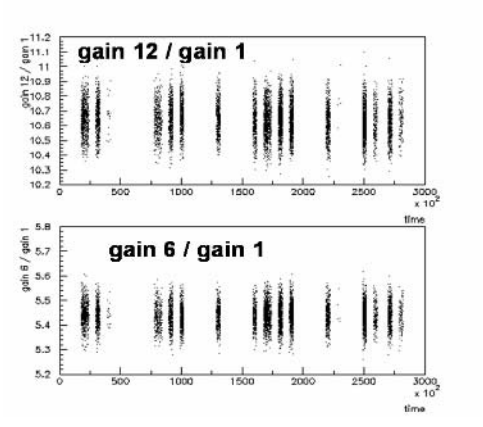

Figure 7: Gain stability over a 6 months period

Linearity, tested over a very wide range of input charges in the different gains, looks very good.

The pulse shape matching requirements is crucial for energy reconstruction over the wide dynamic range. Shapes (see for example Figure 8) are compared within the same gain for different charges or for different gains and show a distortion less than 1%.

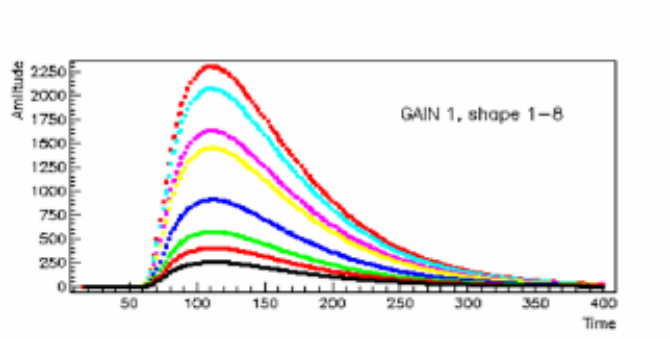

Figure 8: Pulse shapes: different charges at Gain 1

D. FE (Front-End) Board

The FE board, serving one trigger tower, houses the trigger primitives generation, the digital pipeline and the primary event buffers. This configuration requires a well developed clock and control link in order to transmit the level 1 trigger decision as well as the slow control for configuration. The data and the trigger outputs will be sent respectively to the off-detector system with two different 800 Mb/s optical links.

The data readout, received at 40 Mword/s from five VFE cards, is done in three steps. First, while calculating the trigger primitive, all data words are stored into a digital pipeline with programmable length to correspond to the level 1 latency. Second, when the level 1 trigger decision comes back through the TTC system and through the CCS, a time frame from every channel is transferred from the pipeline to the primary event buffer (capacity of 25 events with nominal time frame length of 10 samples). The data corresponding to a rejected bunch crossing are discarded. Third, as soon as the readout data link is available, data from each of the 25 channels, together an event identification and a trailer word are sent to the DCC.

1) FENIX (FrontEnd New Intermediate data eXtractor)

The ASIC [8], radiation tolerant and protected against Single Event Upset (SEU) with triple redundancy, contains the DSP for trigger primitive generation and the RAM for the digital pipeline and the primary event buffer. Seven FENIX chips are arranged on the FE card as in Figure 9. Each of the five FENIX in STRIP mode reads the five channels of a VFE card, calculates the filtered strip sum of the five calibrated channels for the trigger primitive generation. They also contain the pipeline and the primary event buffers for five channels. The FENIX chip in Trigger Primitive Generation (TPG) finalises the process for one trigger tower. TCP requires absolute calibration of each channel. The FENIX chip in DAQ mode controls the readout of the five FENIX STRIP and encapsulates the event. A forth mode, MEM, is used to read out the ADCs monitoring the laser injection system.

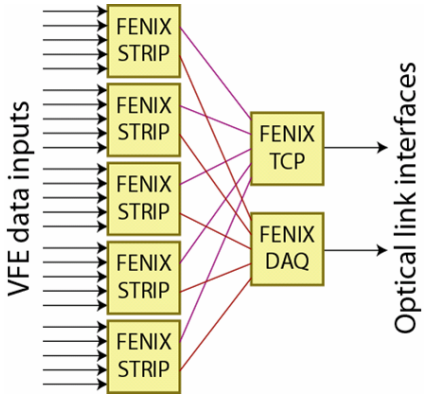

Figure 9: FENIX operation modes on a FE card

2) GOH (Gigabit Optical Hybrid)

The FE hosts two GOH boards, each implementing a data link transmitter, including serializer (Gigabit Optical Link GOL) and a laser diode.

3) CCU (Communication and Control Unit)

The CCU25, developed for the CMS silicon tracker, performs the clock distribution and control of the system. Each CCU contains various types of peripheral controllers and has dual network input and output ports allowing the cabling of a redundant network.

E. Token ring Board

In a SM there are 8 Token Ring bus linking 8 (or 10) FE to provide the clock and trigger information. A double ring system allows to by-pass a deficient board, conserving a closed ring bus. This data link is synchronized to the LHC clock frequency and has raw capacity of 40 Mbit/s.

Off-detector a Front-End Controller (FEC), part of the Clock and Control System (CCS), is the master of the network.

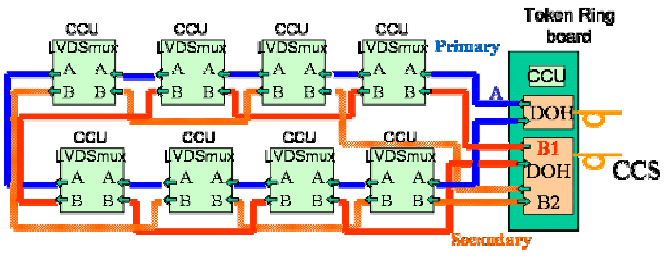

Figure 10: Token Ring System

All ASICs were manufactured in 0.25 µm CMOS IBM process, radiation hard [9], using a single 2.5 V supply, with low power consumption. Other advantages were the high yield and cheaper mass production, together with short turnaround for design revisions.

IV. CONCLUSIONS

All ASICs (MGPA, AD41240, FENIX and service chips) were produced and tested with high yields (> 80%).

All Front-End Boards are under construction and test, ready for the integration.

From data stored in the construction database on crystal light yield, APDs and electronics gains, a first calibration of the Super Modules can be obtained. Since the overall ECAL inter-calibration is of the order of 3-4%, the electronics contribution of the order of 1% should be negligible.

A full SuperModule was exposed in 2004 to different electron beam energies (20-250 GeV). Figure 11 shows a preliminary measurement of the resolution as a function of beam energy for a 3x3 crystal matrix, with a uniform beam impact point.

The values of the resolution parameters, obtained in the fit, are within the required ECAL specifications.

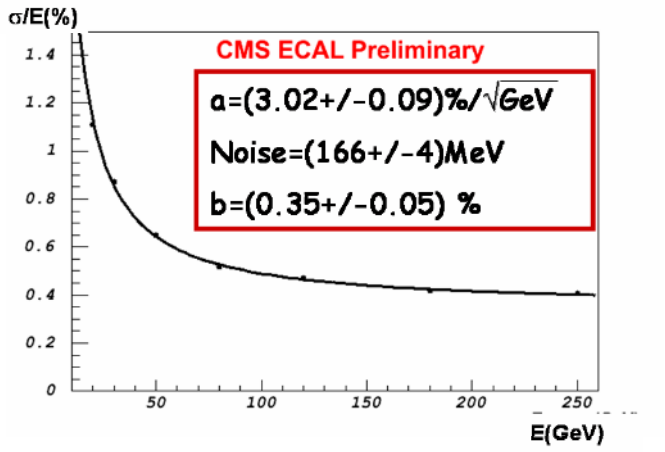

Figure 11: Preliminary results on energy resolution (electron beam)

Beam tests have given very encouraging indications that the ECAL ambitious design goals can be met.

V. REFERENCES

[1] "**The Compact Muon Solenoid (CMS)**", Technical Proposal, CERN/LHCC 94-38, LHCC/P1, 1994.

[2] "**The Electromagnetic Calorimeter Project Technical Design Report**", CMS Collaboration, CERN/LHCC 97-33, CMS TDR 4, 15 Dec. 1997.

[3] "**CMS ECAL Off-detector Elecronics**", R. Alemany et al., Proceedings of the 11th Inter. Conf. on Calorimetry in HEP, CALOR 2004, Perugia Mar 29-Apr 2, 2004.

[4] "**Low Voltage Supply System for the Very Front End Readout Electronics of the CMS Electromagnetic Calorimeter**", B. Betev et al., Proceedings of the 9th Workshop on Electronics for the LHC Experiments, Amsterdam Sept 29 - Oct. 3, 2003.

[5] "**The MGPA Electromagnetic Calorimeter Readout Chip for CMS** ", M. Raymond et al., Proceedings of the 9th Workshop on Electronics for the LHC Experiments, Amsterdam Sept 29 - Oct. 3, 2003; IEEE, Rome Oct. 16-22, 2004.

[6] "**A CMOS low power, quad channel, 12 bit, 40 Ms/s pipelined ADC for application in particle physics calorimetry** ", G. Minderico et al., Proceedings of the 9th Workshop on Electronics for the LHC Experiments, CERN-LHCC-2003-055, 2003.

[7] "**Charaterization and production testing of a quad 12 bit 40 Ms/s A/D converter with automatic digital range selection for calorimetry** ", K. Kloukinas et al., Proceedings of 11th Work. on Electronics for the LHC and Future Experiments, Heidelberg Sept. 12-16, 2005

[8] "**The New Read Out Architecture for the CMS ECAL**", M. Hansen, Proceedings of the 9th Work. on Electronics for the LHC Experiments, CERN-LHCC-2003-041.

[9] "**Total Dose Irradiation of a 0.25 μm process**",E. Noah et al., Proceedings of the 6th Workshop on Electronics for the LHC Experiments, CERN-LHCC-2000-041, 2000.