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The Front-End Electronics System for the CMS Electromagnetic Calorimeter

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CMS designed an high precision electromagnetic calorimeter, to be operated reliably in the high radiation environment of the CERN Large Hadron Collider (LHC), inside the 4 T magnetic field. Innovative solutions were developed to place the front-end electronics within the detector with the advantage of minimizing external noise, while reducing the number of optical links to send data to the off-detector readout. The final system architecture will be reviewed in detail.High resolution, over the wide energy dynamic range, was obtained with studies in an electron test beam.

Summary

The general purpose Compact Muon Solenoid (CMS) experiment is now well into the construction of its very high performance, homogeneous electromagnetic calorimeter (ECAL), made of about 76000 lead tungstate scintillating crystals(36 super-modules of the barrel and eight quadrants of the endcaps).
The low light yield (˜ 50 photons/MeV) requires photodetectors with internal gains, while the strong temperature dependence both of the crystal response and of the photodetectors (1/LY dLY/dt ˜ -5%/C), imposes to control and stabilize the detector temperature with high precision (< 0.1 C).To achieve the best energy resolution measuring electrons and photons, over a wide energy range (˜100 MeV to ˜1.5 TeV), the contributions by fluctuations of shower development, by instrumental and calibration limits must be minimized. To cut down external noise, much of the readout electronics has been mounted within the detector, with severe constraints on radiation hardness, high speed (40 MHz), wide dynamic range (90dB). The system architecture of the readout electronics was revised and heavily changed during the past two years. The trigger primitive generation, the digital pipeline, and the primary event buffers are implemented in the front-end, reducing by an order of magnitude the number of optical data links to carry data off the detector. Full custom-integrated circuits were developed in 0.25 um CMOS technology, intrinsecally radiation hard, using a single 2.5 V supply and a low power consumption (< 3 W/channel). A Multi-Gain PreAmplifier (MGPA - 3 gains 1:6:12) amplifies each photodetector signal as the input of a 12 bit multi-channel ADC. The output of the ADC corresponding to the highest unsaturated gain, together with the information of the amplifier gain, is stored in a pipeline before the Level 1 accept signal allows it to be read from the DAQ. The basic element of the on-detector architecture is the 5x5 crystals Trigger Tower, where 25 channels are read, amplified, digitized and stored into the pipeline of the FENIX (Front-End New Intermediate data eXtractor)ASIC chips. A Mother Board distributes HV to the photodetectors, and LV from the LVRB (Low Voltage Regulator Board) to the five VFE (Very Front-End) boards. Each VFE, containing five MGPA and five ADCs, receives the signals from a row of five crystals to be shaped and digitized, while reading photodetectors'leakage currents and crystal temperature using a Detector Control Unit (DCU). A FE (Front-End) board with seven FENIX chips stores and processes the digitized data during the Level 1 trigger latency of 3 us. Both trigger data and digitized data from the triggered event are transmitted to the off-detector electronics, the so called Upper Level Readout (ULR), through serial digital 800 Mb/s data links.A well developed clock and control link transmits the Level 1 trigger decision as well as slow control for configuration. A full barrel supermodule with the final on-detector electronics has been tested on an electron

beam to measure the front-end electronics performance.

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