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THE ALICE CENTRAL TRIGGER PROCESSOR SYSTEM

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The Alice Central Trigger Processor is described. The current trigger concept was introduced in 2001 and allows up to 50 trigger inputs at three different levels: level 0 (24 inputs, 1.2 μs latency); level 1 (20 inputs, 6.5 μs latency); level 2 (6 inputs, 88 μs latency). Up to 50 trigger classes (where inputs and destination detectors are specified) can be used simultaneously. Detailed designs became available in 2005.

The trigger system is implemented using seven types of 6U VME boards. Six types make up the CTP itself; the seventh, the LTU, provides the detector interface and can also be used as a trigger generator.

Summary

The ALICE Central Trigger processor and its requirements have been in development over a period of about ten years. The present trigger concept dates from 2001.

ALICE expects to take data in a number of different running configurations, using various ion-ion beams and also using pp collisions, the latter at a significantly lower luminosity than the other LHC experiments. The principal design aim for the experiment has been to choose detectors that allow the measurement of very high multiplicities (up to 8 000 tracks in the main detector), and this has led us to a set of detectors with somewhat inhomogeneous intervals for detection and readout of signals. These range from a large Time Projection Chamber (TPC), which is sensitive
for a period of 88 μs and which reads out throughout this interval, to triggering detectors (T0 and V0) sampling forward multiplicities, which are able to resolve a single bunch crossing. The ALICE trigger addresses these problems by implementing partitioning of the detector, so each partition has an independent dead time, and through the imposition of a “past-future protection”interval, related to the sensitive time of the detectors, during which only a programmable restricted number of additional collisions can take place.
The trigger handles combinations of up to 50 trigger inputs and runs up to 50 triggers in parallel; these are mediated through the trigger class, a trigger specification combining trigger inputs, trigger output detectors (the detector cluster) past-future protection requirements and certain other flags.

The Central Trigger Processor (CTP) is implemented using 6 different types of 6U VME board, together making up eleven active boards for the CTP. In addition, for each detector there is a Local Trigger Unit (LTU) which receives trigger information for the specific detector from the CTP and provides the interface to the detector, where appropriate through the RD-12 TTC system. The LTU can also be used in standalone mode as a generator of simulated trigger signals. The LTU boards for ALICE have now been produced, and the production of CTP boards will have been completed by the end of September 2005.

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