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Tilecal ROD final system. Design, performance, production and tests

The Tilecal Read Out System (ROD) must be able to receive the calorimeter data filtered by the first level trigger, process them, and send them to the ATLAS generaldata acquisition system (TDAQ), where the level 2 trigger decision will be taken.Therefore the ROD is placed between level 1 and 2 trigger levels.

The ROD will process in real time the discrete samples of each calorimeter channel (˜10000 total channels) in order to reconstruct from such digital information the following physics parameters:
1)The total Energy of a Calorimeter cell (scintillators + photomultipliers channel),
2)The phase shift (time of signal arrival)
3)Fit quality factor (chi2)
4)Send raw sampled data for later deep analysis in case of pile-up, etc ⋯

Summary

All these processed data will help to understand physics in ATLAS Hadronic calorimeter and to take the level 2 trigger decision where information from all ATLAS Sub-detectors will be correlated. Besides, there is a level 3 trigger of bigger granularity that helps to filter the huge amount of event data generated in ATLAS with a p-p bunch crossing of 25ns in LHC.

The TileCal data acquisition system is divided in 4 readout partitions. A partition is built around a ROD crate with at least 10 modules mounted in it: 1 ROD controller, 1 Trigger and Busy Module and 8 ROD modules (1 ROD Motherboard + 2 DSP Processing Units + 2 S-link HOLA LSC). With this architecture there will be 32 RODs to feed 64 ROBs. With this 1:2 mapping, two optical links (S-Link HOLA LSC) are mounted per ROD to compensate the number of ROBin´s and to fulfill the TileCal dataflow needs.

ROD motherboard based on the ROD final production board from the LiArg sub-detector is the final hardware solution to work at a 100 KHz Level 1 trigger rate with digital signal processing capabilities and input/output optical links. The differences between both RODs are mainly at the input stage of the board and related to the data clock frequency and transmission protocol. There is minor hardware design modifications proposed to keep the same PCB layout and to do a common production, but large modifications related with the input stage and PU firmware. These modifications were proposed to be implemented in the second batch of final ROD prototypes and validated in the two units received for TileCal from the prototype series production.
The design of the Firmware for FPGAs (VHDL) and DSPs (C, ASM), and the Software for ROD library, XTestROD (GUI Interface for debugging) and Online Software for production tests (C++, java) was developed by the Valencia-Tilecal Group. Therefore, all the firmware, online/offline software, and the Hardware is ready to test the full production boards from May to September 2005 in the laboratory and later to install the system in the pit (USA15) during the Tilecal –ATLAS commissioning phase. The Hardware and Software system was also validated in past ATLAS Combined Testbeam 2004 with successful results in terms of management, stability and performance.

Author: Mr CASTELO, Jose Maria (Instituto de Fisica Corpuscular (IFIC) UV-CSIC)

Presenter: Mr CASTELO, Jose Maria (Instituto de Fisica Corpuscular (IFIC) UV-CSIC)