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Advanced Front End Signal Processing Electronics for ATLAS CSC System: Status and post production performance.

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The ATLAS muon spectrometer will employ Cathode Strip Chambers (CSC) to measure high momentum muons in the extreme forward regions [1]. Preamplification of the charge on the strips is performed in the Amplifier Shaper Module I. Amplifier Shaper Module II performs the analog buffering, digitization of the charge signals from individual cathode strips and multiplexes the data into two fiber optics links running at 1 Gbps each. We present the design architecture of the complete front end electronics chain and its performance. We also report on the production and testing status of overall on detector electronics.

Summary

I. Introduction:
Cathode Strip Chambers (CSC) form the first station of the endcap muon spectrometer in the ATLAS experiment. The CSC system consists of 32 four-layer readout planes of 192 x- and four-layer readout planes of 48 y-strips each. Each CSC is served by 5 front end electronics packs called Amplifier Shaper Module Packs (ASM-Pack), which consist of two ASM-I and one ASM-II printed circuit boards (PCB). ASM-Pack together employs 4 different custom designed Application Specific Integrated Circuits (ASIC) fabricated using Agilent Technology (AT) 0.5 μm CMOS, Single Poly, Linear Capacitor, Triple metal process, along with a switched-capacitor array analog memory [2] in a radiation-hardened 0.8⊠m CMOS process and various COTS components. Both PCBs use radiation hard electronic circuits consistent with the ATLAS radiation policies.

II. ASM-I
A CMOS multi-channel ASIC was developed for charge amplification and signal shaping. Bipolar shaping and 70 ns shaping time were chosen to minimize the effects of noise and pileup. In the 25-channel Preamplifier/Shaper, the NMOS input FET of the preamplifiers, DC feedback circuit and pole-zero compensation circuits were optimized to provide lower parallel and series noise to the front-end signal chain, staying within the allocated power budget [1].
Each ASM-I consists of 4 of the above mentioned ASICs processing signals from 96 cathode strips and its output is AC coupled into ASM-II for analog storage, digitization and transmission to off-detector ReadOut Driver (ROD)[3]. The ASM-I also consists of CERN developed LHC-7913 voltage regulator from ST microelectronics and three stages of Electro-Static Discharge (ESD) protection for each channel.

III. ASM-II
ASM-II serves total of 192 channels from two ASM-I. For analog storage, the HAMAC Switched Capacitor Array (SCA) ASIC [2] is used. This chip originally developed for the ATLAS liquid argon calorimeter, has a separate “muon”mode which allows it to function as a 12-channel, single gain memory rather than the 4-channel, tri-gain mode used in the calorimeter. SCA cells are written at 20 MHz and read-out upon level 1 trigger to a 12 bit Analog to Digital Converter (ADC) AD9042 at 6.67 MHz. ASM2MUX, a digital multiplexer ASIC, converts 24 bits from two ADCs at 6.67 MHz into 4 bits out at 40 MHz. Control signals and clocks for SCAs and ADCs are distributed through MC10H116 Positive Emitter Coupled Logic (PECL) buffers, differentially to keep digital noise to a minimum. Custom clock fan-out ASIC is used to distribute clocks to ASM2MUXs and on board Giga bit optical links (G-Link). Seven LHC-7913 voltage regulators on ASM-II distribute power to ASM-I and ASM-II. The data from the chambers are transmitted to and control signals for readout of the board are received from off detector ROD over G-Links, consisting of AT HDMP-

1022, AT HDMP-1024 and SDX-19-4-1-S optical transceivers. Sparsification, event building, and other tasks involved in resolving the hit co-ordinates with a resolution of approximately 60 μm are performed on the ROD [3]. The RODs are also responsible for generating the fast clock and control signals and distributing them to the ASMs, which function as slaves.

IV. Status:
Production of the front end electronics for the ATLAS CSCs is nearing completion. Post production results will be available at the time of the conference.

[1] P. O'Connor "Readout Electronics for a High-rate CSC Detector"Proceedings of the 5th Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA 20 - 24 September 1999
[2] D. Breton et al., "HAMAC, a rad-hard high dynamic range analog memory for ATLAS calorimetry", PROCEEDINGS of the Sixth Workshop on Electronics for LHC Experiments Krakow, Poland, 11 - 15 September 2000; P. O'Connor "Adapting the Liquid Argon Calorimeter SCA for use with CSC BNL"2-Feb-99: http://atlas-csc.inst.bnl.gov/Adapting_LAr.pdf
[3] I. Gough Eschrich "Readout Electronics of the ATLAS Muon Cathode Strip Chambers". In press.

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