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Test Station for the LHCb Muon Front-End Boards

This document describes hardware and software of a station developed to test the LHCb Muon Front-End Boards (FEBs) for MWPC and GEM chambers. Such boards are made up of two Amplifier, Shaper and Discriminator (ASD) ASICs and a read-out and control ASIC, accessible via I2C based data transfer protocol. Such station allows bench tests of front-end readout circuitry using the same facilities which will be used for their supervision, more a charge injection and a custom read-out boards, and a Win API C program (to control and analysis data), achieving a user friendly system which will be utilized in the course of chambers and readout electronics tests. The main parameters to be considered are: data transfer operation, board connectivity, sensitivity, offset, and noise. A brief summary of the first results obtained during its development and implementation is also featured.

Summary

The LHCb Muon System will be made up of 7500 16-channel Front-end Boards (FEBs), each hosting 2 Amplifier-Shaper-Discriminator (ASD) ASICs, called CARIOCA (Cern And RIO Current-mode Amplifier), and a supervisor ASIC (DIALOG, DIagnostics, time Adjustment and LOGics). On a FEB, called CARDIAC (CARioca and DIAlog Connection), two CARIOCAs are managed by a DIALOG, which is also the first recipient of the channels output by CARIOCA, in the readout chain. The LHCb Muon chambers and circuits are currently entering the production stage and most of their testing procedures require usage of FEBs. The system described has been developed to test and measure the FEB characteristics in a stand-alone setup, to allow a flexible adjustment of their parameters during an on-chamber characterization. Possible future improvements include: a database of FEBs characteristics and an on-site testing facility, both for control purposes.

The system allows testing, measurement and diagnostics of several FEB parameters by means of charge injection, alternative FPGA based read-out equipment, I2C data transfer and signal analysis. Various algorithms have been implemented to perform a thorough test of the readout apparatus: connectivity, register access, offset, noise, sensitivity. A noise rate-versus-threshold algorithm (rate-method) is being evaluated, as a solution to verify the ASD response in the field; this last test is going to be implemented in the FE Control System where it should undergo verification.

The main building blocks of the set presented are 4 boards and a Win32 API to a C program. Data transfer is ensured by CANopen and I2C protocols. The CANopen protocol is handled by a commercially available Kvaser PCI adaptor while a VME 6U module (Service Board, SB) implements the I2C protocol. A SB relies mainly on 4 replicas of a module called ELMB (Embedded Local Monitor Board, based on Atmega128 microcontroller) and a Flash Memory based FPGA by Actel. A different card, accessible via I2C, has been implemented to inject charge in the range of a few fC (Injection Board) into the ASD, and finally, a board based on the same FPGA as the SB is used to read the signals generated by the FEBs under test (Counting Board).

The Injection Board contains 16 channels and its circuitry permits to set the injected charge by means of writing into its DAC registers, to mask out some chosen channels, to adjust injection rate and to inject either positive or negative charge. A Counting Board receives differential signals from the FEBs and processes data by means of counters and it transfers data using a simple I2C implementation.

This test station can test either kind of FEBs, on MWP and GEM chambers in the LHCb Muon subdetector and the first prototype has been manufactured and characterized. We present here its circuitry and results to show its implemented features and discuss its future possibilities.

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