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Full custom Quad Ported Memory

The Quad Ported Memory (QPM) is the data memory for the four MIMD CPUs in the TRAP Chip. Which is part of the trigger system for the ALICE Transition Radiation Detector (TRD).
The QPM has 1024 data words each data word consists of 39 bits (32 data bits, plus 7 hamming bits) and is quad ported - each CPU can access the memory, reading or writing completely independent of the CPUS, which are connected to its other ports. It operates with 120 MHz and needs 0.58 mm2 area on the chip. It's implemented in a 0.18 µm CMOS process with six metal layers. The VDD voltage is 1.8 V and the power consumption is for all four ports working 39,6 mW and for no ports active 0,02 mW. The multiport architecture eliminates global busses and arbitration required for memory access, while saving area and power.

Summary

The Quad Ported Memory (QPM) is the data memory in the TRAP Chip.
The TRAP chip is a part of the ALICE Transition Radiation Detector (TRD). The TRD operates as trigger and tracking detector in the ALICE experiment. Therefore there are nearly 1.2 million analog data channels which are digitized at 10 MHz by 10 Bit ADCs within 2 µs. On this Data stream of 13 TByte/s a trigger decision has to be made within 6 µs. In the Trap Chip the pre-amplified analog data are digitized and digital filtered and preprocessed. Each TRAP Chip handles 18 channels plus 3 neighboring channels. In a second stage the TRAP chip performs a straight line fit on a subset of the data. Each Chip has four MIMD CPUs to compute four straight line fits in parallel. The QPM is the data memory for the four MIMD CPUs. The results of the straight line fit (called tracklet) are shipped to the Global Tracking Unit (GTU) which merges tracklets and gives the final trigger decision. 64224 Trap Chips will be used and integrated in the TRD.
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The QPM consists of bit-cells, address decoders, write units, read units and the control logic.
The bit-cells are based on a normal six transistor SRAM bit-cell, but to allow multiple accesses the normal two pass transistors are supplemented with another 6 pass-transistor. So that each of the four ports has two pass-transistors. Also the size of the inner transistors is increased to ensure that the cell is strong enough to cope with all four ports simultaneously. The bit-cells are arranged in 128 rows and 312 columns. In each case 8 columns are combined and represent one of the 39 bits in the read or write data. This happens to save area and to get a better aspect ratio.
Each of the four ports has an independent address decoder. In every address decoder the higher 3 bits of the address selects one of the 8 columns and connect them to the write or read unit via analog multiplexers. The other 7 address bits select one of the 128 rows, by enabling the pass-transistors of the addressed bit-cells.
For each word bit there are four write units (one per port), which can overwrite the addressed bit-cells with the write data.

The read unit detects the stored value in the addressed bit-cells.
This is done in two steps. First the read unit is precharged, so that there is a good balance in the read unit.
Then the pass-transistors of the addressed bit-cells are enabled. Depending on the stored value they disturb the balance in one of two possible directions. A latching amplifier detects this unbalance, amplifies it and latches it until the next precharging.
Via amplifier buffers this values is given to the data-outputs and represent the read data. There are as many read units as writ units.
A single control unit controls the timing of addressing, writing,and reading. It contains two programmable delays, to cope with process variations.
The test results will be presented at the Workshop.

Author: Mr REICHLING, Christian (Kirchhoff Institut für Physik)

Co-author: Prof. LINDENSTRUTH, Volker (Kirchhoff Institut für Physik)

Presenter: Mr REICHLING, Christian (Kirchhoff Institut für Physik)

Track Classification: Custom Integrated Circuits