Contribution ID: 92

The Readout, Fast Control and Powering Architecture for the CMS Preshower

Thursday 15 September 2005 15:15 (25 minutes)

The CMS Preshower detector (ES) comprises ondetector and offdetector components of the readout and control system, as well as the powering system and optical links. The fast control system is largely built around the one originally conceived for the CMS Tracker (FEC, DOH, CCU etc.) whilst the readout part profits from developments made for the CMS ECAL (DCC, GOH, AD41240). There are two ESspecific ASICs: PACE3 (frontend preamp/ shaper/analogue memory) and Kchip (data concentrator). Two custom ondetector PCBs have also been developed: the frontend hybrid (containing the PACE) and the system motherboard (containing all power regulators, digital chips, optical components and ADCs). The full architecture is presented, along with results from system tests.

Summary

The CMS silicon Preshower is a fine grain detector placed in front of the endcap Electromagnetic calorimeter. Its primary function is to detect photons with good spatial resolution in order to perform pi0 rejection. The detector comprises around 4300 silicon sensors, each measuring 6.3cm x 6.3cm divided into 32 strips, with strip

capacitance in the region of 50 pF. Each sensor is attached to a single PACE3 frontend ASIC, which performs amplification and shaping of the signals from the silicon, followed by voltage sampling into an onchip analogue pipeline memory 192 cells deep. Upon reception of a first level trigger the analogue signals are multiplexed out of the PACE3 to a 12bit 40MHz ADC (AD41240). The Kchip ASIC then takes the digitized data from up to 4 PACE3, reformats the data and transmits them to

the offdetector readout boards (ESDCC) via Gigabit Optical Hybrids (GOH). The PACE3 is situated on a PCB bonded to a silicon sensor mounted on a ceramic support and an aluminium tile (to allow overlapping in one direction of adjacent sensors) to form a micromodule . This PCB also contains a DCU chip for calibration of the PACE3, and connects to the System MotherBoard (SMB) via an embedded polyimide cable. Four types of SMB are used, connecting to 7, 8 or 10 PACE3. The SMBs contain the ADCs, Kchips and GOH boards, as well as a set of control chips the CCU, LVDSmux4P, PLL, QPLL, DCU, LVDSbuf used for setup of the ASICs and distribution of the fast timing signals (clock, trigger). Up to 12 SMBs are connected together via polyimide cables to form control rings . Each ring communicates with the offdetector VME modules (Clock and Control System CCS) via Digital Optical Hybrids (DOH) placed on two adjacent SMBs (for redundancy purposes). The low voltage is supplied to the system by CAEN Easy3000

series modules through voltage regulators situated on the SMBs. Each SMB contains a control regulator (CR) for supplying the control chips, and a group of readout regulators (RR) for the PACE3, ADCs, DCUs, Kchips and GOHs. The CAEN system can control the CRs and groups of RRs to allow the switching on/off of relatively small units within the ES whilst still maintaining the integrity of the control rings whenever possible. The micromodules are connected to the large ES lead absorber plates. The possibilities of commonmode pickup by these plates, as well as the possibilities of return current flow through them, have necessitated a precise grounding and shielding scheme. With exception of the ESDCC, which is still in the development phase, all components of the ES electronics system have been prototyped and most are in full production. System tests have been performed with excellent

Author: Mr BIALAS, Wojciech (CERN)

Co-authors: PEISERT, Anna (CERN); GO, Apollo (NCU, Taiwan); BARNEY, David (CERN); LOUKAS, Dimitrios (NCSR Demokritos, Athens, Greece); ARTECHE, Fernando (CERN); SHIU, Jing-Ge (NTU, Taipei, Taiwan); UENO, Koji (NTU, Taipei, Taiwan); KLOUKINAS, Kostas (CERN); MANTHOS, Nikos (University of Ioannina, Ioannina, Greece); VICHOUDIS, Paschalis (CERN); ASPELL, Paul (CERN); WERTELSERS, Piet (CERN); REYNAUD, Serge (CERN); FUNK, Wolfgang (CERN); HSIUNG, Yee (NTU, Taipei, Taiwan); BEAUMONT, Yves (CERN); GAO, Zhengwei (CERN)

Presenter: Mr BIALAS, Wojciech (CERN)

Session Classification: Parallel session A5