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Test Station for the CARIOCA FE-chip of the LHCb Muon Detector

This document describes the hardware and software of a Front-End Electronics Test (FEET) Station developed to test and characterize the LHCb Muon Front-End (FE) ASIC, which processes the signals generated by Multi-wire proportional chambers and GEM detectors. The CARIOCA (Cern And Rio Current-mode amplifier) is an 8-channel Amplifier, Shaper and Discriminator with Base Line Restoration (ASDB). It has entered production phase during the current year. A total of approximately 20000 chips will be produced and they will require individual testing, before final assembly on Printed Circuit Boards (PCB). The ASIC design is fully customized for the LHCb muon chambers and, besides, it is almost entirely analog, what raises difficulties to the adoption of commercial test systems. CBPF has proposed and eveloped a test bench
with the following features: variable and bipolar charge injection, custom read-out, rate and time measuring circuitry, power consumption control and a LabVIEW management program. This system detects open or dead channels as well as short circuits, and measures noise, sensitivity, and the time width of the LVDS output signal. Results for the first thousand chips measured are also shown.

Summary

The LHCb Muon Group has developed the CMOS ASIC CARIOCA to readout its Multiwire Proportional Chambers (MWPC) and GEM detectors, using the radiation hard IBM 0.25um process. Each ASIC holds 8 identical current-mode ASDB channels with individual input thresholds. The Muon detector contains around 120000 physical channels, requiring production of 20000 front-end chips, roughly. CARIOCA has been developed to process MWPC cathode and anode signals (positive and negative charges) and two different versions have been implemented to overcome the requirement of MWPC and GEM detectors operation. The test station has been devised to accomplish bipolar tests and to measure characteristics of both CARIOCA versions. All tests should be carried out before chips are soldered to PCBs in order to minimize potential over-costs related to loss of time and rework activities if a significant proportion of FE boards is found to be defective. Each PCB will have on board two CARIOCAs and another (digital)ASIC developed to receive the 16 channels generated by the two amplifiers.

The current test station permits users to perform measurements, run diagnostics, to acquire statistical data of all important ASDB parameters using several techniques, which will be shown in depth. Various algorithms have been implemented to achieve a systematic test procedure for the detector read-out apparatus. The parameters under test are: power consumption, channel response, offset, sensitivity, time-walk and pulse width.

The main building blocks of FEET are a charge injector, a read-out and counting device, a Time to Digital Converter (TDC) custom circuit, a National Instruments data acquisition (NI-DAQ) PCI board and an integrated LabVIEW program. The Injection Board (IB) contains 8 channels and its circuitry permits a fine tuning of injected charge (in the range of few fC) and of ASD threshold values, it can also mask out any chosen group of channels, control the injection rate and finally inject either positive or negative charge as required. A Counting Board receives differential signals from the ASIC under test and processes data by means of 8 individual counters (all synchronized to IB signals); it transfers data to a local computer via the NI-DAQ board and its functionalities are based mainly on a Xilinx FPGA implementation. The custom TDC module uses a commercial IC to digitalize the time of the CARIOCA input and ouput pulse transitions, allowing the measurement of the CARIOCA response time and output pulse width with a resolution as low as 120ps;

data transfer is carried out via parallel port EPP standard.

This testing station, with its development approaching completion, has suggested and put into evidence parameters to be looked into with more accuracy, and served also to establish procedures for a practical implementation of an easy to use bench station.
Tests of chips from the non recursive engineering run are under way, and will provide the parameters for rejection of the chips from the production run.
Circuitry, algorithms and statistics results will be presented.

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