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Mass production testing of front-end ASICs for ALICE SDD system

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This paper presents the wafer-level testing system developed for the front-end electronics of the Silicon Drift Detectors of ALICE. The system is based on a semiautomatic probe station and has been designed to test two different ASICs with minimal changes in the hardware. All the operations are controlled by a PC running a dedicated LabView software. The architecture of the test system is described and the results obtained in the mass production test are discussed.

Summary

The front-end electronics of the Silicon Drift Detectors (SDDs) of ALICE is based on two custom integrated circuits: PASCAL (Preamplifier Analog Storage and Conversion from Analog to digitaL) and AMBRA (A Multievent Buffer Readout Architecture). PASCAL is a mixed-mode integrated circuit that samples the signals coming from the detector and digitizes them when a trigger signal is received. AMBRA is basically a RAM that allows the derandomization of the trigger. This chip performs also some digital signal pre-processing, like baseline equalization and 10-to-8bit compression. Both ASICs have been designed and produced in 0.25 um CMOS technology. For cost reasons the two chips have been fabricated using the same set of masks. Each 8-inch wafer hosts 146 PASCAL and 146 AMBRA. This paper describes the test system developed for the on-wafer testing and discusses the results obtained.

The test system is based on a Cascade Microtech Rel-6100 probe station with a motorized chuck stage controlled via GPIB interface. It is required to use two different full custom active probe cards for the two ASICs. Each probe card contains custom to standard differential digital buffers.

To reduce as much as possible hardware dependence, the digital control signals are generated by a data pattern generator (Agilent 16702B Logic Analysis System); the outputs are read out by the logic state analyzer (on the same instrument) and then sent to a PC for data analysis. For AMBRA, which is a pure digital IC, it is possible to implement data analysis directly on the logic state analyzer. The data produced by PASCAL are digitized analog signals and a more complex statistical analysis isrequired for an adequate assessment of the performance. In this case the raw data are sent to a PC. The computer performs online a complete data analysis evaluating the critical parameters (gain, linearity, number of dead channels, ADC and DAC performance, etc.).

The whole test system is controlled by a PC running a software developed in LabView. The program allows to drive the test hardware (probe station and power supplies via GPIB, data pattern generator and logic state analyzer via TCP/IP and all support electronics), to control all test steps and to create report files for the database in a friendly windows-based user interface.

The mass production testing system is installed at the INFN in Rome. The typical testing time is 8 minutes for PASCAL and 5 minutes for AMBRA. The architecture of the test system, the test selection criteria and the test results will be discussed in detail in the final paper.

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