Contribution ID: **42** Type: **Oral**

The VMEbus processor hardware and software infrastructure in ATLAS

Thursday 15 September 2005 11:25 (25 minutes)

Most of the off-detector custom electronics of the ATLAS data acquisition system such as the Read-Out Drivers or the Trigger and Timing Control system has been implemented in VMEbus. The paper describes the process of selecting a common VMEbus processor module for all VMEbus systems in ATLAS and the problems encountered during the evaluation of different candidate cards. Some performance figures for VMEbus transfers are presented.
The paper also discusses why ATLAS has decided to develop its own Linux based VMEbus driver and presents the features and performance of that driver and its user level library as well as some related software packages.

Summary

The data acquisition system of the ATLAS experiment contains several large, VMEbus based sub-systems. There will be about 120 9U VMEbus crates to house the Read-Out Drivers. In addition there will be of the order of 30 6U crates to house the modules of the Trigger and Timing Control system. Finally there is a large number of VMEbus based test benches both at CERN and in the collaborating institutes.
It was felt necessary to prevent the groups responsible for the individual sub-systems from selecting their favorite VMEbus Single Board Computer (SBC) by standardizing on a single type of SBC for all installations.
In 2001 a small group of experts was formed to specify the requirements of a common SBC both in terms of its technical features as well as the support which had to be guaranteed by the manufacturer for at least nine years. At the same time a number of VMEbus SBCs from different vendors was evaluated to identify potential problems and to better understand the advantages and disadvantages of the different SBC architectures. To avoid limiting the competition too much the final specification did allow for a wide range of architectures (i.e. PowerPC and Pentium, all types of VMEbus master interfaces). The SBC that was finally selected is based on a Pentium CPU and the Tundra Universe PCI to VMEbus interface.

The evaluation of this and similar SBCs has identified a number of potential problems with the Tundra Universe chip:
- It has no built in endian conversion. In case of a little endian CPU (e.g. Pentium) this feature has to be provided by some vendor specific auxiliary logic.
- Moderate performance
o D32 R/W = 4 MB/s
o D32 posted W = 13 MB/s
o D32 BLT = 20 MB/s
o D64 MBLT = 40 MB/s
- Difficult bus error handling
- No true constant address DMA for reading out FIFOs
- Problems with BERR terminated BLTs

Depending on the PCI host bridge used on the SBC problems in the form of VMEbus error can arise if the SBC has to deal with master and slave accesses at the same time.

In parallel with the H/W the options for the VMEbus access S/W were analyzed. Despite the effort made by the VISION standard a few years ago there is no widely accepted standard API for access to the VMEbus. A number of free and commercial drivers exist for the Tundra Universe chip but they are not compatible. Finally the decision was made to program a dedicated Linux VMEbus driver and library for ATLAS. This gives full control over the code and the API and allows optimizing the S/W for

the particular needs of ATLAS. The driver and library provide two ways of doing single cycles, extensive support for chained block transfers, bus error handling and the possibility to handle interrupts both synchronously and asynchronously. Less frequently used features such a support for SYSFAIL interrupts or special AM codes for geographical addressing (VME64x) have been added as well.

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Session Classification: Parallel session B4