Contribution ID: **1** Type: **Oral**

A VLSI Full Custom ASIC Front End for the Optical Module of NEMO Underwater Neutrino Detector

Tuesday 13 September 2005 11:00 (25 minutes)

A cubic KM scale underwater neutrino detector requires thousands of photomultipliers whose signal must be acquired and transferred through an electro-optical cable to shore for analysis and storage. The transferrable power and data bandwidth of this cable is limited. The work described here has been developed in the context of the NEMO Collaboration with the aim of studying and designing a front-end electronics for the Optical Modules, which contain the telescope optical sensors, as a full-custom Very Large Scale Integration (VLSI) Application Specific Integrated Circuit (ASIC). The advantages of this solution are manifold. The most important are low power consumption and the pre-analysis and opportune reduction of data to be transferred to the shore station for acquisition. A detailed description of the chosen architecture and the design principles of the blocks, that carry out the specialized function required by this architecture, will be given. The chips produced will be described and the test measurements performed will be shown.

Summary

The work here described has been developed within the NEMO Collaboration with the aim of studying and designing a front-end electronics for the Optical Modules, which contain the telescope optical sensors, as a full-custom Very Large Scale Integration (VLSI) Action Specific Integrated Circuit (ASIC). The advantages of this solution are manifold. The most important are the low power consumption and the pre-analysis and opportune reduction of data to be transferred to the shore station for acquisition. The former allows the crucial problem of power transfer to the submarine detector, subject to strong technological limitations, to be solved. More in detail, the main objectives that must be achieved are: • very low power because of the distance from the shore;
• only one submarine interconnecting cable to have the best reliability and to simplify the deployment;flexibility to give the possibility of changing parameters;very small dead-time to get good detector efficiency;
• high dynamic range to fit with different kinds of experiments;very good accuracy of experimental data;low costs, if possible! We can translate these objectives into design specifications for the electronics and show how we foresee obtaining this result. Power will be transferred to the detector at about 100 km from the shore. Since in these conditions the power transfer is limited, as we explained in previous chapters, the electronics power consumption must be limited to not more than a few kW in the whole detector, which is less than 200-300 mW in the OM. This means that the solution proposed by the NESTOR collaboration is unreliable.
We foresee contributing to obtaining this limited power consumption using, as much as possible, VLSI full-custom Action Specific Integrated Circuits (ASICS) in the OM.
Apart from Nestor, all the other submarine Cherenkov detectors use interconnections between the optical modules, which lead to various solution that are heavy, expensive and not very reliable. We want to use only one penetrator, through which, apart from the DC power supply, information between OMs and local control units will flow, in a bidirectional way. The system will be certainly more reliable and

will simplify the deployment. The choice of building coincidences between two or more OMs to limit rate and to obtain acceptable dead time in AMANDA and in ANTARES lacks flexibility. It is not possible, in practice, to change the detector. Even if one forecast proves to be wrong the whole system fails. If one wants a reasonable solution for the interconnections, coincidences must be limited to OMs in the same tower, but the latter does not seem an acceptable solution from the physics point of view. On the other hand to extend coincidences to adjacent modules in different towers makes the hardware more complex with incredible connections or requires a high-speed data transmission system among different modules, which seems unreasonable. It must be taken into consideration that to limit the dead time the coincidence window must be very small. BAIKAL, through a local coincidence between two opposite PMs uses a simple system, with a relatively small coincidence window. This solution dramatically raises the costs and worsens the dead times. For these reason we consider unfeasible the idea of hardware coincidences. NESTOR employs software coincidences. The same solution is anticipated for NEMO. We calculate to be able to get about 0.075% dead time, while the expectation for the other experiments, apart from NESTOR, is of the order of 1%. BAIKAL roughly elaborates the information in the OM and transmits only a part of it. ANTARES and AMANDA propose to perform 320 ns of auto triggered signal samplings at 400 MHz. In NEMO we foresee the transmission of few samplings (we say 10 samples equal to 50 ns) in the case of a Single Photo Electron (SPE) signal or a greater number in the case of a large, or long, signal or of a complex structure (i.e. 100 or 200 samples, equal to 500-1000 ns). In both cases the number of samples is held to be enough to draw form, energy and occurrence time with good precision.

In every case the two parameters are not fixed. They can be changed remotely. We have not deemed it necessary to proceed to oversampling. The system proposed, can allow the attainment of a 20 bit dynamics. If, for power limitations and dead time ANTARES and AMANDA decide to use 8 bit ADC their limit is 16 bit. The dynamics of BAIKAL is limited to 100 PE (7 bit). We foresee accuracy analogous to that of AMANDA: around 1 ns. From the PM two signals are extracted. The anode signal and the one extracted from one of the lower dynodes. When the PM anode signal, sent to the T&SPC (Trigger and Single Photon Classifier) module, makes a trigger event (enough to overcome the SPE/4 threshold) this module outputs a Start signal to the Control Unit. This starts the sampling mechanism performed by one of the two identical memories (Lira), whose size is 3´256 cells. Actually the T&SPC furnishes, after about 60 ns, also the classification of the signal. If it is classified as NSPE (Non Single Photo Electron) the system performs 100 samplings. Otherwise, only 10 samplings. Lira memory (Analogue Delay Line Italian acronym) is endowed with three identical channels one of which samples, simultaneously to the two PM signals, also the Master Clock (MC) at 20 MHz coming from the outside. This is done with the purpose of realizing a time recording system with about 1.4 ns rms resolution, increasable, if necessary, up to0.7ns. A 16-bit counter counts the clock cycles (16 bit correspond to about 3.3 ms). Every millisecond the slow control sends a reset signal to synchronize all the modules. At the trigger, the counter content is transferred to a FIFO to be subsequently used as a time stamp at 50 ns resolution.

Lira samples at the frequency of a Slave Clock (SK), 200 MHz. It is originated, through a frequency multiplier (PLL), starting from the same MC. From the moment that this last MC is sampled at the SC frequency, the system acts as a temporal nonius. One of the memories is always predisposed to perform the sampling. Nevertheless, it samples only for the preset number of times when the Trigger arrives. To be certain of capturing the signal coming from the PM, the latter is purposely delayed by the time necessary for the T&SPC to take the decisions of the case. When a signal has been entirely sampled, the memory, in which the sampling has happened switches to read phase and the other is ready to sample. The reading phase happens at high speed (10 MHz). Only the cells that have been written in the channel are read. Actually only one of the two signals sampled by the PM (under the control of the Dyn signal) is read and transferred to the ADC. The signal sampled in the channel of the fine time does not go to an ADC but, since it

is a signal made of levels, is introduced into an opportune logic for giving precise information on the arrival instant of the signal related to the MC. Once the content of a memory has been transferred and the ADC has ended the conversion this latter is put in a Power Down (PwD) state. In this way one can have a remarkable power saving, about 1/20.
Few hits of Clock, furnished before taking back the reading, put the ADC into the condition of correctly taking back its job.

Author: Dr LO PRESTI, Domenico (Catania University-Physics Department)

Presenter: Dr LO PRESTI, Domenico (Catania University-Physics Department)

Session Classification: Parallel session A1

Track Classification: Custom Integrated Circuits