Test of the End-Ladder Prototype Board of the ALICE SDD Experiment

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Abstract

The paper presents an end-ladder card prototype of the data acquisition chain of the ALICE SDD experiment. The prototype includes most of the electronics devices that will be applied to ALICE SDD experiment. The card interfaces with the front-end electronics and with the counting room detector data link via the interface card named CARLOS_rx. The end_ladder PCB has been fully tested by providing control signals and input vectors via a pattern generator and by collecting output data via the detector data link.

I. INTRODUCTION

The paper explains the design and the construction of an end-ladder card prototype for the Silicon Drift Detector (SDD) experiment, part of the Inner Tracking System (ITS) of the A Large Ion Collider Experiment (ALICE) [1], [2]. In the ITS, which is a portion of the whole ALICE detector, the End-Ladder card performs data reduction, compression and packing for the readout chain. Particularly it includes a chip, named CARLOS [3], which mainly carries out the above-mentioned tasks. Moreover, the end-ladder card interfaces with the Front-End Electronics (FEE) and elaborates and transmits the dataset received from the FEE through an optical channel to the counting room. Also, by means of other two optical channels, the card is synchronized with a 40 MHz system master clock and is configured via a serial signal. The paper describes also the design of the tests that have been carried out on the Printed Circuit Board (PCB) prototype.

II. ALICE SDD DETECTOR AND READOUT SYSTEM

The SDDs are high precision position-sensitive detectors, provide two-dimensional position information and are suitable for high track-density experiments at a low rate and a relatively slow readout rate (a few microseconds). The detector has a bi-directional structure through which electrons drift. In addition, each detector is made up of two half detectors. These half detectors are connected directly to the FEE chips, as illustrated on the left-hand side of Fig. 1. The amount of data generated by the SDD is large: each half detector consists of 256 anodes and for each anode 256 time samples must be taken to cover the full drift (time) length. The data that derives from one half detector are sent to one channel of the CARLOS chip which then interfaces with two half detectors. This explains how the data readout electronics work.

Both the front-end and End-Ladder boards take place in a radiation environment. The acquisition system therefore performs analog data acquisition, A/D conversion, buffering, data compression and interfacing to the ALICE SDD data acquisition system.

Data are transferred at 40 MHz from the eight front-end chips (Fs) of each half-detector to the End-Ladder modules. CARLOS performs zero suppression and data compression [4] before transmission to the DAQ system..

III. DUT-CARD

Before designing the prototype card we have faced the test card design that will follow to facilitate the creation of stimuli and the data collection by means of electronics instruments. Thus we have designed the actual ALICE SDD prototype card, with the up-to-date components foreseen for the final implementation on the experiment, embedded into a larger test card. Fig. 2 shows a sketch of the main blocks that compose the whole card, named Device Under Test card (DUT-card). The End-Ladder Prototype card is the actual device under test while the rest provides all the required I/O signals. Here, all the components that compose the whole card, except the End-Ladder Prototype, are logically grouped and named Test Card. It follows therefore, that the two logical units named End-Ladder Prototype card and Test Card are embedded into the same physical PCB, which is shown in Fig. 3 and named DUT-card. A Counter Room Emulator Card, that is part of the Test Card, provides, through two optical fibers, the clock signal and the serial instructions (serial signal) and by a third fiber receives back the compressed dataset at a serial rate of 800 Mb/s. This card contains a reference clock generator, two optical transceivers, a deserializer chip

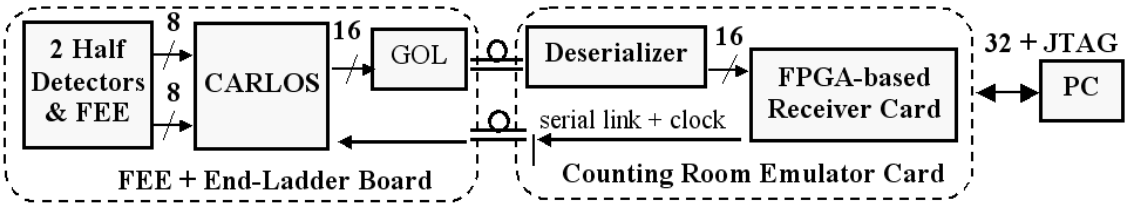

Figure 1: ALICE SDD Readout Architecture

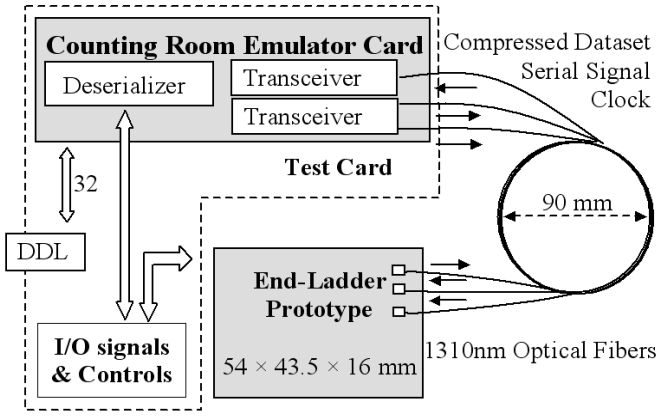

Figure 2: DUT-card sketch

(TLK1501) and an FPGA (XC2V1000) whose main function is data stream error detection. Moreover the Emulator Card includes an I/O port to interface either with a computer or with a logic analyzer. In more detail, this port has monitoring and analysis purposes.

The two bi-directional commercial transceivers, part of the Test Card, allow the interface with the End-Ladder Prototype card. In addition, the figure shows the I/O Signals & Controls block, part of the Test Card, which provides a hardwired external interface with laboratory instruments. In fact, via digital pattern generators and logic state analyzers, the DUT-card receives an input dataset as it were originated by the FEE and outputs a reduced, compressed and packed new output's dataset to the counting room. This latter dataset is recovered either via the state analyzers or via the DDL as shown in Fig. 2. The DDL in fact, can be connected to the

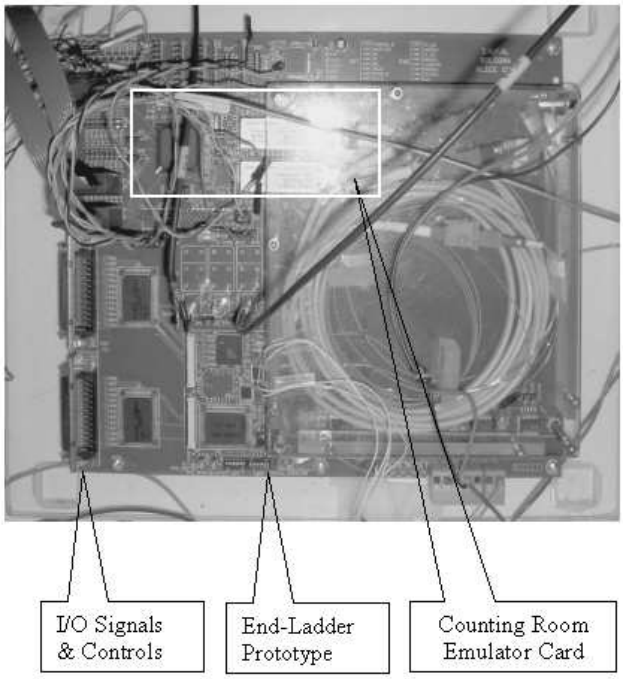

Figure 3: Picture of the DUT-card

DUT-card so that this can be tested as it were embedded within the real Data Acquisition (DAQ) chain. The End-Ladder Prototype card matches the final dimension while the Test Card does not since all its components will be removed in the final version before producing 300 End-Ladder cards. This number accounts for the cards inserted at first in the ALICE SDD plus nearly 50% spare parts that are estimated to be necessary for a ten-year of data-taking.

IV. End-Ladder Prototype card

Fig. 4 shows the layout of the components' positions on the End-Ladder Prototype card. Here the components are summarized. In more detail, by following the picture from the top-right corner, the laser diode is shown. This component transmits the compressed and packed dataset, at a rate of 800 Mb/s, to the Counting Room Emulator. Below the laser, two pin-diodes (FT1 and FT2) receive, from the same emulator, the clock and the serial signals. The latter signals provide the system configuration at start-up and may stop the acquisition in event of channel congestion. The 2 pin-diodes and the laser are single-mode, 1310 nm (wavelength) pig-tailed modules. These interface with the commercial transceivers on the Test Card via optical adaptors. In more detail, the received pin-diode signals interface with the other components through the RX40, 2-channel, receiver chip.

Let us now describe the system data-flow. The dataset that originate from the FEE enters the card through the Molex connectors and is read by CARLOS chip. This performs basically a bi-dimensional compression [5], [6] during the normal DAQ mode and works as a system JTAG switch during the FEE configuration. CARLOS reduces and packs the dataset and its outputs is serialized via the Gigabit Optical Link (GOL) serializer chip that interfaces, by means of an 800Mb/s link [7], with the laser diode. Finally, GOL serializes the dataset that is reconstructed within the Counting Room Emulator by a mirroring de-serializer device that output the

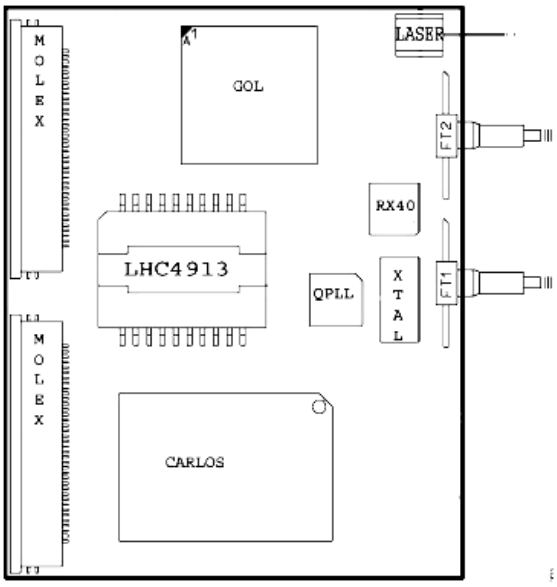

Figure 4: End-Ladder prototype card layout

data to the state analyzer instruments. As the GOL chip requires a low-jitter clock signal, as low as 50 ps, the QPLL clock filter chip has been applied. This locks the 40MHz clock signal, derived from one of the two pin-diodes, on a very-low-jitter 160 MHz crystal (XTAL). Then this frequencies is divided by four passed to the GOL and CARLOS chips. The chips are powered with a 2.5 V low-voltage regulator (LHC4913) that is configured for an overall current of 400 mA. All the components embedded into the End-Ladder Prototype card are Application Specific Integrated Circuits (ASICs) designed to be radiation-tolerant to the total ionizing dose that is estimated (nearly 30 krad) for a 10-years of data-taking within the ALICE ITS environment.

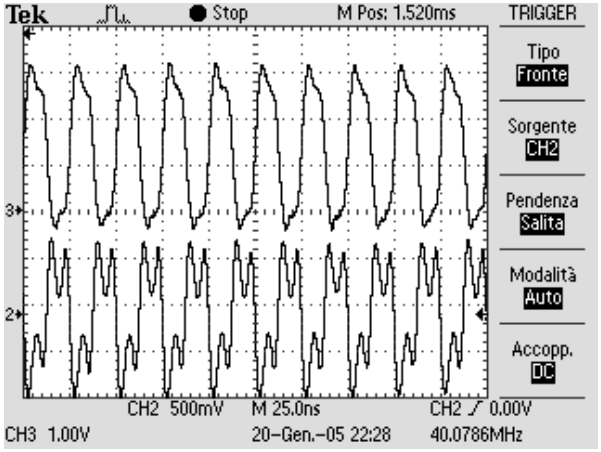

Figure 5a: Test 1

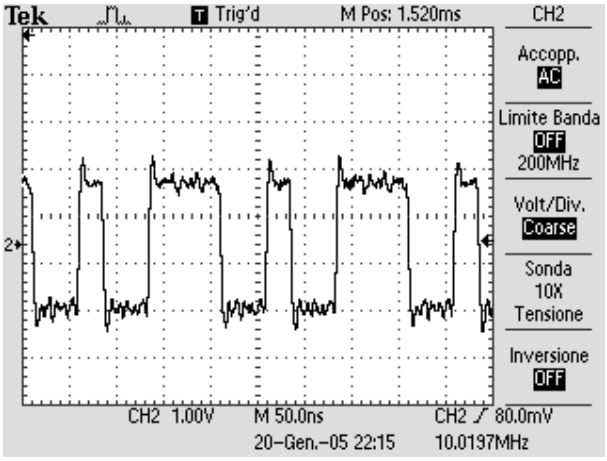

Figure 5b: Test 2

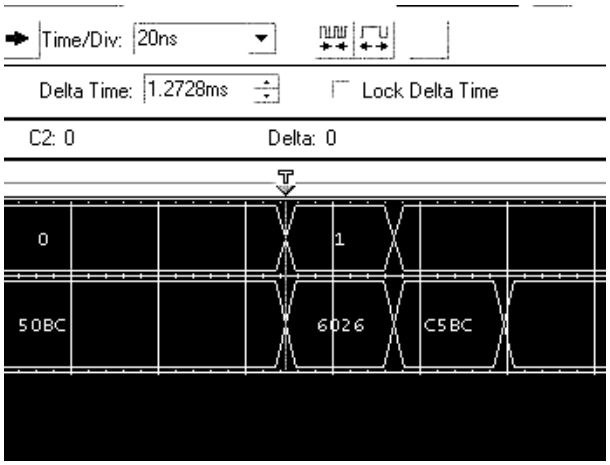

Figure 5c: Test 3

V. End Ladder System Test

To simulate the whole readout system a dedicated hardware and software test architecture has been designed. This is shown in Fig. 3. First, a pattern generator provides the input vectors that emulate the real SDD data. Second, the ALICE Detector Data Link (DDL) [8] system has been mounted in our laboratory to provide the FEE and the DUT cards with the necessary signals and controls as it were transmitted from the counting room. In this way we have designed a whole copy of the SDD readout system and, since that time, we have been able to emulate the data taking.

In more detail, the tests were divided in three main steps. Step 1 was set just to synchronize the clock signal over the optical fiber, the RX40 receiver and the QPLL clock filter. The clock was provided with pattern generator via the Counting Room Emulator Card. Fig. 5a shows the on-fiber input clock below and, above, the phased QPLL regenerated low-jitter signal.

Step 2 was oriented to configure the FEE and the end-ladder ASICs (CARLOS included). This was done via JTAG vectors provided with the pattern generator. All the ASICs were correctly programmed and Fig. 5b shows, as example, the recovered idle waveform on an input pin of CARLOS chip. When the JTAG programming is terminated CARLOS goes in a so-called "Run Mode". Then the chip is ready to process data coming from the FEE as soon as the trigger command is decoded and the output dataset is serialized by GOL chip (8B/10B encoding algorithm at 800 Mb/s). The tests performed with this configuration were error free.

Step 3 was the real data acquisition. The tests performed in our lab used the FEE without the actual drift detector. Thus, the acquired data were just noise or, on demand, the data were internally generated by the FEE as predefined shape pulses. Fig. 5c shows two specific codes: 50BC as idle standard word and 6026 as valid data. It can be noted that in correspondence with the valid data code 6026 a given enable signal goes to 1 and returns to 0 when the valid data end.

VI. Conclusion

The end ladder card prototype for ALICE SDD Experiment was designed, constructed and tested. The tests proved that the system works, the data and signals are recovered correctly on a PC in our laboratory after being passed trough the optical fibres, the GOL serializer, the commercial deserializer chip and the DDL.

CARLOS chip was remotely controlled using the serial back-link via the Counting Room Emulator Card (JTAG and trigger commands proved the full functionality of the system). The QPLL filter showed to match the clock jitter

requirements. The data transmission in the 8B/10B mode via 800 Mb/s optical link was finally error free.
In the meantime a few improvements have been arisen for the PCB design that is in progress with Torino ALICE SDD group to match the mechanical and cooling requirements.

VII. REFERENCES

[1] A Large Ion Collider Experiment at CERN LHC, (http://alice.web.cern.ch/Alice/index.html)
[2] ALICE Collaboration, "ALICE: Physics Performance Report", Jour. Phys. G, 30, (2004), 1517-1763, ISSN 0954-3899, (http://www.iop.org/EJ/abstract/0954-3899/30/11/001/)
[3] A. Gabrielli et al., "Implementation of a bi-dimensional compressor for a high energy physics experiment", IEEE Trans. Nucl. Sci., 51, 5, (2004), ISSN 0018-9499,
[4] A. Werbrouck et al., "Image compression for the silicon drift detectors in the ALICE experiment" Nucl. Instr. Meth. A, 471, (2001), 281-284
[5] D. Falchieri et al., ALICE-CERN Internal Note, "The successful connection to the ALICE DDL of the rad-hard ASIC CARLOS-v2 belonging to the SDD readout chain", (https://edms.cern.ch/file/352427/1/ALICE-INT-2002-24.pdf)
[6] S. Antinori et al., "A Rad-Hard 2D-Compressor ASIC for ALICE SDD Experiment", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 524, 1-3, (2004), 295-305
[7] A. Marchioro et al., "A Radiation Tolerant Gigabit Serializer for LHC Data Transmission", 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14/09/2001, (http://proj-gol.web.cern.ch/proj-gol/paperLEB2001.pdf)
[8] C.E.R.N., PH Department, AID Group, ALICE DDL, ALICE-INT-2004-018 version 1.0, (http://alice-proj-ddl.web.cern.ch/alice-proj-ddl/doc/ALICE-INT-2004-018.pdf)