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# End-Ladder Board for ALICE SDD Experiment

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The paper presents an end-ladder card prototype of the data acquisition chain of the ALICE SDD experiment. The prototype includes most of the electronics devices that will be applied to ALICE SDD experiment. The card interfaces with the front-end electronics and with the counting room detector data link. It has been designed taking into account the constraints on the dimensions of the final apparatus. It has been fully tested within the data acquisition chain and, since the results were good,the final design for production is close to submission.

## Summary

The paper explains the design and the construction of an end-ladder card prototype for the Silicon Drift Detector (SDD) experiment, part of the Inner Tracking System (ITS) of the A Large Ion Collider Experiment (ALICE). The end-ladder card interfaces with the Front-End Electronics (FEE) and elaborates and transmits the dataset received from the FEE through an optical channel to the counting room. The paper describes also the design of the tests that have been carried out on the Printed Circuit Board prototype.
The dataset that originate from the FEE enters the card through the Molex connectors and is read by CARLOS chip. This performs basically a bi-dimensional compression during the normal DAQ mode and works as a system JTAG switch during the FEE configuration. CARLOS reduces and packs the dataset and its outputs is serialized via the Gigabit Optical Link (GOL) serializer chip that interfaces, by means of an 800Mb/s link, with the laser diode. Finally, GOL serializes the dataset that is reconstructed within the Counting Room Emulator by a mirroring de-serializer device that output the data to the state analyzer instruments. As the GOL chip requires a low-jitter clock signal, as low as 50 ps, the QPLL clock filter chip has been applied. This locks the 40MHz clock signal, derived from one of the two pin-diodes, on a very-low-jitter 160 MHz crystal (XTAL). Then this frequencies is divided by four passed to the GOL and CARLOS chips. The chips are powered with a 2.5 V low-voltage regulator (LHC4913) that is configured for an overall current of 400 mA.
All the components embedded into the End-Ladder Prototype card are Application Specific Integrated Circuits (ASICs) designed to be radiation-tolerant to the total ionizing dose that is estimated (nearly 30 krad) for a 10-years of data-taking within the ALICE ITS environment.
The amount of data generated by the SDD originates from 2 half detectors for each CARLOS chip. As each half detector is composed of 256 anodes and, for each anode, 256 time samples are taken in order to cover the full drift (time) length, altogether each detector is able to generate a dataset made up of 256 × 256 data words. The two half detectors'dataset are read by the two channels of CARLOS chip. Thus, the readout electronics is composed of FEE boards, which collect data from the SDDs and End-Ladder boards that reduce, pack and serialize the dataset. Then this is sent to the counting room where it is reconstructed as it was transmitted.
To simulate the whole readout system a dedicated hardware and software test architecture has been designed. First, a pattern generator provides the input vectors that emulate the real SDD data. Second, the ALICE Detector Data Link system has been mounted in our laboratory to provide the FEE and the DUT cards with the necessary signals and controls as it were transmitted from the counting room. In this way we have designed a whole copy of the SDD readout system and, since that time, we have been able to emulate the data taking.

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