Evaluation of SiGe biCMOS Technologies for Next Generation Strip Readout

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Bipolar for Large C – Fast τ_s

We have shown for past experiments that the bipolar technology has advantages over CMOS in power and performance for front-end amplification of silicon strip readout when the capacitive loads are high and the shaping times short.

- **ZEUS-LPS Tek-Z IC**
- **SSC-SDC LBIC IC**
- **ATLAS-SCT ABCD, CAFE-M, CAFE-P ICs**

Since CMOS is the preferred technology for back-end data processing, biCMOS technologies have not been readily available, making it difficult to find a one chip solution.

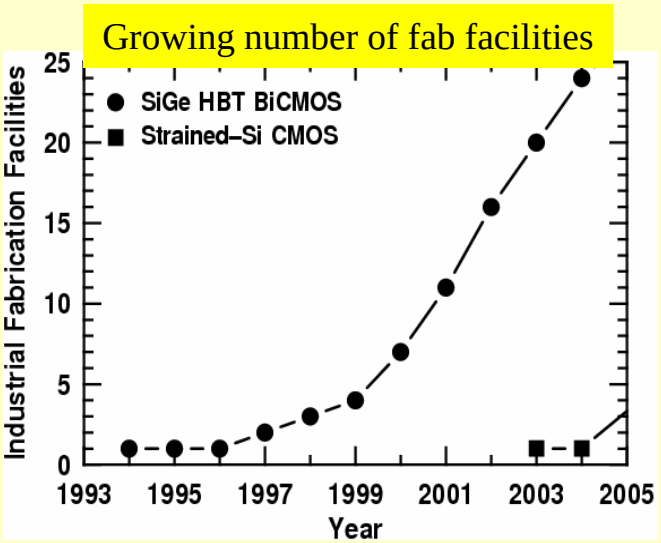
Experience with the commercial 0.25 μm CMOS has shown the great advantage of using a high volume commercial rather than a niche technology.

biCMOS with Enhanced SiGe

The market for wireless communication has now spawned many biCMOS technologies where the bipolar devices have been enhanced with a germanium doped base region (SiGe devices).

We have identified at least the following vendors:

- **IBM (at least 3 generations available)**
- **STm**
- **IHP, (Frankfurt on Oder, Germany)**
- **Motorola**
- **JAZZ**



Advanced versions include CMOS with feature sizes of 0.25 μm to 0.13 μm.

The bipolar devices have DC current gains (β) of several 100 and f_Ts up to 100s of GHz. This implies very small geometries that could afford higher current densities and more rad-hardness.

Tracker Regions Amenable for SiGe

For the inner tracker layers, pixel detectors will be needed, and their small capacitances allow the use of deep sub-micron CMOS as an efficient readout technology.

Starting at a radius of about 20 cm, at fluence levels of 10^{15} n/cm^2, short strips can be used, with a detector length of about 3 cm and capacitances of the order of 5 pF.
At a radius of about 60 cm, the expected fluence is a few times 10^{14} p/cm^2, and longer strips of about 10 cm and capacitance of 15 pF can be used.

It is in these two outer regions with sensors with larger capacitive loads where bipolar SiGe might be used in the front-end readout ASICs with welcome power savings while still maintaining fast shaping times.

Biasing the Analogue Circuit

The analog section of a readout IC for silicon strips typically has a special front transistor, selected to minimize noise (often requiring a larger current than the other transistors), and a large number of additional transistors used in the shaping sections and for signal-level discrimination.

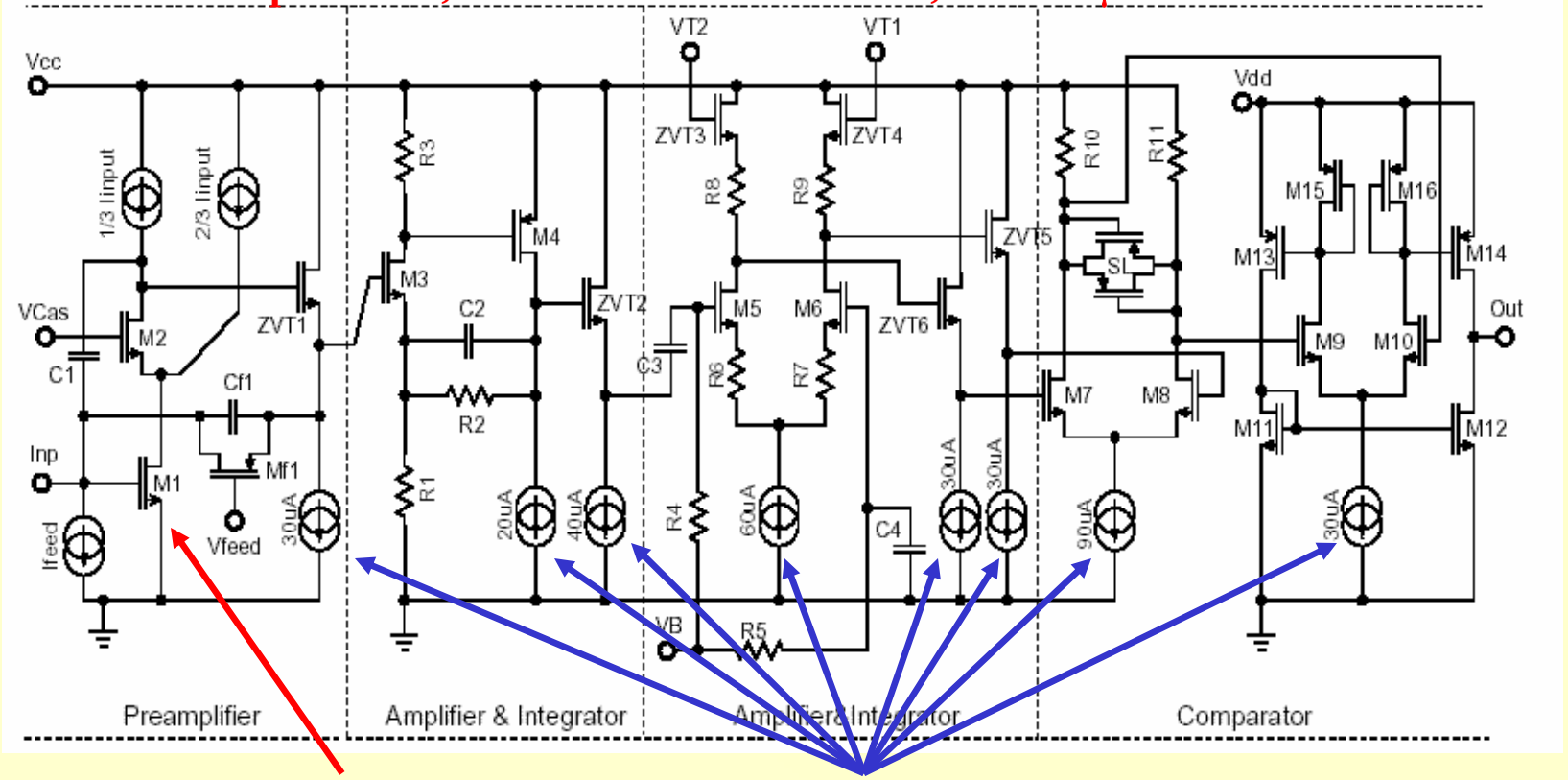
The current for the front transistor is selected in order to achieve the desired transconductance (minimize noise). For the other bipolar devices, bias levels for the other transistors are determined to achieve the necessary rad-hardness, matching and shaping times.

Depending upon the performance (especially radiation hardness) of the bipolar process, power savings could be realized in both the front transistor and in the other parts of the analogue circuit.

Potential CMOS Front-End

Architecture of the Front-End channel

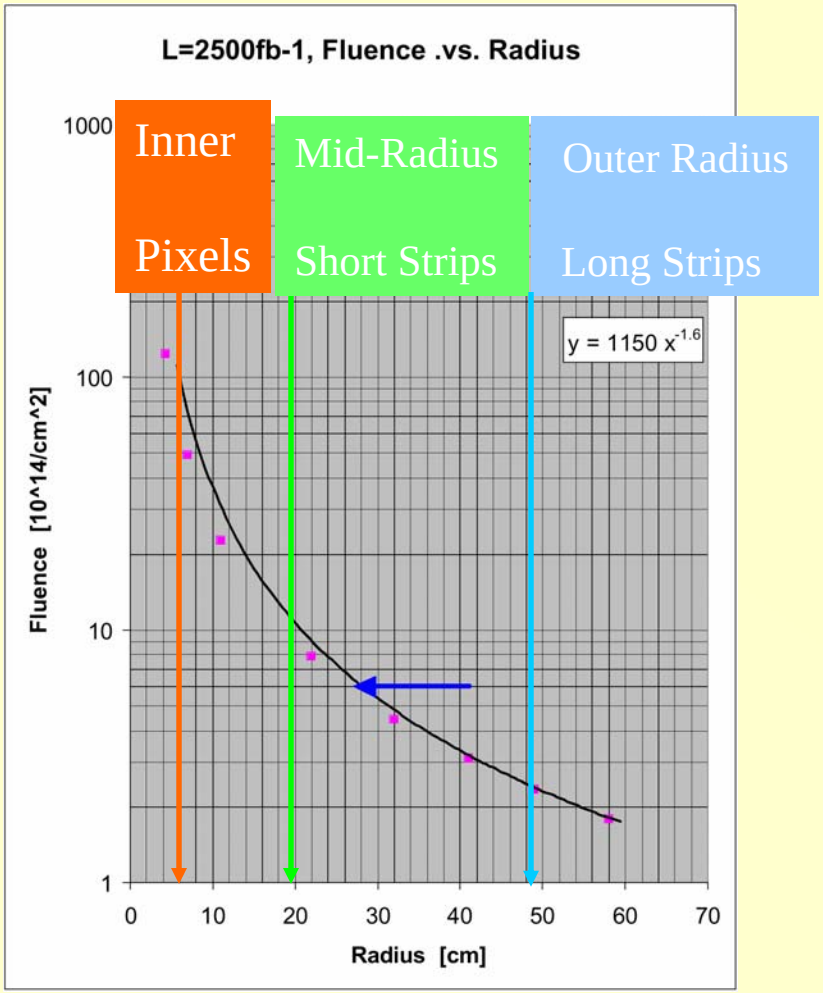
J. Kaplon et al., 2004 IEEE Rome Oct 2004, use 0.25 μm CMOS



For CMOS: Input transistor: 300 μA, other transistors 330 μA (each 20 – 90 μA)

Radiation vs. Radius in Upgraded Tracker

The usefulness of a SiGe bipolar front-end circuit will depend upon its radiation hardness for the various regions (i.e. radii) where silicon strip detectors might be used.



First SiGe High-rate Radiation Testing

Radiation testing has been performed on some SiGe devices by our Georgia Tech collaborators up to a fluence of $1x10^{14}$ p/cm^2 and they have demonstrated acceptable performance. (See for example: http://isde.vanderbilt.edu/Content/muri/2005MURI/Cressler_MURI.ppt)

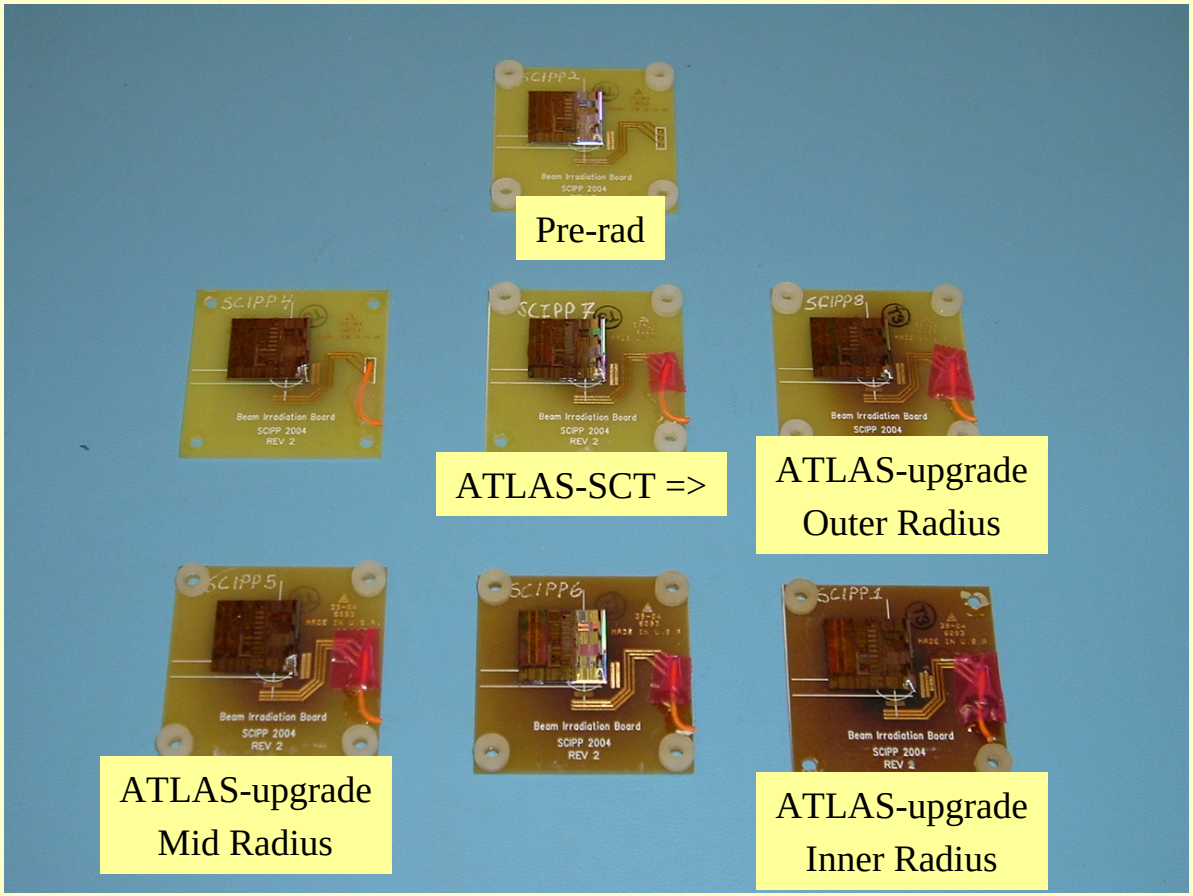
In order to extend this data to higher fluences, we obtained some arrays of test structures from our collaborator at Georgia Tech. These were from a β-enhanced 5HP process from IBM. (i.e. the β was ~250 rather than ~100.)

The parts were tested at UCSC and with the help of RD50 collaborators (Michael Moll & Maurice Glaser) they were irradiated in Fall 2004 at the CERN PS and then re-tested at UCSC.

For expediency, all terminals were grounded during the irradiation This gives slightly amplified rad effects than with normal biasing.

Annealing was performed after initial post-rad testing.

Irradiated Samples

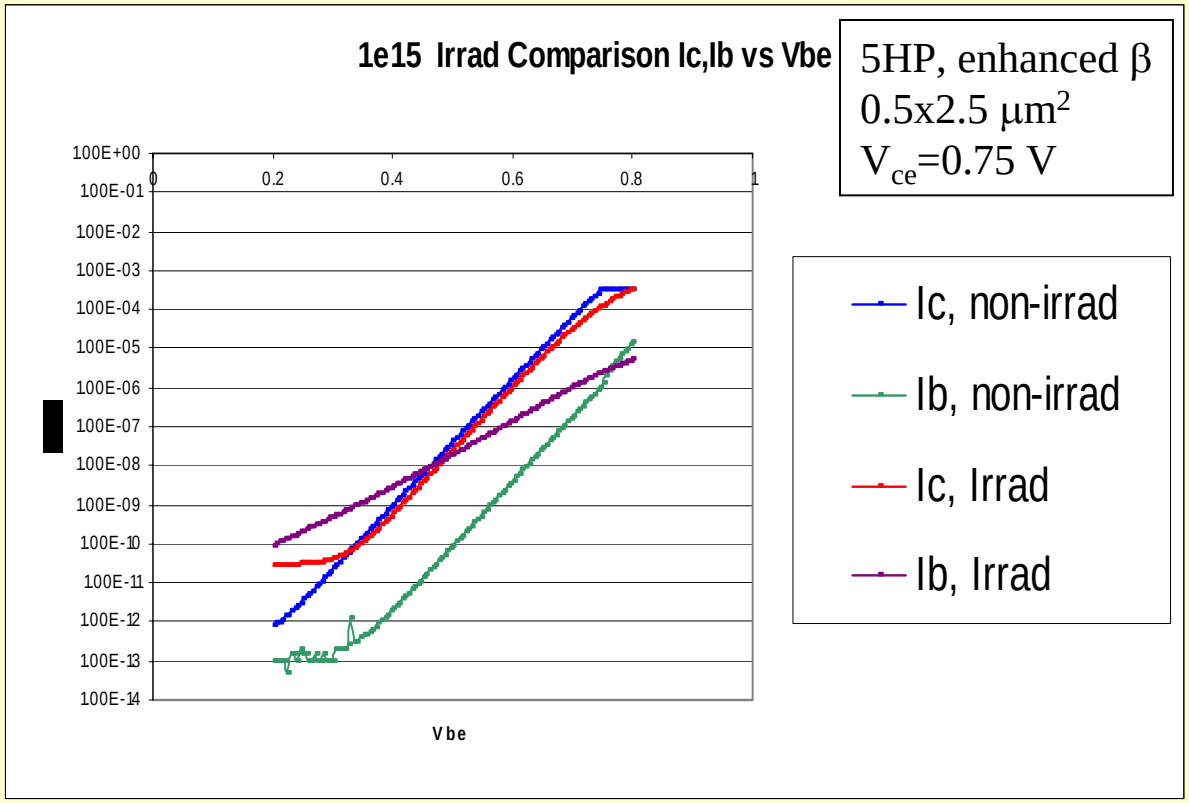


Fluences:

4.15E13 1.15E14 3.50E14 1.34E15 3.58E15 1.05E16

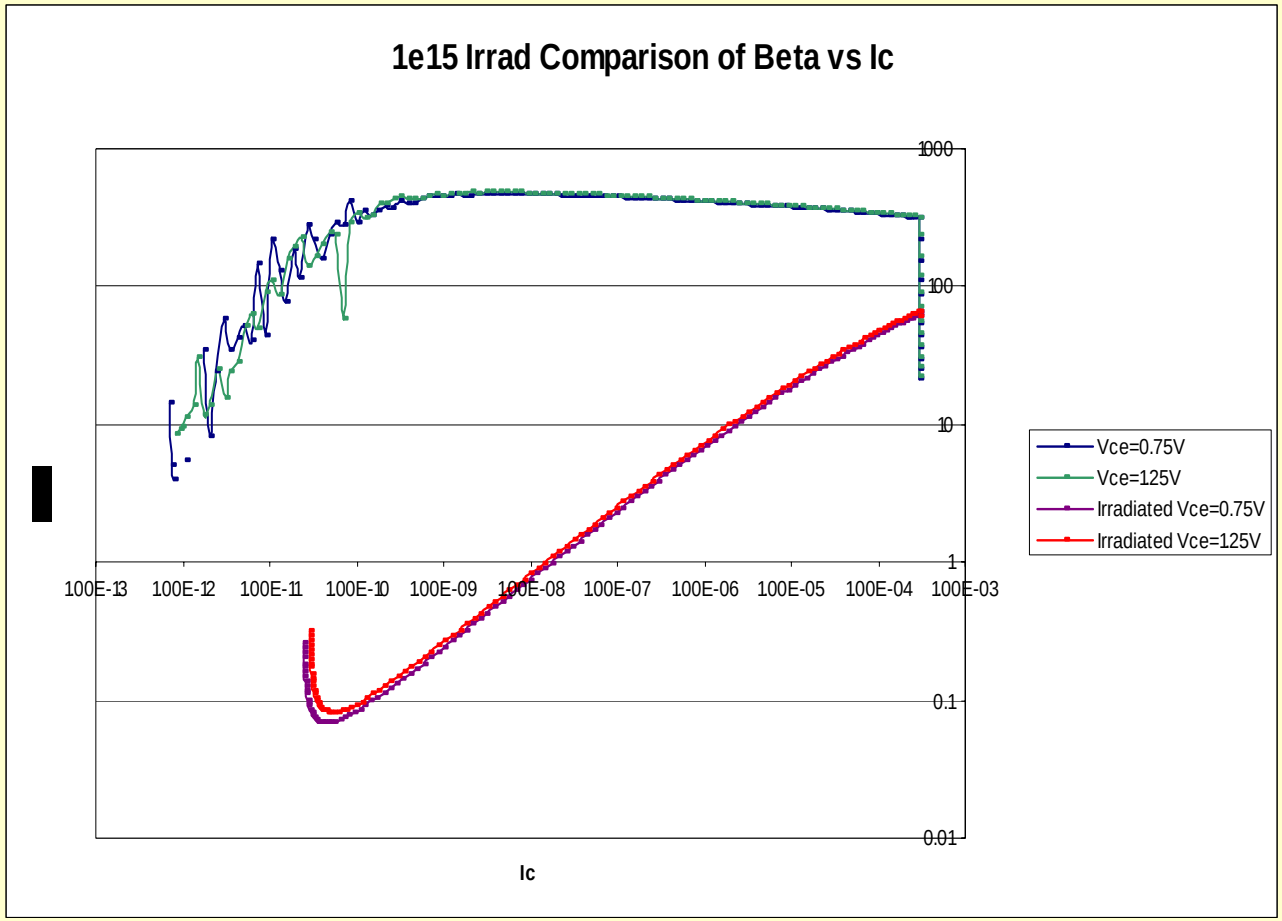
Base Leakage Current Increased by Radiation

Gummel Plot before and after 1.3×10^{15} p/cm^2 (β decreases as base leakage current increases.)



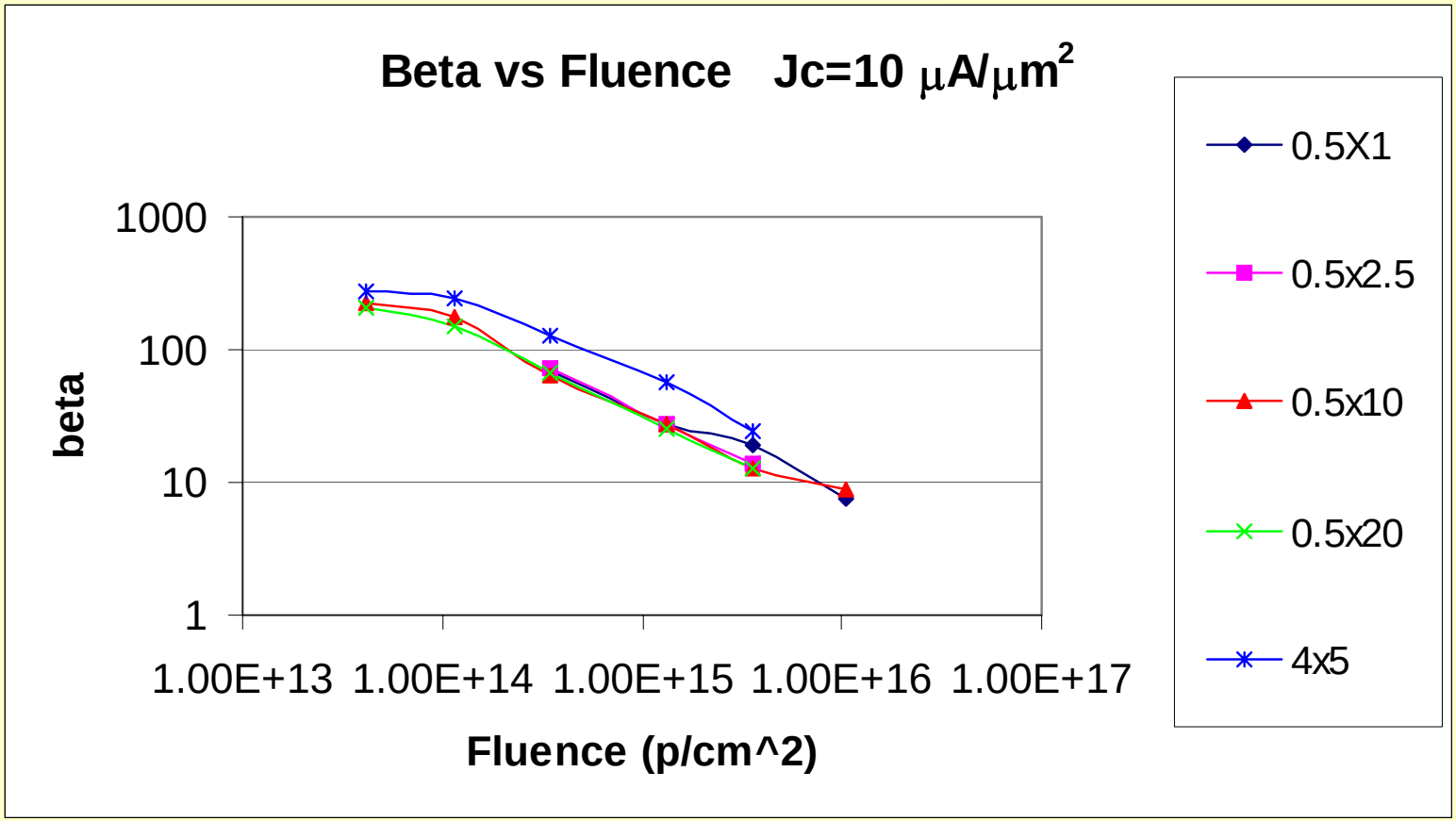
Radiation Damage vs. Currents

We see the typical increase in post-rad β at higher currents



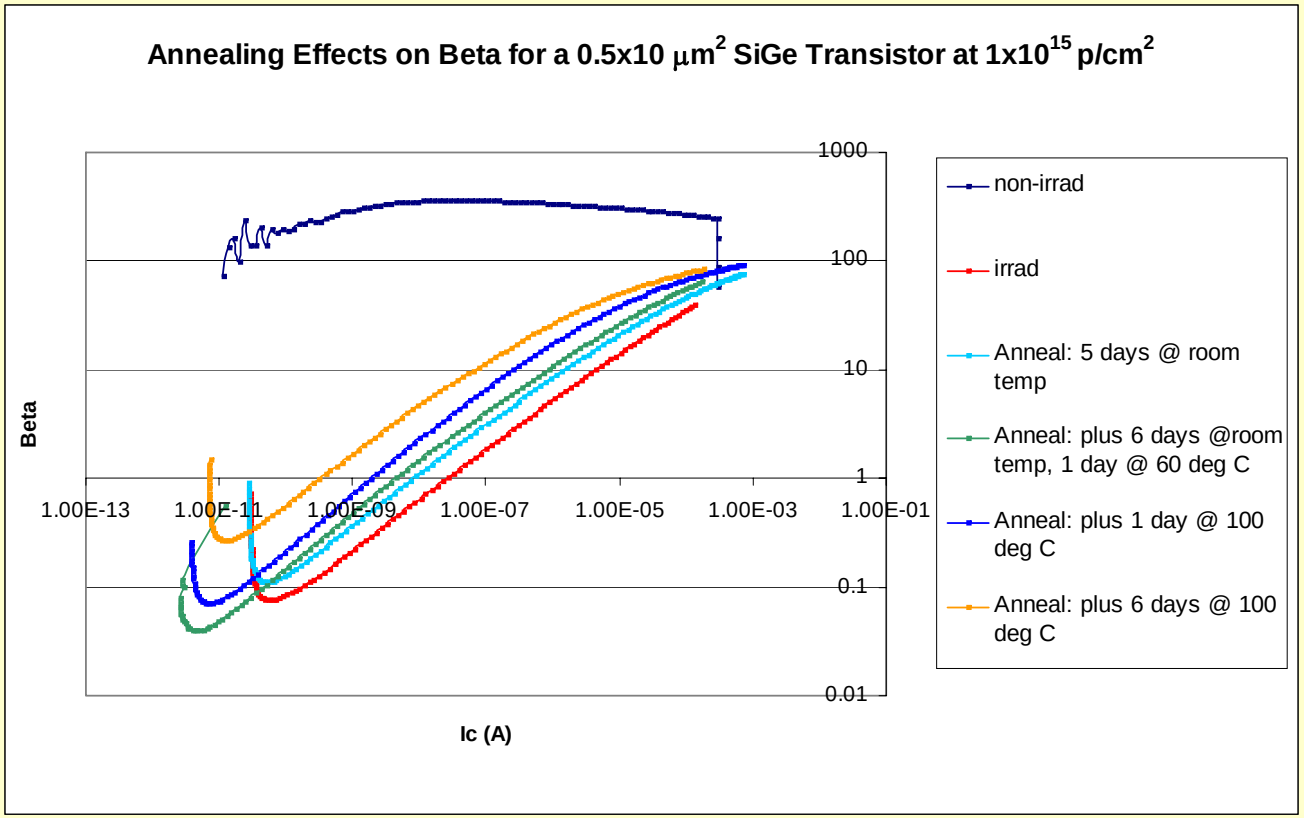
Scaling by Current Density

As expected radiation effects are nearly size independent when scaled by current density.



Annealing Effects

Annealing repairs some of the damage, especially since all device terminals were grounded during irradiation.



Feasibility Estimate for 5HP

As a quick estimate of feasibility and power savings, we can find an operating point with $\beta \geq 50$.

At 1.3×10^{15} (radius ~20cm) the minimum size transistor can operate at 100 nA.

Fluence: 1.34E15 β=50	Required Current	
Transistor Size μm^2	I_c irrad	I_c anneal
0.5x1	3.E-05	1.E-07
0.5x2.5	7.E-05	4.E-06
0.5x10	4.E-04	1.E-05
0.5x20		6.E-05
4x5	1.E-04	1.E-05

For R ~20 cm, bias at I_c = 10 μA shows these effective betas:

Fluence: 1.34E15 I_c=10μA			
Transistor Size μm^2	β_{pre}	β_{irrad}	β_{anneal}
0.5x1	242	35	111
0.5x2.5	320	25	63
0.5x10	302	15	51
0.5x20	300	9	31
4x5	372	19	48

IHP Design to Estimate Power Use of SCT Upgrade Front End

IHP has the SG25H1 200 Ghz Sige process available on Europractice. Beta is ~200. In parallel with radiation testing by Barcelona, UCSC is developing an eight channel amplifier/comparator with similar specifications to the present ABCD.

The x4 minimum transistor has base resistance of 51 Ω, .21 μm x 3.36 μm. 0.25 μm CMOS is also included. Extensive use is made of the 2.0 kΩ/ square unsilicided polysilicon resistor structure, since this is expected to be radiation resistant.

The purpose of this FE design is to estimate the low current bias performance of SiGe, and to see whether it can produce significant power savings. The target voltage bias level is 2 V.

Design Procedure Details

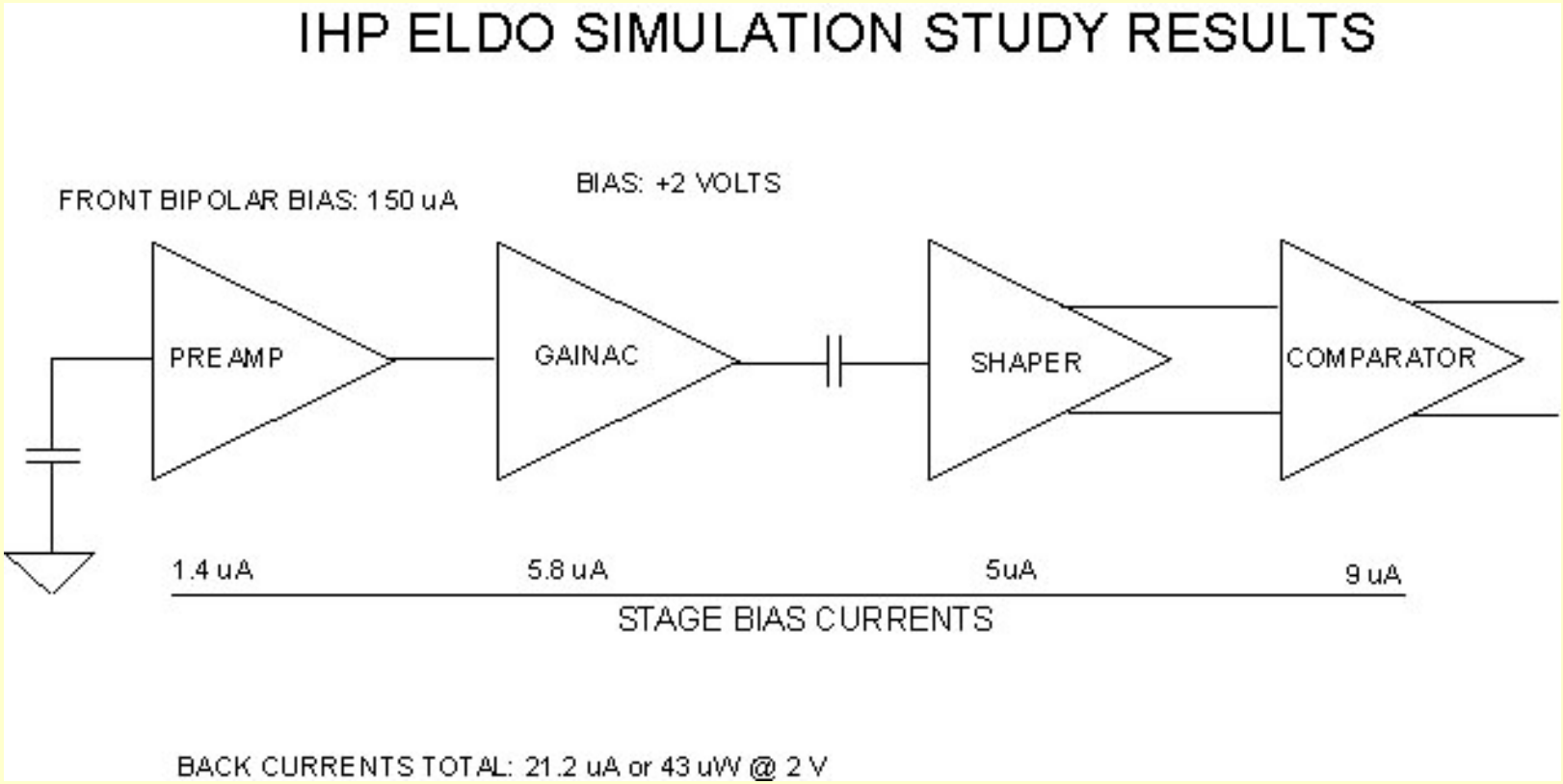
IHP provides a Cadence Kit, with support for both Diva and Allegro.

The bipolar devices are complete as provided, no editing allowed, with some hidden layers to protect IHP intellectual property.

Radiation hard annular NMOS transistor drawing is well supported. This is done by allowing 135 degree bends of Poly lines on Active in the DRC. There are included Virtuoso utilities that are needed for successful DRC.

Cadence Spectre does not DC converge well. Mentor has Eldo utility "Artist Link" that enables Eldo to run with Cadence schematic Composer. Eldo converges vigorously. Overall, the Cadence Kit is complete enough, and with the help of Eldo, is a good toolset.

SCT-FE Sim Results



First Guess at Potential Power Savings

Using similar estimates of bias settings and transistor counts, an estimate for power can be obtained.

CHIP TECHNOLOGY **FEATURE**	0.25 μm CMOS ABCDS/FE J. Kaplon et al., (IEEE Rome Oct 2004)		IHP SG25H1 SCT-FE Preliminary design	
Power: Bias for all but front transistor	330 μA	0.8 mW	= 30 μA (conservative)	.06 mW
Power: Front bias for 25 pF load	300 μA	0.75 mW	150 μA	0.30 mW
Power: Front bias for 7 pF load	120 μA	0.3 mW	50 μA	0.10 mW
Total Power (7 pF) $2x10^{15}$		1.1 mW		0.16mW
Total Power (25 pF) $3x10^{14}$		1.5 mW		0.36 mW

Conclusions

First tests of one SiGe biCMOS process indicate that the bipolar devices may be sufficiently rad-hard for the upgraded ATLAS tracker, certainly in the outer-radius region and even perhaps in the mid-radius region.

A simulation estimate of power consumption for such a SiGe front-end circuit indicates that significant power savings might be achieved.

More work is needed to both confirm the radiation hardness and arrive at more accurate estimates of power savings.

In particular, with so many potential commercial vendors available, it is important to understand if the post-radiation performance is generic to the SiGe technology or if it is specific to some versions.

Work Ahead

Along with our collaborators, we plan two parallel paths of work.

First, we plan more irradiations with several SiGe processes. In particular, we plan to test at least the IBM 5HP, IBM enhanced 5HP, IBM 8HP, IHP SG25H1 and one from STm.

- **CNM has obtained a first set of test structures from IHP and is proceeding.**
- **UCSC has recently received the IBM test structures.**
- **We have been promised test structures from STm but a schedule is not yet fixed.**

To obtain a better handle on the true power savings, we will submit an IHP 8 channel amplifier/comparator early in 2006. This work is in parallel with IHP radiation characterization.