11th Workshop on Electronics for LHC and future Experiments

Report of Contributions

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Contribution ID: **1** Type: **Oral**

A VLSI Full Custom ASIC Front End for the Optical Module of NEMO Underwater Neutrino Detector

Tuesday 13 September 2005 11:00 (25 minutes)

A cubic KM scale underwater neutrino detector requires thousands of photomultipliers whose signal must be acquired and transferred through an electro-optical cable to shore for analysis and storage. The transferrable power and data bandwidth of this cable is limited. The work described here has been developed in the context of the NEMO Collaboration with the aim of studying and designing a front-end electronics for the Optical Modules, which contain the telescope optical sensors, as a full-custom Very Large Scale Integration (VLSI) Application Specific Integrated Circuit (ASIC). The advantages of this solution are manifold. The most important are low power consumption and the pre-analysis and opportune reduction of data to be transferred to the shore station for acquisition. A detailed description of the chosen architecture and the design principles of the blocks, that carry out the specialized function required by this architecture, will be given. The chips produced will be described and the test measurements performed will be shown.

Summary

The work here described has been developed within the NEMO Collaboration with the aim of studying and designing a front-end electronics for the Optical Modules, which contain the telescope optical sensors, as a full-custom Very Large Scale Integration (VLSI) Action Specific Integrated Circuit (ASIC). The advantages of this solution are manifold. The most important are the low power consumption and the pre-analysis and opportune reduction of data to be transferred to the shore station for acquisition. The former allows the crucial problem of power transfer to the submarine detector, subject to strong technological limitations, to be solved. More in detail, the main objectives that must be achieved are: • very low power because of the distance from the shore;
• only one submarine interconnecting
cable to have the best reliability and to simplify the deployment;flexibility to give the possibility of changing parameters;very small dead-time to get good detector efficiency;
• high dynamic range to fit with different kinds of experiments;very good accuracy of experimental data;low costs, if possible! We can translate these objectives into design specifications for the electronics and show how we foresee obtaining this result. Power will be transferred to the detector at about 100 km from the shore. Since in these conditions the power transfer is limited, as we explained in previous chapters, the electronics power consumption must be limited to not more than a few kW in the whole detector, which is less than 200-300 mW in the OM. This means that the solution proposed by the NESTOR collaboration is unreliable.

We foresee contributing to obtaining this limited power consumption using, as much as possible, VLSI full-custom Action Specific Integrated Circuits (ASICS) in the OM.
Apart from Nestor, all the other submarine Cherenkov detectors use interconnections between the optical modules, which lead to various solution that are heavy, expensive and not very reliable. We want to use only one penetrator, through which, apart from the DC power supply, information between OMs and local control units will flow, in a bidirectional way. The system will be certainly more reliable and will simplify the deployment. The choice of building coincidences between two or more OMs to limit rate and to obtain acceptable dead time in AMANDA and in ANTARES lacks flexibility. It is not possible, in practice, to change the detector. Even if one forecast proves to be wrong the whole system fails. If one wants a reasonable solution for the interconnections, coincidences must be limited to OMs in the same tower, but the latter does not seem an acceptable solution from the physics point of view. On the other hand to extend coincidences to adjacent modules in different towers makes the hardware more complex with incredible connections or requires a high-speed data transmission system among different modules, which seems unreasonable. It must be taken into consideration that to limit the dead time the coincidence window must be very small. BAIKAL, through a local coincidence between two opposite PMs uses a simple system, with a relatively small coincidence window. This solution dramatically raises the costs and worsens the dead times. For these reason we consider unfeasible the idea of hardware coincidences. NESTOR employs software coincidences. The same solution is anticipated for NEMO. We calculate to be able to get about 0.075% dead time, while the expectation for the other experiments, apart from NESTOR, is of the order of 1%. BAIKAL roughly elaborates the information in the OM and transmits only a part of it. ANTARES and AMANDA propose to perform 320 ns of auto triggered signal samplings at 400 MHz. In NEMO we foresee the transmission of few samplings (we say 10 samples equal to 50 ns) in the case of a Single Photo Electron (SPE) signal or a greater number in the case of a large, or long, signal or of a complex structure (i.e. 100 or 200 samples, equal to 500-1000 ns). In both cases the number of samples is held to be enough to draw form, energy and occurrence time with good precision.
In every case the two parameters are not fixed. They can be changed remotely. We have not deemed it necessary to proceed to oversampling. The system proposed, can allow the attainment of a 20 bit dynamics. If, for power limitations and dead time ANTARES and AMANDA decide to use 8 bit ADC their limit is 16 bit. The dynamics of BAIKAL is limited to 100 PE (7 bit). We foresee accuracy analogous to that of AMANDA: around 1 ns. From the PM two signals are extracted. The anode signal and the one extracted from one of the lower dynodes. When the PM anode signal, sent to the T&SPC (Trigger and Single Photon Classifier) module, makes a trigger event (enough to overcome the SPE/4 threshold) this module outputs a Start signal to the Control Unit. This starts the sampling mechanism performed by one of the two identical memories (Lira), whose size is 3´256 cells. Actually the T&SPC furnishes, after about 60 ns, also the classification of the signal. If it is classified as NSPE (Non Single Photo Electron) the system performs 100 samplings. Otherwise, only 10 samplings. Lira memory (Analogue Delay Line Italian acronym) is endowed with three identical channels one of which samples, simultaneously to the two PM signals, also the Master Clock (MC) at 20 MHz coming from the outside. This is done with the purpose of realizing a time recording system with about 1.4 ns rms resolution, increasable, if necessary, up to0.7ns. A 16-bit counter counts the

clock cycles (16 bit correspond to about 3.3 ms). Every millisecond the slow control sends a reset signal to synchronize all the modules. At the trigger, the counter content is transferred to a FIFO to be subsequently used as a time stamp at 50 ns resolution.
Lira samples at the frequency of a Slave Clock (SK), 200 MHz. It is originated, through a frequency multiplier (PLL), starting from the same MC. From the moment that this last MC is sampled at the SC frequency, the system acts as a temporal nonius. One of the memories is always predisposed to perform the sampling. Nevertheless, it samples only for the preset number of times when the Trigger arrives. To be certain of capturing the signal coming from the PM, the latter is purposely delayed by the time necessary for the T&SPC to take the decisions of the case. When a signal has been entirely sampled, the memory, in which the sampling has happened switches to read phase and the other is ready to sample. The reading phase happens at high speed (10 MHz). Only the cells that have been written in the channel are read. Actually only one of the two signals sampled by the PM (under the control of the Dyn signal) is read and transferred to the ADC. The signal sampled in the channel of the fine time does not go to an ADC but, since it is a signal made of levels, is introduced into an opportune logic for giving precise information on the arrival instant of the signal related to the MC. Once the content of a memory has been transferred and the ADC has ended the conversion this latter is put in a Power Down (PwD) state. In this way one can have a remarkable power saving, about 1/20.
Few hits of Clock, furnished before taking back the reading, put the ADC into the condition of correctly taking back its job.

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Session Classification: Parallel session A1

Track Classification: Custom Integrated Circuits

Contribution ID: **2** Type: **Oral**

The ATLAS Level-1 Central Trigger Processor

Tuesday 13 September 2005 11:00 (25 minutes)

The ATLAS Level-1 Central Trigger Processor (CTP) combines information from calorimeter and muon trigger processors and makes the final Level-1 Accept (L1A) decision on the basis of lists of selection criteria (trigger menus). In addition to the event-selection decision, the CTP also provides trigger summary information to the data acquisition system and the Level-2 trigger. It further provides accumulated and bunch-by-bunch scaler data for monitoring of the trigger, detector and beam conditions.
The CTP will be presented and results will be shown from tests with the calorimeter and muon trigger processors connected to detectors in a particle beam, as well as from stand-alone full-system tests in the laboratory which were used to validate the CTP.

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Session Classification: Parallel session B1

Track Classification: Triggering

Contribution ID: **4** Type: **Poster**

Modeling of the Minimum Ionizing Particle detection in Active Pixel Sensor Devices for High Energy Physics Silicon Detectors

The new TCAD tools for IC modeling allow the verification of the silicon circuit implementation from the fabrication stages to the final implementation circuits. Using such setup a study of the Minimum Ionizing Particle (MIP) has been carried on in order to optimize and predict behaviors of the Silicon Detectors used by High Energy Physics experiments. This paper shows the use of such tools to model and reproduce detection conditions for Active Pixel Sensor detectors and their possible influence over the initial design expectations.

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Contribution ID: **5** Type: **Oral**

Design and performance of the front-end electronics of the LHCb Muon Detector

Thursday 15 September 2005 14:50 (25 minutes)

The system architecture of the front-end electronics of the LHCb Muon Detector, consisting of wire-chamber detectors and, for a small region, of triple-GEM detectors, is reviewed. The design of the front-end boards and of the ASD chip, the CARIOCA and the CARIOCA-GEM, are discussed in detail, together with the performances measured both with test benches in the lab and on chamber with radioactive sources and cosmic ray stands.
The status of the production and the testing procedures of the 8,000 boards and the 24,000 chips, built with the 0.25mm radiation tolerant technology, will also be summarized.

Summary

The LHCb Muon system consists of five stations of detectors, M1 to M5, only the first one lying before the calorimeters. Each station is radially segmented in logical pads, which are the input cells to the level-0 Muon trigger, of four sizes, R1 to R4.
Most of the system is builts with the wire-chamber technology while only M1-R1 is built with the triple-GEM technology.
The front-end electronics of the Muon detector is based on two custom chips: the CARIOCA (with a modified version for the GEM detector)and the DIALOG, both designed with the 0.25mm radiation tolerant technology.
The CARIOCA is a fast (about 10ns peaking time) and low-noise (ENC=2500e-+45e-*Cdet, where Cdet is the detector capacitance in pF, ranging from 15pF to 200pF in the Muon system) amplifier-shaper-discriminator chip, with an active baseline restoration circuit. A special version of it, named CARIOCA-GEM, was designed in order to read-out the triple-GEM detector, with a modified shaping stage not including the ion tail cancellation circuit.
The DIALOG chips takes care of the logical channel generation for the trigger and of the interaction with the slow control system, i.e. threshold setting and front-end monitoring.
The front-end boards house two CARIOCA chips and one DIALOG chips.
The experiment is now in the production phase of the front-end electronics, including 8,000 boards and the 24,000 chips.
The front-end chips and boards are being extensively tested in the lab and their interaction with grounding issues and power supply distribution of the chambers studied in detail.

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Session Classification: Parallel session B5

Contribution ID: **9** Type: **Oral**

End-Ladder Board for ALICE SDD Experiment

Thursday 15 September 2005 16:25 (25 minutes)

The paper presents an end-ladder card prototype of the data acquisition chain of the ALICE SDD experiment. The prototype includes most of the electronics devices that will be applied to ALICE SDD experiment. The card interfaces with the front-end electronics and with the counting room detector data link. It has been designed taking into account the constraints on the dimensions of the final apparatus. It has been fully tested within the data acquisition chain and, since the results were good,the final design for production is close to submission.

Summary

The paper explains the design and the construction of an end-ladder card prototype for the Silicon Drift Detector (SDD) experiment, part of the Inner Tracking System (ITS) of the A Large Ion Collider Experiment (ALICE). The end-ladder card interfaces with the Front-End Electronics (FEE) and elaborates and transmits the dataset received from the FEE through an optical channel to the counting room. The paper describes also the design of the tests that have been carried out on the Printed Circuit Board prototype.
The dataset that originate from the FEE enters the card through the Molex connectors and is read by CARLOS chip. This performs basically a bi-dimensional compression during the normal DAQ mode and works as a system JTAG switch during the FEE configuration. CARLOS reduces and packs the dataset and its outputs is serialized via the Gigabit Optical Link (GOL) serializer chip that interfaces, by means of an 800Mb/s link, with the laser diode. Finally, GOL serializes the dataset that is reconstructed within the Counting Room Emulator by a mirroring de-serializer device that output the data to the state analyzer instruments. As the GOL chip requires a low-jitter clock signal, as low as 50 ps, the QPLL clock filter chip has been applied. This locks the 40MHz clock signal, derived from one of the two pin-diodes, on a very-low-jitter 160 MHz crystal (XTAL). Then this frequencies is divided by four passed to the GOL and CARLOS chips. The chips are powered with a 2.5 V low-voltage regulator (LHC4913) that is configured for an overall current of 400 mA.
All the components embedded into the End-Ladder Prototype card are Application Specific Integrated Circuits (ASICs) designed to be radiation-tolerant to the total ionizing dose that is estimated (nearly 30 krad) for a 10-years of data-taking within the ALICE ITS environment.
The amount of data generated by the SDD originates from 2 half detectors for each CARLOS chip. As each half detector is composed of 256 anodes and, for each anode, 256 time samples are taken in order to cover the full drift (time) length, altogether each detector is able to generate a dataset made up of 256 × 256 data words. The two half detectors'dataset are read by the two channels of CARLOS chip. Thus, the readout electronics is composed of FEE boards, which collect data from the SDDs and End-Ladder boards that reduce, pack and serialize the dataset. Then this is sent to the counting room where it is reconstructed as it was transmitted.

To simulate the whole readout system a dedicated hardware and software test architecture has been designed. First, a pattern generator provides the input vectors that emulate the real SDD data. Second, the ALICE Detector Data Link system has been mounted in our laboratory to provide the FEE and the DUT cards with the necessary signals and controls as it were transmitted from the counting room. In this way we have designed a whole copy of the SDD readout system and, since that time, we have been able to emulate the data taking.

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Session Classification: Parallel session A6

Contribution ID: **11** Type: **Oral**

0.13 um CMOS technologies for analog front-end circuits in LHC detector upgrades

Tuesday 13 September 2005 09:45 (25 minutes)

Deep submicron CMOS technologies are widely used for the implementation of low noise front-end electronics in various detector applications. In this field the designers'effort is presently focused on 0.13 micron technologies. This work presents the results of noise measurements carried out on CMOS devices in 0.13 um commercial processes from different foundries. The study also includes an evaluation of the impact of high doses of ionizing radiation on the noise performances. Data obtained from the measurements provide a powerful tool to model noise parameters and establish design criteria in a 0.13 um CMOS process for detector front-ends in LHC upgrades.

Summary

Submicron CMOS technologies provide well-established solutions to the implementation of low noise front-end electronics for a wide range of detector applications. The advantages in the design of high performance mixed signal systems were exploited in recent years and led to the fabrication of integrated circuits in 0.35 um and 0.25 um CMOS processes. Following the trend of commercial silicon foundries, the IC designers'effort is gradually shifting to 0.13 um CMOS generations, to implement readout integrated circuits for silicon strip and pixel detectors, in view of future applications (LHC upgrades, Linear Collider, Super B-Factory). Furthermore, a beneficial side effect of CMOS scaling is that the technology becomes harder for every new generation. This observation is related to the thickness reduction of both the gate and isolation dielectric layers, making them less susceptible to ionization damage. However, it is very important to assess the impact of technology scaling on the noise parameters, which can be affected by gate oxide quality and short-channel phenomena. This can be very critical in applications such as LHC upgrades, where a very short signal shaping time is required because of high event rate, or where a thin silicon detector (100 um or less) is mandatory for material minimization or radiation hardness.

The MOSFETs studied in this paper belong to two commercial CMOS processes with minimum gate length of 0.13 um and manufactured by STMicroelectronics and IBM. The devices were characterized at drain currents from several tens of uA to 1 mA, that is, the usual operating currents of input devices in integrated charge-sensitive preamplifiers. In these conditions, deep submicron devices are biased in weak or moderate inversion. The behavior of the 1/f and white noise terms is studied as a function of the device polarity and of the gate length and width to account for different detector requirements. The analysis of the experimental results includes the comparison of PMOS and NMOS inside the 0.13 um CMOS generation considering devices from the two foundries.

In this study an evaluation of the impact of ionizing radiation on the analog performances is also reported and discussed. An interesting point is to verify if

standard open structure devices can be safely used in rad-hard circuits, without implementing any special radiation hard technique. Besides key parameters, such as the threshold voltage shift, a special attention is given to the beavior of white and 1/f components in the noise voltage spectrum. Experimental results point out that open structure devices in the examined 0.13 um technologies exhibit a large degree of tolerance to ionizing radiation. This may be exploited to remove geometry constraints and increase functional density.

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Session Classification: Plenary Session P2

Contribution ID: **12** Type: **Poster**

SWIFT: A Deskewing and Fault Tolerance Switch for LVDS Links

The device presented at this work is a switch designed for compensating the skew which affects parallel data signal transmissions and for providing fault tolerance in large scale scalable systems, for instance used in trigger farms for high energy physics experiments. The SWIFT chip (SWItch for Fault Tolerance)is part of a cluster built around commercially components which has been inspired by the LHCb experiment. The skew is extremely important because it directly affects the sample window available to the receiver logic and either forces to use quality and expensive cables in order to minimize its effects or reduces the maximum signal transmission range or distance. This problem is handled by the deskewing circuitry at the SWIFT chip, which is able to match dynamically the signal transitions at the receiver link by adding an individual delay to each input signal in steps of 100 ps for LVDS signals up to 250 MHz. A 16-bit processor is implemented for processing tasks. SWIFT has been implemented in a 0.35 microns CMOS process, compensates dynamically skews of LVDS signals up to 250 MHz in steps of maximum 100 ps, and adds fault tolerance in the farm of PCs by allowing the bypassing of a failing compute node to which is attached.

Summary

In this work alternative techniques to minimize the effects of the skew in point-to-point high frequency parallel data transmission over differential signaling are presented. Novel methods of deskewing circuitries and comparison with existing approaches were done. Based on the premises of minimizing the skew between the parallel signals down to 100 ps, performing a self calibration of the skew in the receiver link, and having the possibility to bypass a broken link adding fault tolerance in order to do not disturb the data flow, an interface VLSI called SWIFT compatible with any interconnection technology working at high frequency speeds is designed in 0.35 μm CMOS process, implemented and satisfactory tested.

The architecture of the SWIFT chip developed is described. The bypass function in SWIFT is implemented in a component which is snooping continuously the clock signal, being received from the host (compute node, NIC, etc.) to which the chip is attached. The deskew function is implemented by observing the timing transitions on each data line relative to the received clock signal. Therefore the delays on each line can be adjusted individually in order to optimize the sampling time relative to the received clock. A fundamental part of the design is based on programmable delay units capable to produce delays of 100 ps granularity. Since the skew which must be compensated is a priori unknown and it changes randomly, a self calibration skew circuitry is designed. An embedded processor is implemented in the chip for adding versatility to the design. Analog and VHDL simulations of the entire placed and routed chip are presented and discussed together with a description of the mixed analogue and digital design flow of SWIFT, which was developed for the 0.35 μm CMOS process used. The results of the SWIFT testing and the comparison with those existing from simulations are presented. The programmable delay units work as expected producing delay steps of maximum 100 ps in a dynamic range of 2.75 ns. The deskew function of SWIFT (dynamic and static mode) is verified and examples of skew

compensations down to 125 ps are shown. The bypass function of SWIFT is working correctly. Extensive measurements results are presented, compared with simulated ones, and discussed. The results show the feasibility of SWIFT under voltage variations. The 16-bit processor is verified during the test procedure.

The chip implemented is used to theoretically improve the performances of a real system as for example the trigger farm developed at KIP as a part of the data acquisition system of a high energy physics experiment as the LHCb (Large Hadron Collider Beauty) at CERN. It is feasible to significantly improve the performances of such systems using the SWIFT chip as interface between the interconnect network and the compute node of the farm. The positive results can in general be applied to any point-to-point based system with ringlet as the basic element, which transmits parallel signals between the hosts over differential signaling, and with large amount of data transferred at high frequency speeds.

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Track Classification: Custom Integrated Circuits

Contribution ID: **13** Type: **Oral**

Implementation and Test of the First-Level Global Muon Trigger of the CMS Experiment

Tuesday 13 September 2005 12:15 (25 minutes)

In CMS, three independent first-level muon trigger systems identify muon candidate tracks. The Global Muon Trigger (GMT) receives up to 16 candidate tracks and combines them using algorithms exploiting the complementarity of the muon systems. The GMT also correlates the muon candidate tracks with calorimeter regions in order to determine muon isolation or confirmation by the calorimeter. The top four muon candidates are forwarded to the Global Trigger. The GMT algorithms are implemented in ten Xilinx Virtex-II FPGAs on a single 9U-VME board. The development of the VME board and its firmware as well as the results of system and integration tests are presented.

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Session Classification: Parallel session B1

Contribution ID: **14** Type: **Oral**

ATLAS DAQ/HLT infrastructure

Thursday 15 September 2005 11:00 (25 minutes)

The ATLAS DAQ/HLT equipment is located in the underground counting room and in the surface building. The main active components are rack-mounted PC's and switches. The issues being resolved during the engineering design are powering and cooling of the DAQ/HLT equipment, monitoring of the environmental parameters, installation and maintenance procedures. This paper describes the ongoing activities and presents the proposed solutions.

Summary

The ATLAS DAQ/HLT system handles data coming in parallel from the detector. The readout system, located in the underground counting room, and the computing farm, located in the surface building are both based on rack-mounted PC's and network switches. They are now entering the installation stage and therefore need an operational infrastructure. It includes counting rooms design, rack selection, supply of electrical power from the distribution network and UPS, as well as cooling of the equipment and monitoring of the environmental parameters.
The engineering design of the infrastructure is a common activity of ATLAS DAQ/HLT and Technical Coordination together with CERN Technical Support division. The task of the DAQ/HLT is to define their specific requirements and to find a common solutions within DAQ/HLT and with other experiments and Information Technology division. The example is the LHC PC rack project which lead to a common water-cooling solution for the horizontal air flow inside the racks. For the power distribution, the DAQ/HLT formulated their requirements, supplied the Technical Coordination with results of preliminary studies and working together towards the most cost effective final design. The implementation of the monitoring of the environmental parameters is a full responsibility of the DAQ/HLT. We are aiming to have a single coherent management and monitoring tool based on IPMI, Linux tools and standard tools developed for the ATLAS Detector Control System and integrated into overall operation of the experiment. Installation and maintenance procedure of the DAQ/HLT equipment is supported by the Rack Wizard - a graphical interface for electronics configuration and cabling databases.

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Session Classification: Parallel session B4

Contribution ID: **15** Type: **Oral**

The 0.25um Token Bit Manager for CMS Pixel Readout

Tuesday 13 September 2005 11:50 (25 minutes)

To coordinate groupings of pixel readout chips, the Token Bit Manager (TBM), has been developed for the CMS experiment.

The TBM will coordinate passing of the readout token around a group readout chips (ROC). In addition it supplies the DAQ with a header and trailer record to facilitate event recognition.

Also present on the same chip is a Control Network Hub, which directs control commands to the TBM, as well as the ROC.

The Latest design details, and resent performance measurements will be presented, including the results of radiation and low temperature testing.

Summary

An intelligent coordinator for the readout of groupings of pixel readout chips, the Token Bit Manager (TBM), has been developed for the CMS experiment at LHC. To reduce readout dead time, the TBM needs to be located as close as possible to the readout chips. This forces developing this electronics in a rad-hard process.

Implied by its name, the Token Bit Manager will coordinate passing of the readout token around a group of from 8 to 24 readout chips. Each arriving Level 1 trigger will be assigned an 8 bit event number and 8-bits of error status. This information will be placed on a 32 event deep stack awaiting its associated token pass. This data will be supplied to the DAQ along with header, and trailer ID's as wrapper to the combined readout chip analog encoded data stream, to facilitate event recognition, and alert the DAQ of problems in the readout chain.

Also present on the same rad-hard chip is a Communication Control Hub, implemented with a 40 Mhz, differential, serial protocol similar in struction to I2c. This protocol will be used to provide command structures and parameter modifications for the TBM itself as well as for all readout chips. The procedure and timing constraints for setting and refreshing some 30M pixel trim settings will also be presented.

Several test results from resent submissions in 0.25u will be presented. These include radiation and low temperature testing, as well as results of using the TBM as the core of the control hardware for the Forward Pixel testbeam.

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Session Classification: Parallel session A1

Contribution ID: **16** Type: **Oral**

Final Results of the Industrial Production of CMS Tracker Analog Optohybrids

Tuesday 13 September 2005 15:30 (25 minutes)

Approximately 15,000 analog optical transmitter modules with 2 or 3 channels each will be installed in the CMS experiment to read out the Silicon Strip Tracker. These Analog Optohybrids were produced in Austrian and Italian industries from mid-2003 to mid-2005.

After assembly, each unit was thoroughly tested for electrical and optical properties and all results are stored in the CMS Tracker database, which allows a wide range of statistical analyses. We will discuss statistical distributions of important parameters and their impact on the system.

Among minor issues, three significant problems occurred during the industrial production. Those will be described together with the corrective actions taken and the lessons learned.

Summary

The main components of the CMS Tracker Analog Optohybrids are pigtailed laser diodes and the Linear Laser Driver ASIC, which allows flexible adjustments for gain and bias current of each channel such that sample spread as well as temperature and radiation effects can be compensated.

The production of optohybrids is exceptional to industry for several facts. First of all, the number of units is rather small and hence does not allow cost-effective automation such that a high degree of manuallabor is involved. Nevertheless, specialized equipment like a bonding station and non-standard optical devices are required. Thus, particular care was taken when selecting potential manufacturers and prototyping was started with promising candidates to get an impression of their abilities. Finally, the contract was mainly awarded according to this experience, since all bids were quite similar.

Despite all precautions, three major problems appeared unexpectedly during the series production. First of all, the package of the Linear Laser Driver ASIC slightly changed but unfortunately caused shorts on some optohybrids. Since this happened soon after starting the production, it was decided not to attempt repair or workaround procedures but rather re-design the PCB to avoid such potential shorts.

A few months later it turned out that the chosen fiber buffer can develop small cracks and ruptures which do not affect functionality but carry a mechanical risk in the long term. Several investigations were performed and finally, three actions were taken: The buffer type was changed from acrylate to polyethylene which does not show such ruptures.
Because of the staged pipeline production process, more than 5000 optohybrids were still to be equipped with the old fiber type. Hence, each fiber was visually inspected prior to assembly and the glue curing temperature was lowered to the minimum possible value which yielded fewer buffer ruptures.

After a third of the Austrian production was completed, it was discovered that the company had used other SMD capacitors than specified for all optohybrids produced

so far. The assembled type was not tested for radiation tolerance. Thus, the production was halted and a re-qualification was performed in comparison to the previously specified brand, comprising characterization before, between and after gamma and proton irradiations at high statistics. Fortunately it turned out that the used type was equally suitable as the one originally specified and manufacturing was resumed without change.

During the whole production and those problems in particular, we recognized the importance of keeping close contact to the company, and geographical proximity turned out to considerably ease such matters.

Since the production will be finished in mid-2005, we can extract statistical properties from the complete data set as stored in the database. The electrical to optical gain is the key figure since it needs tuning for each channel. Values should be as close as possible to the target gain while retaining headroom for the Laser Driver settings to account for individual adjustments and radiation effects.

Moreover, the power consumption, depending on the accumulated radiation level, can be predicted from bias and supply current statistics. Other properties such as the analog bandwidth are achieved by design; yet the spread and shape of such distributions give an indication of quality and uniformity of the devices.

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Presenter: Dr FRIEDL, Markus (HEPHY Vienna)

Session Classification: Parallel session B2

Contribution ID: **17** Type: **Oral**

Concept, realization and characterization of serially powered pixel modules

Thursday 15 September 2005 12:15 (25 minutes)

We demonstrate here for the example of the large scale pixel detector of ATLAS that Serial Powering of pixel modules is a viable alternative powering scheme that have been devised and implemented for the modules using dedicated on-chip voltage regulators and modified flex hybrid circuits. The equivalent of a pixel ladder consisting of six serially powered pixel modules with about 0.3 Mpixels has been built and the performance with respect to noise and threshold stability and operation
failures has been studied. We believe that Serial Powering in general will be necessary for future large scale tracking detectors.

Summary

Large scale and high granularity tracking detectors are usually built from many identical modules which operate individually. Such modules can then be optimized in performance and power consumption. The usual scheme of parallel powering every module
with a constant voltage is disadvantageous for the performance of the detector as a whole. Above a certain granularity the power losses in the cables easily exceed the actual power consumption of the modules, especially if the readout chips need a low supply voltage, but have a high power density at the same time.
Moreover a vast amount of cables is needed to power such a large scale detector. The cables are in the way of the particles that are tracked and lower the originally optimized performance of the module and of all following detectors.
For the LHC experiments this already now is a major problem for the optimal performance of the detectors and it has become evident, that for an upgrade program alternative powering schemes must be investigated.

We prove and demonstrate here for the example of the large scale pixel detector of ATLAS that Serial Powering of pixel modules is a viable alternative. A powering scheme that powers a chain of modules with a constant current and uses dedicated on-chip voltage regulators and modified flex hybrid circuits has been devised and implemented for ATLAS pixel modules.
The implementation of Serial Powering is the serial connection of a ladder of 13 modules. An example calculation shows that such a chain of 13 modules offers a reduction in power losses of the cables by 90% and a reduction in passive materials by 98%, this is a reduction of 85% in radiation length.
Prior to building serially powered modules the characteristics of the voltage regulators, namely shunt and linear regulators, as the key elements to this powering scheme were measured on over 250 chips of a current production wafer. It has been shown that the spread in quality is small and the voltage stability of the linear regulators is excellent, so that the voltage regulators are applicable for Serial Powering.
The serially powered modules have been intensively tested in the lab and in test

beams. The comparison between parallely powered and serially powered modules with respect to noise and threshold stability performance have shown no difference between the two powering schemes. Finally the equivalent of a pixel ladder consisting of six serially powered pixel modules with about 0.3 Mpixels has been built and the performance with respect to operation failures has been studied. The major objection against Serial Powering is the possible noise pickup by modules through the power lines. Measurements with artificially noisy modules mimicked by inducing noise on the power lines have only shown a marginal increase in noise of the other modules in the chain. We therefore strongly believe that Serial Powering is not only a viable powering scheme for an upcoming upgrade of the ATLAS pixel detector, but is also viable, if not absolutely necessary for future large scale tracking detectors. The presentation will show the scheme, the design of the necessary components and the measurements.

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Session Classification: Parallel session A4

Contribution ID: **19** Type: **Oral**

Radiation-Hard Optical Link for the ATLAS Pixel Detector

Tuesday 13 September 2005 14:40 (25 minutes)

We have developed a radiation-hard optical link for the ATLAS pixel detector at the LHC at CERN. The driver and receiver chips are implemented in 0.25 micron CMOS technology using enclosed layout transistors and guard rings for increased radiation hardness. The former drives the Vertical Cavity Surface Emitting Laser (VCSEL) diode to transmit 80 Mbit/s data from the detector. The latter decodes the Bi-Phase Marked signal received optically by a PIN diode to recover the control data and 40 MHz clock. The chips and optical devices are mounted on a hybrid circuit board, opto-board. We present the experience from the production of the opto-boards together with results from the the irradiation studies with 24 GeV protons up to a total dose of 32 Mrad. In addition, we will present some results from the simulation of the upgrade versions of the chips operating at Gbit/s for the SuperLHC.

Summary

The ATLAS pixel detector consists of two barrel layers and two forward and backward disks which provide at least two space point measurements.
The low voltage differential signal (LVDS) from the pixel detector is converted by the VCSEL Driver Chip (VDC) into a single-ended signal appropriate to drive a Vertical Cavity Surface Emitting Laser (VCSEL).
The resulting optical signal is transmitted to the Readout Device (ROD)via a fibre.
The 40 MHz beam crossing clock from the ROD, bi-phase mark encoded with command signals to control the pixel detector, is transmitted via a fibre to a PIN diode.
This signal is decoded using a Digital Opto-Receiver Integrated Circuit (DORIC).
The PIN and VCSEL are packaged in the so-called opto-packs for connecting to the chips and fibers.

We implement the VDC and DORIC circuits in standard deep submicron (0.25 micron) CMOS technology. Employing enclosed layout transistors and guard rings, this technology promises to be very radiation hard.
After five prototype runs, the chips meet the ATLAS specifications,including the radiation hardness requirements.

The chips together with the optical devices are mounted on a hybrid circuit board, opto-board. The board uses BeO as the substrate for heat management. We are currently producing the 300 opto-boards needed for the pixel detector. The micro-soldering of the leads of the opto-packs is a particular challenge and we will present this along with other production experience.

In June 2004, we irradiated the production opto-boards with 24 GeV protons at CERN up to a dosage of 32 Mrad. We observed no significant degradation of chips and the VCSEL still produces quite adequate power after the irradiation. The results indicate that the optical link meets the radiation hardness requirements for the ATLAS pixel detector.

We are also in the process of converting the VDC and DORIC to operate at Gbit/s with 0.13 micron technology for the Super-LHC. Some preliminary results from the

conversions will be presented.

In summary, we have developed an opto-link that meets all the requirements for operation in the ATLAS pixel optical link. The link is expected to be sufficiently radiation hard for ten years of operation at the LHC. We are also in the process of converting the chips to operate at much higher speed for the Super-LHC.

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Session Classification: Parallel session B2

Contribution ID: **21** Type: **Oral**

A High Voltage System with 60 High Voltage Power Supply Channels in 2U Height EURO Crate

Thursday 15 September 2005 11:50 (25 minutes)

A high voltage system includes 60 high voltage power supply channels in a 2U height EURO crate. The system is interfaced with a computer through USB interface. The output voltage of the channel ranges from 1 kV to 4 kV with an output current of more than 100 uA. Ripples on the output voltage is less than 100 mV in peak-to-peak amplitude. The output voltage can be set and monitored with 1 V resolution. The output current is monitored with 9-bit resolution at the sampling rate of 80 Hz. The channel is provided with over-current shut-down. A hardwired logic turns off the output voltage when the output current exceeds a prescribed limit current in a predefined time interval, where the limit current and the time interval can be set by the computer. Since high voltage is generated by a ceramic transformer, the system can be operated in a magnetic field of 1 T. The high voltage system satisfies the CERN Radiation Hard Criteria required for TGC power supplies.

Summary

A high voltage system includes 60 high voltage power supply channels in a 2U height EURO crate. The system is composed of 20 high voltage (HV) card and an interface card, where the interface card is located at the 21-th slot. Three high voltage power supply channels are implemented on the HV card with control logic. A back-plane bus is shared among the cards for communication and voltage distribution.

A ceramic transformer is utilized to generate high voltage in the channel. The high voltage is rectified to be the output voltage. A driver circuit generates a carrier to drive the ceramic transformer. The HV card is supplied with 3.5 V and ±5V. The driver circuit is supplied with 3.5 V. An analog circuit to stabilize the output voltage is powered by ±5V. The control logic on the HV card is mostly digital logic electrified by 5 V. The system is supplied in total with 40 A of 3.5 V, 20 A of 5 V and 1 A of -5 V.

The interface card is equipped with USB interface, and the high voltage system is connected to a computer by a USB cable. The channel can supply the output voltage ranging from 1 kV to 4 kV with a load of larger than 30 Megohms. Ripples on the output voltage is less than 100 mV in peak-to-peak amplitude. The output voltage can be set and monitored with 1 V resolution. The output current is monitored with 9-bit resolution at the sampling rate of 80 Hz. The channel is provided with over-current shut-down. A hardwired logic turns off the output voltage when the output current exceeds a prescribed limit current in a predefined time interval, where the limit current and the time interval can be set by the computer.

The ceramic transformer takes the place of the conventional magnetic transformer. The ceramic transformer utilizes piezoelectric effect to generate high voltage. The ceramic transformer is constructed from a ceramic bar and does not include any magnetic material. So the transformer is free of leakage of magnetic flux and can be operated efficiently under a magnetic field. The high voltage system can work without a loss of efficiency under a magnetic field of 1 T.

The HV cards have been irradiated by cobalt 60 up to 300 krad successfully. The HV

cards have been exposed to a protons flux at PSI. The exposure amounts 60 MeV 1E11 protons without causing problems. The exposure is equivalent to 1E11 neutrons and 14 krad. So the radiation test shows the HV card and then the high voltage system satisfies CERN Radiation Hard Criteria required for TGC power supplies.

The high voltage system is now used in a beam test of TGC in CERN. The high voltage system is now put to final cost reduction. The price is not yet settled, while the design goal of the price is targeted between 100 euros and dollars per channel.

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Session Classification: Parallel session B4

Contribution ID: **22** Type: **Poster**

A Silicon Strips Detector Readout Prototype Chip in 180 nanometer CMOS Technology

A 16-channel readout chip for Silicon strips detectors has been designed in 180 nanometer CMOS technology and tested. It includes low-noise amplification, pulse shaping, sampling and threshold detection. An input referred noise of 190 + 12 electrons/picoFarad for an integration time of 3 microseconds has been measured, leading to an overall signal to noise ratio of 30 and a dynamic range of 75 Minimum Ionizing Particles at +/- 1.5 linearity, for a 60 centimeter long strip. Power dissipation is 350 microWatt per channel, area is 0.05 square millimeter.

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Contribution ID: **23** Type: **Poster**

A real time electronic emulator with realistic data generation for reception tests of the CMS ECAL front-end boards.

The electromagnetic calorimeter (ECAL) of the CMS experiment is equipped with ˜3000 front-end boards (FE) performing both trigger and data readout functions. Prior to their integration at CERN in the ECAL detectors the FE boards are tested using a dedicated test bench located in Laboratoire Leprince-Ringuet. This test bench, called XFEST, was designed and built for testing as much as 12 FE boards at the same time. The tests are performed by injecting the same digital input patterns with a 40 MHz rate on the 12 FE boards and by comparing their 24 output signals. Failures in the behavior of bad FE boards are signalled by different output signals from those of a reference FE board. This contribution describes the solution developed in order to create a real time emulator of realistic digital input patterns at 40 MHz rate as well as the implementation of a real time comparison of the 12 FE boards output streams.

Summary

Each ECAL front-end board receives 25 digital signals of 14 bit at a 40 MHz clock frequency from the very front-end electronics (VFE). These signals are processed by seven dedicated asics called FENIX. In order to emulate the 25 digital input vectors a prototype version of the FE board equipped with commercial programmable circuits in place of the FENIX asics has been used. This board called EF is installed on a motherboard designed and developed at LLR. The main role of this motherboard is to insure the duplication of the 25 digital signals in order to feed four FE boards. There are three motherboards in total each one equipped with one EF board in order to test at the same time 12 FE boards. The output digital signals of the four FE under tests are shipped by optical fibers to a prototype of the Trigger and Concentrator Card (TCC) in the same way as the final ECAL lectronics. The TCC is also equipped with commercial programmable circuits. In order to perform the real time comparison between the FE output signals the TCC firmware has been modified.

- For the 25 VFE signal's emulators, the analogue shape and the pileup characteristics of these signals have been implemented. Noises and pedestals are digitally emulated, the trigger occurrence distribution and energy amplitude are randomly generated according to pseudo Gaussian distributions. Amplitude gains, energy range, level of noise or pedestals are all programmable via an integrated I2C interface.
These capabilities imply a great flexibility and very efficient way to tune specific parameters.
- For the comparison system, the main issue is to aggregate and compare in a same clock domain all data from different clock time buckets. The real time computing of all input data is a key point to solve buffer control problems. Parameters setup like reference card selection is possible with an embedded VME interface. Diagnostic and error counting are included in the design.

This presentation will describe a solution to efficiently test a large set of complex electronic cards with many input ports and high throughput data rate. Algorithm to emulate the VFE signals is embedded in field gate programmable array circuits. The test bench will also be presented.

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Contribution ID: **24** Type: **Oral**

CMS ECAL Front-End boards: the XFEST project

Thursday 15 September 2005 14:50 (25 minutes)

The Front-End (FE) boards are part of the on-detector electronics system of the CMS electromagnetic calorimeter ECAL. Their numerical functionalities and properties are tested by a dedicated test bench located at Laboratoire Leprince-Ringuet, prior to the board integration in the CMS detector at CERN. XFEST, acronym for eXtended Front-End System Test, is designed to perform tests that can last several hours, on up to 12 FE boards in parallel. The system is foreseen to deliver 80 tested boards per week. This contribution presents the XFEST set-up and the results of the measurements on FE boards.

Summary

XFEST is a test bench designed to control the FE boards production after the burn-in phase. Its basic idea is to inject realistic 14-bits digital patterns into several boards in parallel at a 40 MHz clock frequency and to compare their outputs to the ones of a “reference”.

XFEST is organized in three main subsystems:
- The pattern generator used to inject the signals to the FE boards is an old prototype of FE board working in a reverse mode (producing 25 outputs in place of inputs), in which FPGAs have been reprogrammed for this purpose (more details are given by another contribution to this conference).
- The data corresponding to 25 channels are then distributed to four FE boards positioned on a XFEST motherboard. The different boards are linked through a token ring, providing the clock and the trigger information. In order to test a large number of FE boards during a sufficient time (10ˆ12 different patterns are compared per hour), we consider for the final production test the possibility to use three motherboards.
- The two optical outputs (trigger and data streams) of the FE boards are sent to the TCC-24 board, which is a prototype of the Trigger Concentrator Card (TCC) developed at Laboratoire Leprince-Ringuet. This prototype used as a comparator for this project can treat 2x12 input channels, which allows to test up to 12 FE boards simultaneously. Any discrepancy at the bit level between one or several boards and the reference increments the error counters.

A user web interface allows the control of the whole test bench. In a first phase, the results of the TCC comparisons are checked with ChipScope; in a second phase, it will be done via a VME interface.

This contribution will describe the system and report the results of the measurements as well as mention the encountered problems.

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Presenter: COLLARD, Caroline (LLR Ecole Polytechnique)

Session Classification: Parallel session A5

Contribution ID: **25** Type: **Oral**

Performance of CMS pixel detector barrel modules

Thursday 15 September 2005 11:25 (25 minutes)

The central part of the CMS pixel detector will consist of about 800 modules, which are mounted on three concentric barrel layers. The radii of the layers are 4cm, 7cm and 11cm. The modules cover an area of 66.5mm * 18.5mm and have 66560 pixels. The 16 Read Out Chips are connected to the sensor by bump bonds.
The performance of the prototype modules has been evaluated in detail in the laboratory. Furthermore there will be a high rate testbeam at PSI to validate the performance of the module exposed to a particle rate comparable to LHC conditions. The results of the measurements from the laboratory and from the high rate testbeam will be shown.

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Session Classification: Parallel session A4

Contribution ID: **26** Type: **Oral**

SPD Very Front End Electronics

Thursday 15 September 2005 17:15 (25 minutes)

The SPD (Scintillator Pad Detector) is a part of LHCb calorimetry. Its function is to discriminate between charged particles and neutrals for the LHCb level0 trigger. This detector uses scintillator pad readout by wavelength shifting (WLS) fibbers that are coupled to MAPMT via clear plastic fibbers. The specific features of the SPD detector are the high granularity in the inner part of the detector, and the use of 64-channel photomultiplier tubes with small pixel dimension. The choice of a MAPMT allowed to design a fast, multi-channel pad detector with a reduced cost per channel..

The signal outing the SPD PMTs has large fluctuations in the signal pulse shape since the average of photoelectrons is only about 20-30 due to the response of the WLS fibre, which has low decay time. This fact causes another bothering trouble: the potential tail of a high amplitude event could cross the threshold and provoke a fake trigger. Thus, pile-up correction is needed.

SPD Readout system is performed by an specific ASIC which integrates the signal, makes the pile-up compensation, and compares the level obtained to a programmable threshold (distinguish electrons and photons), an FPGA which programmes the ASIC threshold and pile-up subtraction and finally LVDS serializers, in order to send information to the first level trigger system.

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Session Classification: Parallel session A6

Contribution ID: **27** Type: **Poster**

Performance of the Bandgap Reference Circuit, designed in a commercial 0.13um CMOS technology.

A new all-MOS bandgap voltage reference circuit has been developed and implemented in a commercial 0.13-μm CMOS technology. The proposed circuit features dynamic-threshold MOS transistors (DTMOST's) and therefore well fits into the low supply-voltage range of the technology.
Measured Vref is 425±15mV (chip-to-chip statistical spread) for 8 samples. The circuit runs at supply voltages down to 0.85V and occupies 0.015mm2 on the wafer.
The X-ray irradiation facility has been used to examine radiation hardness of the circuit. When being irradiated up to 47 Mrad the reference voltage of the circuit shifts typically by 12mV.

Summary

Analog blocks are mandatory parts of today's CMOS ASICs used in high energy physics experiments. Such the blocks like supply voltage regulators, high quality ADCs and DACs include a reference circuit. The common way to implement reference circuit with a low temperature sensitivity and high power supply ripple rejection is the bandgap reference circuit.
With steadily decreasing power supply voltages (Vdd) in present and future deep sub-micron CMOS technologies a design of any bandgap voltage/current reference on-chip becomes a non-trivial task.
The classical voltage summing bandgap reference circuit (BGR) featuring parasitic diodes (p-diffusion in N-well) is not suited for a 0.13μm CMOS technology with a maximum Vdd of 1.2V. It is so because the value of bandgap voltage (Vgap) in silicon (1.12V) turns out to be very close to the nominal supply voltage of the process.
This causes the circuit to fail.
We use a new structure called a dynamic-threshold MOS transistor (DTMOST) in place of conventional diodes in the circuit. Such a combination constitutes a high-quality reference circuit able to fit into the reduced supply voltage range of a 0.13μm CMOS technology.
In order to construct a model of the DTMOST device suitable to run simulations, pre-design characterizations have been carried out.
The circuit has been submitted in CuTe2 MPW submit in May 2004.
Testing has shown that the measured performance of the circuit is in good agreement with the performance predicted by simulations.
The circuit is able to operate at supply voltage in range from 1.4V down to 0.85V.
Sensitivity of the reference voltage to the power supple voltage variation is 3.3mV/V.
The circuit can be externally trimmed in order to reach the operating point where the reference voltage has the lowest temperature coefficient (less than 1mV in the range from 0°C up to 80°C). However, due to statistical variation the trimming is dedicated to the chip. With no trimming the temperature coefficient is typical 0.05mV/°C.
The circuit will operate in the radiation environment of high energy physics

experiments and therefore radiation tolerance is an issue for the design. We used the CERN's in-house X-ray facility for the irradiation of the chips. The effect caused by irradiation consists in the shift of the reference voltage while the circuit remains fully operational.
The change of the reference voltage has been monitored in the time of the irradiation. We tested 5 chips and have seen that the reference voltage does not demonstrate an identical behaviour. The only thing to conclude is that the reference voltage deviates in the range of ± 12mV. It indicates that the irradiation is the dominant factor of instability of the reference voltage.
In some applications not only stability of the reference voltage is important but its absolute value as well. The absolute value differs from chip to chip and is caused by fabrication process variation. With few samples available we can roughly estimates chip-to-chip spread of the value of the reference voltage. It turned out to be confined in the range of ± 15mV.
A commercial 0.13um CMOS technology is suitable to design a high quality bandgap voltage reference circuit in spite of a low power supply voltage.
Redesign of the circuit is needed in order to improve chip-to-chip spread of absolute value of the reference voltage as well as its sensitivity to irradiation.

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Presenter: GROMOV, Vladimir (NIKHEF)

Contribution ID: **28** Type: **Oral**

The Production of the SCT Optical Links

Tuesday 13 September 2005 15:05 (25 minutes)

The on detector optical links for the SCT have been produced and mounted on the detector. Most of the off-detector opto-electronics has also been produced and has been used to successfully read out modules assembled on barrels and End Cap disks. Many problems were encountered during the production and these will be described. The lack of modularity in the system design has been a major disadvantage and some suggestions for a simpler and more modular system for the optical links for an upgraded tracker at the SLHC will be discussed.

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Session Classification: Parallel session B2

Contribution ID: **29** Type: **Poster**

ALICE HLT-RORC with Xilinx Virtex4

The ALICE HLT-RORC, a FPGA based PCI card, will be the link between the front-end electronics of the detector and the Front-End processors in the High Level Trigger.
Equipped with the new Xilinx Virtex4 LX40 FPGA a fast PCI 64/66 interface and up to two optical links the card will not only be able to inject the raw detector data into the memory of the Trigger farm, it also provides the possibility of processing the raw data "on the fly"inside the FPGA. A fast clusterfinder algorithm in hardware already exists and a Hough tracker is currently under development.

Summary

Three years ago, a first iteration of the HLT-RORC has been successfully developed to explore the possibilities of an FPGA based PCI card as both a receiver card for the raw data coming from the detector and an online processor for processing the raw data. Each RORC was able to hold one optical link to receive the data and sending it via the PCI bus directly into the main memory of the Front-End processors, the first stage of an online reconstruction framework called High Level Trigger. The concept has proven to work in various internal tests as well as in the TPC Front-End electronics integration tests in April 2004 at CERN.
In parallel two approaches for online processing on the card has been investigated. One is a fast clusterfinder for the TPC based on the offline algorithm; the second is a Hough tracker for the TPC. Both algorithms were adapted to the requirements of FPGA based computation, means additions, multiplications and Look-Up tables. It has shown that the cluster finding can be done completely inside the FPGA while the Hough tracker requires Look-Up tables stored in an external memory device.
These results together with the latest improvements in the FPGA technologies made it obvious to redesign the first version of the HLT-RORC. The choice of the device for the new card, a Xilinx Virtex4 LX40, reflects the experience made within the last three years. The LX family provides a large number of I/Os which makes it possible to implement a PCI 64/66 interface, two optical links and four independent banks of fast DDR-SDRAM on the new card. The four independent banks, each 16bit wide, can be used combined or separately thus allowing it to have several Hough tracker in parallel, each with its own Look-Up tables in one bank.
In addition to the large number of I/Os, the LX40 has 64 internal digital processing units, the DSP slices, Each DSP implements a 18x18 multiplier combined with a 48bit accumulator capable of running with up to 500MHz and will replace the old combinatorial arithmetic in the clusterfinder and in the future Hough tracker thus giving a considerable improvement in processing power. To take into account that future upgrades or algorithms may require a reconfiguration of the card or exchange of information between the cards, a smart configuration scheme and a fast serial link between the cards will be implemented.
This configuration scheme is based on an onboard flash and a small CPLD and will allow configuring the card remotely over PCI even in case that the current design

in the FPGA is corrupted and the connection via PCI will be lost.

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Track Classification: Programmable Logic and Embedded Processing

Contribution ID: **30** Type: **Oral**

Irradiation Studies of the ATLAS Inner Detector Opto-Electronic Readout System for SLHC

Tuesday 13 September 2005 16:25 (25 minutes)

The readout system of the ATLAS inner detector for SLHC will need to cope with ten time's higher radiation doses than the current ATLAS inner detector readout system. It is an open question of whether the current opto-electronic readout system could be used at SLHC. This is a critical question for the detector design as it will have a major influence on the layout of the readout. We have started to irradiate VCSEL lasers, PIN diodes and optical fibres up to the levels expected at SLHC and are measuring the device-performances. The results of these irradiations tests are summarized.

Summary

Plans are being formulated at CERN for a luminosity upgrade to the Large Hadron Collider (LHC) machine. The LHC upgrade (SLHC) is being designed to increase the luminosity from 1034cm-2s-1 to 1035cm-2s-1. The expected time-scale would be around year 2015. The fluences at the SLHC will be 10 times higher than at LHC. For radii greater than 20 cm the expected fluence is 1015 hadrons/cm2. It is not clear, if the current opto-electronic components of the inner detector readout system are able to cope with this challenging radiation environment of SLHC.
Previous radiation tests have shown that the opto-electronic components (VCSEL lasers, PIN diodes and optical fibres) can survive 10 years of LHC operation. Radiation tests by the ATLAS Pixel detector group have demonstrated that these components can survive fluences and doses up to a factor of two higher than the SCT values.
Therefore there is an open question of whether this type of opto-electronics could be used on the upgraded SCT detector at the SLHC. This is a critical question for the design of this detector as it will have a major influence on the layout of all the readout services and therefore needs to be answered before the detector design can advance very far.
We are presenting the results of irradiation tests of Truelight VCSEL lasers, Centronic PIN-diodes, and SIMM fibres up to SLHC fluences.
Our previous radiation tests have shown that VCSELs and PIN diodes suffer from bulk damage but are insensitive to surface charge effects. These tests have also demonstrated good agreement with the NIEL scaling hypothesis. Hence, the first irradiation tests for SLHC we plan to be perform at the Ljubljana neutron reactor using NIEL scaling as a first step. We intend to confirm these results with other beams in the future.
For the irradiation studies of VCSEL lasers we are planning to have several cycles of irradiation and annealing as we had demonstrated that nearly full recovery of the VCSEL performance can be achieved with injection annealing (i.e. running the VCSELs with a DC current of 10 to 20 mA).
The radiation damage mechanism in fibre is due to creation of "colour centres"in

the electronic levels of the molecules. This is then only sensitive to ionising dose, so can be most conveniently studied with a gamma source. We need a high dose rate gamma source and a large area source to give a uniform dose over the sample. A suitable facility is the INER in Taiwan, which we will use to irradiated the fibres up to 100 Mrad. We will determine the induced attenuation of the fibres during irradiation.
We are presenting in this paper the results of the irradiation tests of the VCSEL lasers, PIN diodes and fibres up to SLHC doses and show the performance degradation of these devices as function of radiation dose.
In the future we intend also to determine SEU cross section of the GOL driver chip and QPLL chip while operating them at 1.6 GBits/sec.

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Session Classification: Parallel session B3

Contribution ID: **31** Type: **Poster**

Maximizing the Bandwidth Efficiency of the CMS Tracker Readout Optical Links for Super LHC

The maximum attainable data rate in a digital readout system based on the current CMS Tracker optical link components is investigated. Additional digital modulation and demodulation on either side of the current analog link would be required for implementation. The feasibility of such a conversion is explored in terms of performance that can be achieved and implementation complexity. Several bandwidth-efficient digital modulation schemes together with bit error rate (BER) reducing techniques are considered. The results from a simulation that includes a realistic model of the physical characteristics of the current components are presented.

Summary

Approximately 40 000 analog readout optical links are being installed in the CMS Tracker sub-detector for operation in the LHC. The next iteration of the CMS Tracker will be operated in the Super LHC (SLHC), and will have to cope with significantly increased data rates due to the tenfold increase in luminosity that is foreseen. In contrast to the telecom industry where the optical fiber and its installation drive the cost of a transmission system, it is the cost of the optoelectronic components that represents a large fraction of the CMS Tracker electronics budget. Hence, a digital system based on the existing components that can deliver sufficient performance for SLHC operation, if feasible, could potentially yield significant financial savings.

Historically, optical transmission systems employ simple binary digital, or on-off keying (OOK), schemes due to the large bandwidth available in optical fiber. In contrast, fast transmission through wireless and copper-based communication channels which are severely band-limited requires modulation techniques that are more bandwidth-efficient. Research into multi-level signaling for optical systems is a relatively recent subject of research, prompted by the desire to reach even higher data rates.

The current CMS Tracker optical readout links are equivalent to a digital system capable of pulse amplitude modulation (PAM) at 40MS/s with 8bit resolution (=320Mbps). The excellent noise characteristic (typical SNR ˜50dB) means that the current link is particularly suited to a bandwidth efficient, multi-level digital modulation scheme. Moreover, the short transmission lengths (˜65m) suggest immunity to attenuation, phase noise and dispersion which are typical performance-limiting factors in optical transmission systems. It is the bandwidths of the laser driver chip and receiver amplifier (˜100MHz) that ultimately restrict the achievable data rate.

ADSL is an example of how digital communication theory can be used to fully exploit a system's available bandwidth. Copper telephone lines, typically having a 3-dB bandwidth of ˜20kHz, attenuate a signal by as much as 90dB at 1MHz, which is the outer edge of the frequency band used by ADSL. Using advanced techniques which are variations of Orthogonal Frequency Division Multiplexing (OFDM) and Quadrature Amplitude Modulation (QAM), data rates between 2 and 6MBps are accomplished.

Measurements on the Tracker analog links show an attenuation of around 50-60dB at a frequency of ˜700MHz. If similar digital modulation schemes can be employed over this vastly increased bandwidth and superior Signal to Noise Ratio (SNR), data rates in the Gbps range could be envisaged.
A simulation using MATLAB Simulink has been developed in order to evaluate the benefits and drawbacks of various well-documented digital modulation techniques. The simulation can be used to produce eye diagrams as well as compute BER. The problem is treated as that of the design of a digital communication system, with the analog channel (or medium) over which signals are transmitted being the current Tracker readout link. Extensive testing on the Tracker links allows accurate modeling of the channel as a frequency-selective filter which adds Additive White Gaussian Noise (AWGN). Hence the effects of amplitude and phase distortion that cause Inter Symbol Interference (ISI) are included. In addition to performance assessment of modulation schemes, the simulation model can be used to identify the methods of Forward Error Correction (FEC) that are appropriate for this particular system. Moreover, source encoding (i.e. at the front end) in the form of data compression or optimal digitization of the analog detector signals can be easily explored.
The results of the study will demonstrate the feasibility of maximizing the bandwidth utilization of the current CMS Tracker optical links to achieve a Gbps link, and guide in the choice of method required. The application of advanced communication theory in the context of a HEP experiment is novel and would, in practice, present serious technological challenges. Nevertheless, the knowledge gained in this project could benefit future experiments by providing insight into fundamental engineering concepts never implemented before in HEP instrumentation.

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Contribution ID: **32** Type: **Oral**

A current-based readout ASIC with on chip pedestal subtraction and zero suppression for a fast readout at a future collider

Tuesday 13 September 2005 12:15 (25 minutes)

For a very fast readout of a DEPFET pixel matrix at the ILC (International Linear Collider) the 128 channel CURO II ASIC has been designed and fabricated in a 0.25 µm process.
Due to the signal of the sensor being a current, the architecture of the chip is completely based on current mode (SI) techniques.
This comprises double-correlated-sampling in the analog front end with current-memory-cells and a simultaneous current compare.
Zero suppression of the data is done also on chip by a hit finder arranged in parallel.
Measurements on the readout chip show a performance close to the ILC-requirements.
A complete DEPFET pixel system has been operated using the CURO chip in detecting 6keV photons achieving a total system noise level of ENC < 250 e-.

Summary

The future TeV-scale linear collider ILC (International Linear Collider) offers a large variety of precision measurements complementary to the discovery potential of the LHC (Large Hadron Collider). To fully exploit this physics potential, a vertex detector of unprecedented performance is needed. By moving the innermost layer very close to the interaction point (r=15mm), the occuring background by beamstrahlung becomes unusually high for an e+/e- collider (80 hits/mm²/bunch train). To keep the occupancy of the detector at a reasonable level line rates of up to 40MHz are needed.
Offering an excellent signal to noise ratio, DEPFET pixels are one promising approach for the ILC vertex detector. The DEPFET concept integrates a FET into the high resistivity detector substrate. After the amplification, the signal of the device is the transistor current proportional to the initially generated charge in the detector. With the DEPFET concept noise figures of a few 100e- ENC are possible at the required readout rates.
For the readout of such a DEPFET pixel system, the ASIC CURO II (Current ReadOut) has been designed. The full blown, 128 channel chip is 4.5 x 4.5 mm² large and has been fabricated in a 0.25 µm process.
The readout concept of the CURO chip is completely current based perfectly adapted to the signal mode of the sensor. Designing the chip, the properties of a current memory cell have been studied in detail in order to optimize the speed and noise performance. Several of these current memory cells are used in the analog front end to perform a fast Correlated-Double-Sampling. This achieves a pedestal subtraction as well as a suppression of the 1/f components of the sensor noise. After a current compare, zero suppression is done by a hit finding logic arranged in parallel which identifies up to 2 hits within less than 10ns, more than a factor of two faster

than needed for the expected occupancy at the ILC. Stand alone measurements at ˜25MHz line rate of the analog part of the chip show an INL (Integral Non-Linearity) of about 2% for a dynamic range of several mips and a capacitive load of 10pF.
The noise contribution has been measured to ENC = 45e- (considering an internal amplification of 1nA/e- of the DEPFET sensor).
A complete ILC DEPFET-system equipped with a 64x128 pixel DEPFET matrix (with ˜30x30 µm² pixel size) has been operated successfully using the CURO II chip. The system has been operated in the lab for the spatial detection of 6keV photons achieving a noise level of ENC < 250 e-. Furthermore, the system was used in a 4GeV electron test beam at DESY to study the spatial resolution and tracking efficiency of the sensor.

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Session Classification: Parallel session A1

Contribution ID: **33** Type: **Oral**

First High Fluence Irradiation Tests of Optical Link Components for Upgraded CMS at SLHC

Tuesday 13 September 2005 16:50 (25 minutes)

Lasers and photodiodes used currently in CMS, alongside new, faster components, were irradiated for the first time to very high neutron fluences, up to 2x10ˆ16n/cm2. The usual radiation effects in lasers and photodiodes were observed, with the ultimate failure point of the device being observed for the first time. As this was a particularly aggressive test these types of components are probably still suitable for optical link applications in an upgraded experiment. Equally interesting was that the laser lifetime was limited by thermal performance as much as radiation damage. As such, both a streamlined test procedure could be envisaged in future, as well as ways to improve the device radiation resistance by better cooling.

Summary

In view of proposed upgrades to CMS, work has started at CERN to investigate optical link components for new high speed links, expected to be up to 10Gbit/s capacity. The radiation environment in the upgraded experiment is expected to be ˜10 times more intense than that we have considered in the current generation of the optical links.
Testing is therefore expected to be required at dose levels of 1MGy and fluences of

10ˆ15particles/cmˆ2, where the dominant, most damaging particle species is expected to remain charged pions with energies around 200MeV as in the current generation Tracker.
A first test has been made with neutrons to very high fluences, in order to try to measure the ultimate lifetime of some laser and photodiode samples, as well as to gain some experience of high-fluence testing with a view to propose an appropriate test procedure for the future. Two types of laser and photodiode were irradiated with up to 10ˆ16n/cmˆ2, using ˜20MeV neutrons at the CRC facility in Louvain-la-Neuve. The first type of laser was that used in the current generation of CMS optical links and the second type was a similar device, but with larger bandwidth. Likewise, the first type of photodiode tested was that used in the CMS Tracker control links. The second type was very similar, from the same supplier, with this time a smaller active diameter, which meant also a higher bandwidth.
Both types of laser exhibited similar effects. There was the usual close-to-linear increase in threshold current and decrease in efficiency, which was ultimately stopped when the efficiency reached zero. There was significant annealing of the damage. The photodiodes also exhibited the expected increase in leakage current and loss of response (which decreased eventually to zero), but with more limited annealing. Both sets of devices were therefore killed by the test and, as such, their ultimate lifetime was observed for the first time.
Interestingly, the point at which this the lasers stopped working appeared to be as much affected by the internal (junction) temperature of the laser, as by the radiation induced change in threshold current or efficiency. The effects are synergistic; after being damaged, more current is required to drive the laser and this, in turn, heats the device. For these InGaAsP/InP lasers it is well known that

the performance is strongly temperature dependent and under these test conditions this sensitivity ultimately determined the lifetime of the lasers. Thorough tests of the thermal behaviour of the current generation of lasers have since been made, with measurements of thermal resistance and junction temperature. The combined results from the radiation damage and thermal tests suggest that a streamlined method could be used for future radiation hardness validation tests such that the radiation damage would be measured at lower fluences (an easier, cheaper test) in parallel with full thermal characterization of the device. These two measurements combined could predict the effects of a high fluence test, with the result being that fewer higher fluence tests would be necessary. In addition, these results also suggest that R&D into improved sub-mounts for the lasers, to maximize heat transfer away from the laser, would also be very worthwhile.

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Session Classification: Parallel session B3

Contribution ID: **34** Type: **Poster**

Fast tracking for the CBM experiment

Typical central Au-Au collision in the CBM experiment (GSI, Germany) will produce up to 700 tracks in the inner tracker. Large track multiplicity together with presence of non-homogeneous magnetic field make reconstruction of events complicated.

A cellular automaton method is used to reconstruct tracks in the inner tracker. The cellular automaton algorithm creates short tracklets in neighboured detector planes and links them into tracks. Being essentially local and parallel the cellular automaton avoids exhaustive combinatorial search, even when implemented on conventional computers. Since the cellular automaton operates with highly structured information, the amount of data to be processed in the course of the track search is significantly reduced. The method employs a very simple track model which leads to utmost computational simplicity and fast algorithm.

Track and vertex fitting is done using the Kalman filter technique.
A special analytic formula has been derived for fast track extrapolation in an inhomogeneous magnetic field.

Results of tests of the reconstruction procedure are presented.

Summary

In order to test the quality of the reconstruction procedure we used 1000 events of central Au+Au collisions at 25 AGeV in the asymmetric inhomogeneous magnetic field of the CBM magnet. The Monte Carlo simulated tracks were transported trough the inner tracker and their positions were smeared with sigma of 10 μm in order to emulate detector measurements.

Total track finding efficiency is about 97%, providing very clean reconstructed tracks with practically no ghost tracks (0.6%).

Three procedures for the propagation of track parameters have been implemented in the Kalman filter track fitting routine: a linear extrapolator for fast propagation in field free regions, a fourth order Runge-Kutta extrapolator and an extrapolator based on the analytic formula for propagation in the inhomogeneous magnetic field.

A measure of the reliability of the fit is the pull distributions of the fitted track parameters. The reconstructed track parameters and covariance matrix at the vertex where the track originates are obtained by propagating the track parameters at the measurement position closest to the vertex, taking into account the remaining material traversed.

All pulls are centred at zero indicating that there is no systematic shift in the reconstructed track parameter values. The distributions are well fitted using Gaussian functions with small tails caused by the various non-Gaussian contributions to the fit. The average relative momentum resolution is 0.73%.

The primary vertex fitting algorithm provides a very high accuracy: the residuals of the xv and yv positions of the primary vertex are about 1 μm and the zv position is reconstructed with an accuracy of 5 μm. The normalized residuals (pulls) are close to unity. The average relative momentum resolution of primary tracks is 0.63%.

The fit of secondary vertices is implemented with three options:
geometrical without constraints and with mass and topological constraints. The pull of the secondary vertex position shows that the vertex parameters are well estimated. The longitudinal resolution of the vertex of D0 decay is 61 μm. The relative momentum resolution of pi+ and K- secondary tracks are 0.43% and 0.54% respectively.

A possible hardware (FPGA) implementation of the reconstruction algorithms for the Level-1 trigger is discussed.

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Track Classification: Triggering

Contribution ID: **35** Type: **Oral**

Progress with the CMS Tracker control system

Thursday 15 September 2005 14:00 (25 minutes)

The recent progress on the CMS Tracker control system is reviewed in depth, with a report of activities and results related to ongoing parts production, acceptance testing, integration and system testing, as well as controls software development. The integration of final parts into Tracker systems and the subsequent testing is described taking the Tracker Outer Barrel as an example application.

Summary

The CMS Tracker control system is used to configure and then operate the CMS Tracker front-end electronics and readout system. The different component parts, firmware and software are in various states of production and integration, and QA/QC tests are taking place at all levels from that of the full control system down to component level. This paper will review the ongoing activities on the key parts and on the control system as a whole.
The off-detector front-end controller cards (optical mFEC) have been developed and tested at CERN. 900 optical mFECs (plus spares) are foreseen for the whole of CMS, since the same, or very similar, control system will also be used in the Pixel, ECAL, Preshower and RPC detector systems. The mFEC can be used either on the 9U FEC/CCS card or on a PCI carrier. A purely electrical version (i.e. without optical transceiver, TRX) of the mFEC has also been designed for test-system applications as well as a portable USB-interfaced FEC for rapid system debugging.
The FEC/CCS which hosts up to 8mFECs on a 9U board is approaching final production with version 3. The Tracker requires 44 FEC/CCS out of a total 130 for all of CMS. The card has been tested successfully in a VME 64x crate utilizing a bridge with a LINUX PC running the XDAQ software. It has been fully populated with 8 mFECs, and tests were carried out on the VME-local bus interface, fast timing path, as well as monitoring of the temperature of the TRXs. The power consumption is 30W. 10 earlier prototype FEC/CCS boards were made for use in system/beam tests and currently a pre-production of 10 boards is ongoing.
The production of optical control links components is almost complete. The yield is very high indeed. All parts have been tested either at the manufacturer or by CERN to ensure the reliability of the front-end digital optohybrid (DOH) and off-detector TRX parts, as well as the fibres and connectors. Only known-good parts are being used for assembly and integration into the final system. Component obsolescence in the very dynamic telecom/datacoms industries is also a serious concern and a suitably conservative approach to spares has been adopted. The DOHs are now being integrated into the Tracker sub-systems, where the different sub-systems have developed their own DOH modules (DOHM), that also include solutions for fibre-management.
The communication and control unit ASICs (CCUs), have been available in a final form for some time already, along with modules (CCUMs) to house them. A test-system was built at CERN, allowing for a full control ring with redundancy, to be tested

exhaustively with up to 16 CCUMs in the ring. The test system is fully configurable such that the number of CCUMs can be adjusted, as well as the associated cable lengths, and the eventual failure of any given CCUM, or associated element can be simulated and studied.
On the software front, the controls software consists of several dedicated layers of code. The first layer is able to access the VME through the PCI to VME interface. The original software in this layer was intended as a Linux device driver able to drive either an electrical and optical PCI FEC. The second layer manages the control ring and the way in which the the front-end ASICs are accessed and configured through the I2C bus. A third layer manages the eight rings on a single FEC/CCS board and the fourth layer is the high level software that will be integrated in the complete framework of the data acquisition system in the CMS experiment using XDAQ. The high level software is able to retrieve information from a database management system to configure the front-end ASICs with the appropriate settings. It also manages the handling of possible errors in the ring, switching between the primary and backup control path in the redundancy scheme. The speed at which the system commands are transmitted has been measured in detail and this will be reported.
The control system for the Tracker Outer Barrel (TOB) will be considered in more detail as an example application. The integration and assembly and testing of the various parts onto 'rods'(the basic detector unit of the TOB) has been defined and the activity is currently well under way. No rods have been rejected due to failures in the control elements so far. A thorough test of the TOB control system using final CCU and DOH carrier boards is also under way, employing the latest versions of the controls software. The performance of the control system with up to 10 TOB-variant CCUMs in the ring has been studied, with the front-end parts exposed to temperatures between ambient room temperature and -30C, which is below the intended operating temperature of the Tracker. The control system works well, with a low rate of transaction errors (at room temperature and at low temperature), in tests conducted continuously over several days with I2C commands sent to the various front-end components in a continuous stream. More tests at different temperatures are foreseen and these will be reported.

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Presenter: Mr GILL, Karl Aaron (CERN)

Session Classification: Parallel session B5

Contribution ID: **36** Type: **Oral**

Tilecal ROD final system. Design, performance, production and tests

The Tilecal Read Out System (ROD) must be able to receive the calorimeter data filtered by the first level trigger, process them, and send them to the ATLAS generaldata acquisition system (TDAQ), where the level 2 trigger decision will be taken.Therefore the ROD is placed between level 1 and 2 trigger levels.

The ROD will process in real time the discrete samples of each calorimeter channel (˜10000 total channels) in order to reconstruct from such digital information the following physics parameters:
1)The total Energy of a Calorimeter cell (scintillators + photomultipliers channel),
2)The phase shift (time of signal arrival)
3)Fit quality factor (chi2)
4)Send raw sampled data for later deep analysis in case of pile-up, etc ⋯

Summary

All these processed data will help to understand physics in ATLAS Hadronic calorimeter and to take the level 2 trigger decision where information from all ATLAS Sub-detectors will be correlated. Besides, there is a level 3 trigger of bigger granularity that helps to filter the huge amount of event data generated in ATLAS with a p-p bunch crossing of 25ns in LHC.

The TileCal data acquisition system is divided in 4 readout partitions. A partition is built around a ROD crate with at least 10 modules mounted in it: 1 ROD controller, 1 Trigger and Busy Module and 8 ROD modules (1 ROD Motherboard + 2 DSP Processing Units + 2 S-link HOLA LSC). With this architecture there will be 32 RODs to feed 64 ROBs. With this 1:2 mapping, two optical links (S-Link HOLA LSC) are mounted per ROD to compensate the number of ROBin´s and to fulfill the TileCal dataflow needs.

ROD motherboard based on the ROD final production board from the LiArg sub-detector is the final hardware solution to work at a 100 KHz Level 1 trigger rate with digital signal processing capabilities and input/output optical links. The differences between both RODs are mainly at the input stage of the board and related to the data clock frequency and transmission protocol. There is minor hardware design modifications proposed to keep the same PCB layout and to do a common production, but large modifications related with the input stage and PU firmware. These modifications were proposed to be implemented in the second batch of final ROD prototypes and validated in the two units received for TileCal from the prototype series production.
The design of the Firmware for FPGAs (VHDL) and DSPs (C, ASM), and the Software for ROD library, XTestROD (GUI Interface for debugging) and Online Software for production tests (C++, java) was developed by the Valencia-Tilecal Group. Therefore, all the firmware, online/offline software, and the Hardware is ready to test the full production boards from May to September 2005 in the laboratory and later to install the system in the pit (USA15) during the Tilecal –ATLAS commissioning

phase. The Hardware and Software system was also validated in past ATLAS Combined Testbeam 2004 with successful results in terms of management, stability and performance.

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Contribution ID: **37** Type: **Poster**

The Macro Assembly of The ATLAS Semi-Conductor Tracker

With the completion of the assembly of silicon detector modules and their supporting structures, the focus of activity has moved to the production and operation of large assemblies of multiple modules. This involves the physical mounting of modules onto their supports, the connection of their services and the subsequent testing. This paper describes the assembly and test procedures for these complex arrays and draws conclusions on the transition from the operation of single modules to large scale structures with in excess of 100 individual modules each. The current status of the final testing of the barrel and endcap sections of the detector at CERN, comprising a total of 4000 modules, is described.

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Contribution ID: **38** Type: **Oral**

ALICE SILICON STRIP DETECTOR MODULE ASSEMBLY WITH SINGLE-POINT TAB INTERCONNECTIONS

Wednesday 14 September 2005 14:40 (25 minutes)

The silicon strip detector (SSD) modules cover the two outermost layers of the Inner Tracking System of ALICE. The SSD module assembly will be performed at three locations in Europe: Helsinki, Strasbourg and Trieste. After a tedious preparation period within the whole ALICE SSD collaboration, mass production of the SSD modules was launched during autumn 2004 in Helsinki. Presently all the sites are producing the SSD modules successfully.

Due to tight requirements of light structure and flexible geometry the so-called single-point tape-automated bonding (spTAB) with thin polyimide-Al cables has been chosen as interconnection technique. The technique is based on Ukrainian industrial technology. In an spTAB interconnection very reliable Al-Al bonds connect the front-end chips, hybrids and sensors together. The use of Al as conductor allows for low-force ultrasonic bonds to be performed gently at room temperature.

Presently, the spTAB interconnections are performed successfully at all three sites with bonding yield approaching close to 100%. This paper describes the phases in bond process tuning before achieving this result, including discussion on the most probable root-causes of failures and the long-term reliability of the interconnections. The interconnection reliability defines the lifetime of an SSD module as a significant part of the assembly.

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Session Classification: Plenary session P5

Contribution ID: **40** Type: **Oral**

TTC challenges and upgrade for the LHC

Friday 16 September 2005 11:05 (25 minutes)

The TTC (Timing, Trigger and Control) system broadcasts the timing signals from the LHC machine to the experiments. At the detector level, it integrates the trigger information and local synchronous commands with these signals, for transmission to several thousands of destinations. If the support of the TTC system at the level of the detectors is well in hand, the main network between the machine and the experiments will require re-development to ensure its easy maintenance. A status of this system will be presented, as well as the challenges it has to cope with and the necessary upgrade which will be needed in the near future to make it operational for LHC start in 2007.

Summary

The TTC (Timing, Trigger and Control) system broadcasts the timing signals from the LHC machine to the experiments. At the detector level, it integrates the trigger information and local synchronous commands with these signals, for transmission via optical fibres to several thousands of destinations. If the support of the TTC system at the level of the detectors is well in hand, the main network between the machine and the experiments will require re-development to ensure its easy maintenance.

The functional specification of the TTC has changed during the last 5 years: three different types of 40.079 MHz clocks, as well as their respective orbits have been now defined to be transmitted by the TTC from the machine up to the experiments. Their availability during the various machine modes is not guaranteed by the machine outside the flat tops of LHC runs. The TTC has then to be able to supply these signals if they are not transmitted by the LHC. Moreover, the channel B, defined for control and command transmission, is not used at the LHC level, but only at the level of the detectors. A simplification of the TTC at the CERN Control Centre could then be made.

The need to simplify the first level of the system is also made necessary by the fact that the electronics at the CERN Control Centre is now becoming obsolescent as well as at the reception level in the detectors. As the number of timing signals to be transmitted has now increased, the need in term of infrastructure also augmented. The number of available receiver crates is not sufficient to receive the 3 various Bunch Clocks and Orbits. Spares are also missing, and there is no way to replace faulty modules.

Finally, at present, the system can neither be remotely controlled, nor monitored, which makes the on-call support and the maintainability difficult.

A status of the present TTC system will be presented (available infrastructure, production status, comparison with the BST system), as well as the challenges it has to cope with (latest problems solved, new test benches) and the necessary upgrade which will be needed in the near future to make it operational for LHC start in 2007:
• New solutions for the timing signal transmission, from the machine to the

experiments
• New hardware proposal to replace the TTCmi crates
o Clock and orbit reception
o Missing Clock compensation
o Phase adjustment control
o Remote monitoring module and solutions for the support
o Signals distribution

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Session Classification: Plenary session P9

Contribution ID: **41** Type: **Poster**

PIConNET Based Distributed System Dedicated to Magnetic Test of the CMS Muon Barrel Alignment

For the precise measurement of the positions of the barrel muon chambers in the CMS detector, a Position Monitoring System (PMS) has been developed at our institutes. The magnetic field, which has to be tolerated by the system, is 2 Tesla. The aim of this paper is to present and discuss the logical organisation, applied tools and methods of a subsystem of the PMS, which is dedicated to the forthcoming magnetic test.

Summary

Performance of the CMS detector of the Large Hadron Collider (LHC) is affected by the position and orientation of the individual detectors. Therefore, the CMS detector has an alignment system that consists of several subsystems. One of them is the barrel and end-cap internal alignment, which measures the positions of the muon detectors with respect to the linking points. This system will consist of LED light-sources with related electronics, video cameras equipped with video-sensors, temperature and tilt meters and a local network of 36 pcs PC-104 based computer for data acquisition and system control.
The optical, opto-electronic components and the computers have to work in a 2 Tesla strong magnetic environment. The possible damages induced by the strong magnetic field can alter electrical and optical characteristics of the components and thus the accuracy of the whole alignment system. In late 2004 the CMS Collaboration decided to put up a special experiment for the CMS Muon System with the Alignment components mounted, in order to enable the characterisation of the whole system under real conditions. For the experiment only the most crucial parts of the detector system (Sector 10/11 from each Wheel) will be installed, equipped and tested.
As it was reported in our earlier papers a computer network - based on dedicated so called mini-Crates - will be used for controlling of the opto-electronic components of the Alignment System. The delayed delivery of the mini-Crates prevents them to be used in the scheduled magnetic run. Their functionality can be replaced by the PIConNET micro-controller board, which is a versatile board equipped with an Ethernet communication interface.
For communication media we have chosen twisted pair Ethernet and for communication protocol we use a User Datagram Protocol (UDP) based proprietary protocol. The advantages of Ethernet and UDP/IP technologies are clear: they are mature and well tested, many applications are available for development and debugging, they are scalable and cost efficient.
The dynamic discovery of components (clients, masters and servers) is a key function of the design. For this purpose we designed and implemented a custom protocol, which is similar to the Dynamic Host Configuration Protocol (DHCP).
Our contribution will show the design of the dedicated PIConNET based distributed system for magnetic test of the CMS Muon Barrel Alignment. The investigation is focused on the components that are very sensitive for the magnetic field and on

those methods that preferably have to be applied in case of trouble.

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Contribution ID: **42** Type: **Oral**

The VMEbus processor hardware and software infrastructure in ATLAS

Thursday 15 September 2005 11:25 (25 minutes)

Most of the off-detector custom electronics of the ATLAS data acquisition system such as the Read-Out Drivers or the Trigger and Timing Control system has been implemented in VMEbus. The paper describes the process of selecting a common VMEbus processor module for all VMEbus systems in ATLAS and the problems encountered during the evaluation of different candidate cards. Some performance figures for VMEbus transfers are presented.
The paper also discusses why ATLAS has decided to develop its own Linux based VMEbus driver and presents the features and performance of that driver and its user level library as well as some related software packages.

Summary

The data acquisition system of the ATLAS experiment contains several large, VMEbus based sub-systems. There will be about 120 9U VMEbus crates to house the Read-Out Drivers. In addition there will be of the order of 30 6U crates to house the modules of the Trigger and Timing Control system. Finally there is a large number of VMEbus based test benches both at CERN and in the collaborating institutes.
It was felt necessary to prevent the groups responsible for the individual sub-systems from selecting their favorite VMEbus Single Board Computer (SBC) by standardizing on a single type of SBC for all installations.
In 2001 a small group of experts was formed to specify the requirements of a common SBC both in terms of its technical features as well as the support which had to be guaranteed by the manufacturer for at least nine years. At the same time a number of VMEbus SBCs from different vendors was evaluated to identify potential problems and to better understand the advantages and disadvantages of the different SBC architectures. To avoid limiting the competition too much the final specification did allow for a wide range of architectures (i.e. PowerPC and Pentium, all types of VMEbus master interfaces). The SBC that was finally selected is based on a Pentium CPU and the Tundra Universe PCI to VMEbus interface.

The evaluation of this and similar SBCs has identified a number of potential problems with the Tundra Universe chip:
- It has no built in endian conversion. In case of a little endian CPU (e.g. Pentium) this feature has to be provided by some vendor specific auxiliary logic.
- Moderate performance
  - o D32 R/W = 4 MB/s
  - o D32 posted W = 13 MB/s
  - o D32 BLT = 20 MB/s
  - o D64 MBLT = 40 MB/s
- Difficult bus error handling
- No true constant address DMA for reading out FIFOs
- Problems with BERR terminated BLTs

Depending on the PCI host bridge used on the SBC problems in the form of VMEbus error can arise if the SBC has to deal with master and slave accesses at the same time.

In parallel with the H/W the options for the VMEbus access S/W were analyzed. Despite the effort made by the VISION standard a few years ago there is no widely accepted standard API for access to the VMEbus. A number of free and commercial drivers exist for the Tundra Universe chip but they are not compatible. Finally the decision was made to program a dedicated Linux VMEbus driver and library for ATLAS. This gives full control over the code and the API and allows optimizing the S/W for the particular needs of ATLAS. The driver and library provide two ways of doing single cycles, extensive support for chained block transfers, bus error handling and the possibility to handle interrupts both synchronously and asynchronously. Less frequently used features such a support for SYSFAIL interrupts or special AM codes for geographical addressing (VME64x) have been added as well.

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Session Classification: Parallel session B4

Contribution ID: **44** Type: **Oral**

The Detector Control System for the ALICE Time Projection Chamber Front-end electronics

Thursday 15 September 2005 14:25 (25 minutes)

The ALICE Time Projection Chamber (TPC) is read out by 4356 Front-End Cards serving roughly 560000 channels. Each channel has to be configured and monitored individually. As one part of the overall controlling of the detector this task is covered by the Detector Control System (DCS).

Since fault tolerance, error correction and system stability in general are major concerns, a system consisting of independently running layers has been designed. The functionality layers are running on a large number of nodes and sub-nodes.

This talk will focus on the concept and architecture of the DCS for the Front-end electronics of the Time-Projection Chamber (TPC) and present results and experiences from system integration tests.

Summary

The Detector Control System in general is divided into three layers, Supervisory Layer, Control Layer and Field Layer. The Supervisory Layer is the top-level with the operator's user-interface. The Control Layer is a communication layer, and the Field Layer is where the different hardware devices are found. All the components in the system work in parallel, feeding the operator with useful information concerning the status of the system, or responding to commands given at the top-level. The DCS for the TPC Front-end electronics is designed to act upon errors as close as possible to the source. Functional blocks are distributed over a larger number of computing nodes and sub-nodes.

The system described is based on so called Front-End-Electronics-Servers (FeeServers). A FeeServer abstracts the underlying Front-end electronics to a certain degree and covers the following tasks:
- Interfacing hardware data sources and publishing data
- Receiving of commands for configuration and controlling the Front-end electronics
- Self-test and Watchdogs (consistency check and setting of parameters)

A dedicated communication software, the InterComLayer, handles the connection between the lower Field Layer and the upper Supervisory Layer. The main tasks are controlling the FeeServers in the Field Layer, sending configuration data to the Front-end electronics and transporting monitoring data to the Supervisory Layer. The InterComLayer implements three interfaces, a Front-End-Electronics client, a Front-End-Device server and a client to the Configuration Database. These interfaces are common abstraction layers within the ALICE experiment.

The FeeServer and other controlling software in the Field Layer runs on the DCS board, an autonomous single-board computer which allows running complex controlling software under the operating system Linux. Further custom hardware devices have been developed covering specific tasks and serving as sub-nodes. The Readout Control Unit (RCU) hosts basic controlling functionality for a set of FECs. Some tasks of the DCS like the Monitoring and Safety Module are carried out by firmware modules of the RCU.
In total the system consits of 216 embedded Linux nodes. Together with standard

computers in higher control layers the DCS board and the RCU board form a distributed control system.

The architecture has several advantages:
- Distributed and module-based design with well-defined interfaces increases structure and testability.
- Parallel systems increase bandwidth and reduce workload on each node.
- The system is independent of physical intervention. This is of high importance as the system is unaccessible when it is in operative mode.
- Linux operating systems on the embedded computers provides flexibility and standard tools.
- Software and Firmware that is easily reconfigurable.
- Low-level devices with intelligent error-handling decrease the possibility for permanent failures.

The system is still under development. Several small scale control systems consisting of the DCS board and applicable sub-nodes has already been used as stand alone systems in major tests. The modularity makes it possible to test and review each sub-system on it's own independently of the complete setup. Several integration and beam-tests have been performed with satisfying results. The talk will focus on experiences and results from the major integration test in May 2005.

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Session Classification: Parallel session B5

Contribution ID: **45** Type: **Oral**

Production of the LHCb Silicon Tracker Readout Electronics

Tuesday 13 September 2005 17:15 (25 minutes)

We give an overview on the status of production of the LHCb Silicon Tracker Electronics. Lessons learned together with the industry in the preseries production of the Silicon Tracker Digitizer Boards were integrated into the design to optimize the production and assembly yield of the main batch of 700 Digitizer Boards. A report on the preseries readout module performance and on the testing procedures for the full production lot is given. In addition, a final proton irradiation test of a complete readout system has been performed, of which results will be presented.

Summary

The LHCb Silicon Tracker is part of the LHCb main tracking system and provides data for region of high track densities. For the tracking station TT in front of the main dipole magnet, the Silicon Tracker covers the full acceptance angle of the experiment, while for the stations T1-T3 after the magnet, the Silicon Tracker only covers the region directly around the beam pipe. The analogue hit information of the silicon strip detectors, which is amplified by the Beetle readout chip, is transmitted via copper cables to the Services Boxes, which are located outside the acceptance area. This does not only reduce the amount of material inside the detector but in addition relaxes the requirements to the Service Box electronics concerning radiation tolerance. The Service Boxes hold the Digitizer Boards, on which the analogue signals from the Beetle frontend chips is digitized and encoded into a Gigabit data stream for transmission via VCSEL diodes and 120 m of multi-ribbon optical fibre to the counting house. In the counting house, the optical ribbons can be directly connected to TELL1 preprocessor boards equipped with two multi-channel optical receiver cards.
This talk briefly describes the general design of the Silicon Tracker readout system and its common elements with other LHCb subdetectors. We present results on performance and lessons learned from the production of preseries modules, which have been included in the final design. The full production of 700 units will be done this summer and details about production lot testing and burn-in are given. The final design was also tested again for radiation tolerance by a proton irradiation, of which results will be shown. Preseries modules have been connected to a full length setup of the readout link with optical ribbon cable. On the receiving side, a first preseries unit of the common LHCb Level-1 preprocessor board (TELL1) was used to record the data coming from a beetle readout hybrid. For trigger control, a LHCb TFC readout supervisor was used together with the optical TTC trigger distribution network, therefore representing the first global setup using LHCb DAQ components.

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Session Classification: Parallel session A3

Contribution ID: **46** Type: **Oral**

Delay25, an ASIC for timing adjustment in LHC

Tuesday 13 September 2005 11:25 (25 minutes)

A five channel programmable delay line ASIC was designed, fabricated and tested. The IC features 4 channels that allow to phase delay periodic or non-periodic digital signals and a master channel that can be used to phase delay a clock signal. The master channel serves as a calibration reference guaranteeing independence from process, supply voltage and temperature variations. The phase of each channel can be independently programmed with a resolution of 0.5 ns through an I2C interface. The reference clock frequency can be 32, 40, 64 or 80 MHz. The ASIC is manufactured in a 0.25 m CMOS standard technology using radiation tolerant layout practices. The measured output jitter for the master channel is below 10 ps (rms) and below 20 ps (rms) for the replica channels.

Summary

The Delay25 is a 5 channel programmable delay line ASIC intended to be used in timing distribution systems and for phase adjustment of signals in HEP experiments. The ASIC consists of a master channel controlled by a Delay-Locked Loop (DLL) and 4 replica channels. It is able to delay asynchronous and uncorrelated digital signals with a resolution of 0.5 ns. A signal can be delayed up to 32ns.
The master channel consists of a delay-locked loop that receives an external clock reference. It locks to this signal guaranteeing a delay of 0.5 ns in each Delay Element (DE) along the master delay line. This means that the delay on each DE of the master delay line is independent of the process, temperature and supply voltage being self calibrating.
Each delay line consists of 64 delay elements. The ASIC can operate with four different reference frequencies: 32, 40, 64 and 80MHz. The control is made such that along the line the total delay is exactly one clock period. Since each DE should have 0.5 ns delay, the total number of delay elements used in the control loop depends on the input signal frequency: 64 for 32 MHZ, 50 for 40 MHz, 32 for 64 MHz and 25 for 80 MHz.
The layout of the replica channels is made exactly the same as that of the DLL delay line for good matching among the five delay lines. The replica delay lines operate in open loop so the control voltage for each delay element on these lines is the voltage that is generated by the DLL to control loop.
The ASIC has 6 internal registers that can be accessed by an I2C interface. Five of these registers are used to program the delay of each channel. The other register is used to program the operation mode and can also be used to initialise the DLL or perform an ASIC reset through software.
The ASIC has five independent inputs and five independent outputs, one per channel. The I/O levels can be configured through a dedicated pin to be either CMOS or LVDS compatible.
The measured output jitter is below 10 ps (rms) for the master channel and below 20 ps (rms) for the replica channels. The integral non-linearity (difference between

the programmed delay and the measured delay) and the differential non-linearity (difference from the expected delay in a certain tap and the measured delay for that tap) are both below 50 ps (rms) for both the master and the replica channels.
The ASIC is manufactured in a 0.25 ☒m CMOS standard technology using radiation tolerant layout practices.
Measurement results will be presented focusing on the comparison of the performance of the two I/O modes regarding output jitter, Integral and Differential non-linearity, pulse distortion and crosstalk between channels.

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Session Classification: Parallel session A1

Contribution ID: **47** Type: **Oral**

FPGA Dynamic Reconfiguration in ALICE and beyond

Friday 16 September 2005 10:10 (25 minutes)

Using the FPGA Virtual File System for Dynamic Reconfiguration of FPGAs, we have been investigating improvements to various aspects and components of the ALICE electronics. In this paper, we will briefly summarize the results from our work on improving the radiation tolerance of FPGA-based experiment electronics, followed by a deeper coverage of our more recent work on using the File System for reconfiguration of functional modules and for FPGA debugging, including the underlying concepts as well as the practical applications for ALICE and LHC in general.

Summary

The FPGA Virtual File System (FPGA VFS) is a technology based around the idea of FPGA Dynamic Reconfiguration. It provides accessibility of the FPGA configuration data of Xilinx Virtex devices on different levels of abstraction. We are using the FPGA VFS to improve various aspects of ALICE electronics, in particular for the TPC, RCU, TRD and GTU.

As reported previously, we have performed radiation tolerance experiments with Xilinx Virtex-II Pro FPGAs, using the FPGA VFS to identify and repair single-event upsets in the configuration memory. The results of this initial work formed the basis for the redesign of the RCU, leading to a system with a higher radiation tolerance and significantly improved system availability. We will give a brief summary of the key technologies and system requirements to built such a system.

More recently, we have been investigating other applications of the FPGA VFS for ALICE electronics. In these applications, the Virtual File System acts as the middleman between the user (or engineer) and the hardware by taking care of the details of FPGA reconfiguration and providing the necessary functionality at the required level of abstraction.

Of particular interest are the following two: in-vivo replacement (reloading) of functional modules, and in-system, non-invasive FPGA debugging.
Reloading of functional modules is one of the key ideas of FPGA Dynamic Reconfiguration. In ALICE electronics, it can improve the overall performance of the system. It does so by enabling the system to adapt to changing requirements, and it allows to fit more functionality into smaller parts, thus helping keep the system within power restrictions. To give some examples: using different algorithms when observing different trigger conditions, dynamically changing the routing or processing for faulty modules, loading I2C diagnostics modules depending on pecific error conditions etc. are all possible using this technology.

Debugging of the in-system FPGA is an idea resulting from the capability of the FPGA Virtual File System to represent all components of the FPGA in a user configurable hierarchy. In particular, it can present the states of the flip-flops and memories using the naming from the HDL source, i.e. “/module_name/component_name/register_name”. It can also be used to reconfigure the clocks to allow single-stepping of the FPGA.

Combining these features, we get two of the three basic functionalities of any software debugger –inspection of memories and single-stepping. In contrast to other approaches to FPGA debugging, the Virtual File System does not require modifications to the existing design, thus preserving the original system. The third basic functionality, the ability to set break points, is not currently part of our work, but certainly not impossible achieve.

We will report about the details of both concepts, as well as the status of their practical implementation in ALICE.

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Session Classification: Plenary session P8

Track Classification: Data Acquisition and Controls

Contribution ID: **48** Type: **Oral**

Mass production testing of front-end ASICs for ALICE SDD system

Tuesday 13 September 2005 16:25 (25 minutes)

This paper presents the wafer-level testing system developed for the front-end electronics of the Silicon Drift Detectors of ALICE. The system is based on a semiautomatic probe station and has been designed to test two different ASICs with minimal changes in the hardware. All the operations are controlled by a PC running a dedicated LabView software. The architecture of the test system is described and the results obtained in the mass production test are discussed.

Summary

The front-end electronics of the Silicon Drift Detectors (SDDs) of ALICE is based on two custom integrated circuits: PASCAL (Preamplifier Analog Storage and Conversion from Analog to digitaL) and AMBRA (A Multievent Buffer Readout Architecture). PASCAL is a mixed-mode integrated circuit that samples the signals coming from the detector and digitizes them when a trigger signal is received. AMBRA is basically a RAM that allows the derandomization of the trigger. This chip performs also some digital signal pre-processing, like baseline equalization and 10-to-8bit compression. Both ASICs have been designed and produced in 0.25 um CMOS technology. For cost reasons the two chips have been fabricated using the same set of masks. Each 8-inch wafer hosts 146 PASCAL and 146 AMBRA. This paper describes the test system developed for the on-wafer testing and discusses the results obtained.

The test system is based on a Cascade Microtech Rel-6100 probe station with a motorized chuck stage controlled via GPIB interface. It is required to use two different full custom active probe cards for the two ASICs. Each probe card contains custom to standard differential digital buffers.

To reduce as much as possible hardware dependence, the digital control signals are generated by a data pattern generator (Agilent 16702B Logic Analysis System); the outputs are read out by the logic state analyzer (on the same instrument) and then sent to a PC for data analysis. For AMBRA, which is a pure digital IC, it is possible to implement data analysis directly on the logic state analyzer. The data produced by PASCAL are digitized analog signals and a more complex statistical analysis isrequired for an adequate assessment of the performance. In this case the raw data are sent to a PC. The computer performs online a complete data analysis evaluating the critical parameters (gain, linearity, number of dead channels, ADC and DAC performance, etc.).

The whole test system is controlled by a PC running a software developed in LabView. The program allows to drive the test hardware (probe station and power supplies via GPIB, data pattern generator and logic state analyzer via TCP/IP and all support electronics), to control all test steps and to create report files for the database in a friendly windows-based user interface.

The mass production testing system is installed at the INFN in Rome. The typical testing time is 8 minutes for PASCAL and 5 minutes for AMBRA. The architecture of

the test system, the test selection criteria and the test results will be discussed in detail in the final paper.

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Session Classification: Parallel session A3

Contribution ID: **49** Type: **Poster**

The Control System for the Muon Detector of LHCb

Within the Framework of the CERN Control System Project, using PVSS as the main tool, we developed an instrument to manage of the Muon System of LHCb.
Adjustment and monitoring of High and Low Voltage power supplies,on-line diagnostics and fine tuning of the Front-End read-out devices, data acquisition from the gas system and the monitoring of pressure and temperature of the experimental hall have been implemented.
The system will also manage long term data archiving and the alert handling.
The Control System performance is now being deeply tested in a cosmic ray station.
Built as a final quality control of the LHCb Multi-Wire Proportional Chambers, allowing acquisition of data from as many as 600 Front-End readout channels, the cosmic ray station is fully managed by means of a Control System prototype.
The developed tools and the test results will be presented.

Summary

The LHCb muon system, presently under construction, will be composed of five detector stations (M1-M5) equipped with more than 1400 detectors.
High efficiency and a good space resolution are required.
The large number of the detectors and the high performance required make the Control System of the Muon System Apparatus a significant task to accomplish.
Within the Framework of the CERN Control System (CS) Project, using the PVSS program, we designed an instrument to fully manage the Muon System during the data acquisition.
Performance of the chambers in the Muon System will strongly depend on the temperature and pressure of the experimental hall.
Consequently, it will be mandatory to monitor and acquire the environmetal parameters.
An equalization and a stabilization of the gain will be achieved by tuning the high voltage supplies on a case by case basis.
The Control System will also manage the ramp-up and ramp-down phases of the entire high voltage system, monitoring of the current drawn at the same time.
The Muon System will be made up of 120,000 readout channels.
Electronic channels will need a constat monitoring in order to single out dead or noisy channels and adjust the channel settings, such as thresholds and masks.
An array of low voltage supplies will be used to provide power to the front end readout devices.
Their main paramenters such as current, voltage as well as their overall status will be will be acquired.
The data coming from the gas distribution system, regarding the supply of the gas mixtures to the detectors will be monitored and acquired.
The Control System will manage the long term archiving and alert handling for all the data concerning the status of the apparatus.
A first down scaled implementation of the Control System is now being used and

tested to fully manage a cosmic ray station built for the studies of the LHCb MultiWire Proportional Chambers.
The CS controls high and low voltage supplies as well as the front-end readout devices, stores data regarding the system status and manages the alert and the alarm situations.
The CS test is giving a unique possibility to study in details their different features and is an usefull tool to test the robustness of the Muon Detector CS.

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Contribution ID: **50** Type: **Oral**

A multiplicity trigger based on the Time of Flight detector for the ALICE experiment

Thursday 15 September 2005 16:25 (25 minutes)

The goal of the ALICE Time of Flight detector, based on MRPC technology, is to perform charged particle identification at |eta|<1. This large area (150 mˆ2), finely segmented detector (˜160,000 channels), provides fast signals which will contribute to the L0 and L1 trigger decisions.
Hits from the TOF detector are used to determine the multiplicity and topology of the events. This information is used to (a) generate a cosmic muon trigger and (b) to differentiate between central and peripheral collisions.
The system architecture foresees a first layer of 72 VME boards interfacing the detector front-end to a second layer, which receives and processes all the information and takes trigger decisions.

Summary

The design of the trigger of the ALICE experiment foresees a multilevel architecture, with three levels of hardware implemented currently. The first decision (L0) is taken 1.2 microsec, the L1 decision is taken 6.5 microsec and the L2 decision is issued 88 microsec after the collision.

Taking advantage of the MRPC (Multigap Resistive Plate Chamber) detector, the Time of Flight provides very fast signals with very low noise. The idea is to use the information from this large area (150 m2), finely segmented detector (˜160,000 channels) for a fast estimate of the event track multiplicity. Since the fast signals from the detector are available shortly after the collisions, the TOF trigger can comfortably contribute to the ALICE L0 trigger decision. The large granularity of the TOF and the low noise of the MRPC allows to trigger on various configurations:
- classification of events with very large/low track multiplicity corresponding to the central/peripheral ion-ion collisions;
- identification of events with large and localized track multiplicity as jet events in pp collisions;
- back to back patterns of cosmics events, which will be very useful during the commissioning of the detector itself.

The TOF detector is made of 18 supermodules, each covering an azimuthal angle of 20ˆo and a pseudorapidity of |eta|<1. Four Local Trigger Modules (LTMs) are needed to process the data from one supermodule. Each LTM has 48 inputs. Each input is made by the logical OR of 48 TOF pads, whose area is ˜9 cmˆ2.
The architecture of the TOF trigger uses a first layer of 72 VME (9U) boards (LTM). The LTMs provide an interface between the front end electronics and the second trigger layer, called CTTM (Cosmic and Topology Trigger Module) and made of a number of VME boards. The CTTM receives the input signals from the 72 cables coming from the LTMs and each cable transmits 24 signals. The distance between the 72 LTMs and the CTTM is about 60 m.
Extensive R&D has been performed to safely transmit LVDS signals over this distance.

A dedicated calibration is foreseen to allow the LTMs to compensate for the relative time differences among the 1728 input signals. This is achieved by using commercial delay line units, programmable through the LTM VME interface. The aligned input signals are then processed in the LTMs using an Altera Cyclone FPGAs. The clock used by the FPGA to sample the input signals is synchronized to the LHC machine clock (40 MHz) to associate correctly the input data to the corresponding bunch crossing and to provide to the CTTM the full set of information required to assert a L0 trigger decision.

The CTTM generates the L0 and the L1 trigger decisions. Since the L0 decision must reach the ALICE Central Trigger Processor (CTP) within 800 ns after the interaction, a very fast data processing will be implemented. A more detailed analysis will be possible for the L1 decision.

At present both the LTM boards and the protocol for 60 m LVDS signal transmission have been successfully prototyped and tested, while the design of CTTM boards is well advanced.

In this talk we will show the TOF trigger layout and selection capabilities, both for cosmic and beam events. The results obtained with the prototype boards are presented.

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Session Classification: Parallel session B6

Contribution ID: **51** Type: **Oral**

Installation and Test of the CMS Crystal Calorimeter Electronics

Thursday 15 September 2005 14:25 (25 minutes)

The CMS Electromagnetic Calorimeter consists of roughly 76000 lead tungstate crystals. Nearly 25000 Printed Circuit Boards of 5 different types and about 5500 Gigabit Optical Links are used to process the signals of the photo-detectors and to send the resulting data to the off- detector electronics.
The integration of this electronics together with its cooling system, mechanical supports, the low voltage distribution, various signal cables and optical fiber patch panels is described. Complexity and installation sequence require tests at each step of installation. The test strategy during the installation is described and results of the system performance achieved are presented.

Summary

The CMS Electromagnetic Calorimeter (ECAL) is divided into the Barrel (EB) and two End-Cap (EE) calorimeters
made of 61200 and 14648 crystals, respectively. The EB is made of 36 super modules with 1700 crystals each
and the EE of 4 DEE's with 3662 crystals each.
In each super module 554 printed circuit boards have to be installed:

1) 68 mother boards (MB) provide the connections between the photo-detectors (APD) and the very front
end (VFE) cards, distribute the bias voltage of the photo-detectors and part of the low voltage
2) 340 VFE cards amplify, shape and digitize the photo-detector signals of 5 crystals each
3) 68 low voltage regulator (LVR) cards provide the required low voltages
4) 68 front end boards (FE) process the digital data of 5 VFE cards each, generate trigger information and
perform control functions
5) 8 token ring link boards (TRLB) interface the control fibers to electrical token rings, providing the LHC
clock as well as fast and slow control data to the FE cards
6) 2 x 68 gigabit optical hybrids (GOH) transfer the data and trigger information to the off detector
electronics
7) Two FE cards and two GOH are used to read out the pin diodes of the light monitoring system
8) Low voltage bus bar distributions, power cables, remote sense wires and low voltage control cables are required
9) 12 distributed fiber patch panels bundle the fiber pigtails of the GOH into 12 way ribbons

The basic building block of the electronics is the readout of a trigger tower (a matrix of 5 x 5 crystals)
consisting of one mother board, five VFE cards, one LVR card and one FE card. Thus the basic test block is the test of a trigger tower. It includes verification of

the FE identifier, listing the I2C devices, initialization, parameter setting and verification of the FE, setting of the VFE parameters, computing of the pedestal DAC setting, measuring the pedestals, injecting test pulses into the VFE using the integrated test pulse generators and reading of the LVR card voltages.
The installation is performed in 5 steps:
1) Installation of the mother boards and verification the connection to the photo-detectors, followed by the
completion and test of the cooling system.
2) Mounting of the trigger tower electronics and test of each trigger tower individually.
3) Installation of token ring boards, connection and verification of the token rings, including the redundant
parts.
4) Installation of the gigabit optical hybrids and the distributed fiber patch panels, followed by a repetition
of the test of individual trigger towers
5) Installation of the low voltage distribution system.

A completed supermodule is operated for about one week. The data taken during this period are analysed to assess the system performance.

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Session Classification: Parallel session A5

Contribution ID: **52** Type: **Oral**

Electromagnetic Compatibility of a DC Power Distribution System for the ATLAS Liquid Argon Calorimeter

Thursday 15 September 2005 12:15 (25 minutes)

The front end electronics of the ATLAS Liquid Argon Calorimeter is powered by DC/DC converters nearby the front-end crates. They are fed by AC/DC converters located in a remote control room through long power cables. The stability of the power distribution scheme is compromised by the impedance of the long interconnection cable, and proper matching of the converters dynamic impedances is required. Also, the long power cable fed by a powerful AC/DC converter is a source of electromagnetic interferences in the experimental area. The optimal grounding and shielding configuration to minimize these EMI is discussed.

Summary

I. POWER DISTRIBUTION SCHEME FOR THE LIQUID ARGON DETECTOR
The amount of power required by the front end crates of the Liquid Argon Detector of the ATLAS experiment imposes the presence of a power supply in their vicinity. As the magnetic field limits the use of power transformers, a front end power supply based on modern DC/DC converters was chosen. AC/DC converters that sit in a control room located 100 meter away of the detector provide the bulk power to the front end power supplies.
The long DC power link faces several electromagnetic compatibility issues that are specific to this configuration:
• Stability of the power link.
• Common mode and differential mode noise propagation along the cable.
• EMI emissions of the power cable.

II. STABILITY OF THE DC POWER LINK
When both AC/DC and DC/DC converters chained together, the resulting transfer function involves the ratio between the output impedance of the AC/DC converter and the input impedance of the DC/DC converter. The stability of the system must be insured by proper matching of the converters impedances.
The impedance of the long cable used to link the converters is the dominant factor in the transfer function. The resulting impedance seen by the DC/DC converters towards the back end power supply is considerable, and the gain and phase margins become critical for the overall stability.

III. NOISE PROPAGATION ALONG THE LINK
The long DC power link is modelled as a multiconductor transmission line. As the impedances at both ends of the cable are low, the CM current gets amplified at some resonance frequencies as it propagates along the cable. The resonance frequencies must be known to make sure they do not match an eventual resonance of the front end DC/DC converter input filter.

IV. EMI EMISSIONS OF THE DC POWER LINK.
The power converters are a source of CM and DM noise. The noise source is identified as inductive in the near field region.
The DM noise is caused by the back end converter filtering, and by the front end

switching device. It is a source of electromagnetic interferences at low frequencies.
The common mode noise is contributed by the switching devices of both converters. As it returns through the ground, it is a potential source of strong EMI emission. The CM noise is the dominant source of EMI by several orders of magnitude when compared to the DM source.
In sake of a healthy electromagnetic environment of the experiment, the EMI emissions caused by CM and DM noise must be minimised. This is achieved by shielding the link; the shield is preferably grounded on both ends to provide and adequate return path for the CM currents in a minimised loop.

V. CONCLUSION

The DC power link used to feed the front end electronics of the Liquid Argon Calorimeter brings specific electromagnetic compatibility issues. The critical stability requirements are analysed and measured. The noise propagation along the line is measured to identify the resonance frequencies of the power link. The converters input and output filter must be such that they do not resonate at the link critical frequencies. The optimal shielding method that minimises the EMI emissions of this setup is last achieved by connecting the shield on both ends.

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Session Classification: Parallel session B4

Contribution ID: **53** Type: **Poster**

FAD - a Modular Assembly of the Fast and Portable Front-End Channels for the ALICE TRD Testing Bench

FAD-a modular assembly of the fast (320 MHz input pulse BW at 20 Db gain factor) and portable (120x30 mmˆ2 PCB per 4-input unit) front-end electronic channels, each aggregating linear adders, amplifiers, LED type threshold discriminators and output ECL shapers, has been designed to implement primarily the ALICE TRD testing bench. An initial series of the FAD based modules is prepared to provide triggering and registering events within a 160-output scintillator system, which verifies the ALICE TRD chambers by using cosmic or X-rays.
The FAD concept is mainly distinguished by a widely extended input dynamic range, allowing to registrate and to discriminate the detector signals of 1.1 ns rise time and 20 fC charge as minimum.

Summary

The present R&D is aimed at creating a newly compact, portable and rather fast
appliance, performing the mostly used input front-end functions of an analog channel within conventional detector electronics, and also allowing an experimentator to use it as an elementary unit while composing a stack of these channels in quantity over the limit assigned per unit.
In distinct from schematics of any wide spread manufactured signal discrimanators, the given FAD (Fast Adder/Amplifier/Discriminator) deliver physicists a feasibility of linear, prompt on the FAD inputs, summing any random selected pairs of detector signals with next amplifying pulse sums by a gain factor of 10 or 20.
This featuring leads to some FAD's advantages such as an extended dynamic range of accepted detector signals, and a better signal to noise ratio as well.
Another distinction is the FAD can admit signals coming both from a scintillator with an attached PMT, and/or from a MWPC-like detector; that goes right because of input high voltage capacitors foreseen as optionally mounted in the FAD boards.
A basic FAD unit handles up to 4 input signals accepted thru high-frequency on-board coaxial connectors. The unit contains two identical channels, where each channel comprises a linear adder of 2 detector signals from the adjacent inputs, a fast amplifier of the sum pulse, a high-speed leading edge discriminator (LED) of this amplified sum, and a fast ECL- compatible output signal shaper as well.
Due to application of the best slew rate commercial SMDs, like 1 GHz operational amplifiers and high-speed comparators from ADI, the FAD is able to support 320 MHz input pulse bandwidth at the 20 dB gain factor.
Therefore, the basic FAD unit, of the 120x30 mmˆ2 printed circuit board (PCB) dimensions, can be taken for a very fast and wide range front-end cell.
It goes to sum, to amplify, and to discriminate, according to regulated threshold settings, 4 detector signals of above 1.1 ns rise time and 20 fC charge as minimum,

producing 2 balanced (+/-) and their “OR” ECL signals in outcome.
The first series of NIM standard modules, based on the FAD units, is prepared to provide triggering and registering events within a 160-output scintillator detector system, which is under construction to verify the ALICE TRD chambers by exposing them in cosmic background or stimulated X-ray radiation.
Each of those NIM front-end electronic modules accumulates an assembly of 4 basic FAD units, thus providing 16-input (8-channel) segment of the system. There are also some additional schematics to elaborate an accurate setting of the controlled FADs’ threshold, and to convert all FADs’ “OR” ECL signals into 2 output NIM-level signals of an adjusted duration.
The series of 10 manufactured modules, lined in a system row, where discriminating threshold can be set either separately for each module, or jointly by a “daisy-chain” for a group of applied modules, completely cover all needs of the pointed 160-output(80-channel) ALICE testing bench, which should be considered like a pilot experience to further application and development of the FAD concept.

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Contribution ID: **54** Type: **Oral**

ALICE TRD Track Matching Unit with 12 Multi-Gigabit Inputs

Thursday 15 September 2005 16:50 (25 minutes)

The ALICE TRD trigger demands for high-speed computation and low-latency transmission of event data along the complete data path.
The module presented here is being developed for the detector's global online tracking unit which contributes to the L1 trigger of the experiment. It is an FPGA-based system utilizing PCI and 12 fibre-optical SFP transceiver interfaces, realized as a CompactPCI plug-in card. Three independent 8-Bit wide source synchronous LVDS interfaces allow for low-latency connection to other modules. The main FPGA is a Xilinx Virtex-4 FX chip which includes integrated multi-gigabit serializer/deserializer and PowerPC processor blocks. Three 36-Bit wide QDR2-SRAM chips provide a high-bandwidth memory used as event buffer.

Summary

The high demands in terms of computational power and data latency posed on the electronics of the LHC experiments require in many cases the development of specialized hardware. As available standard systems and network components are not directed towards the requirements of high energy physics, they do for example introduce a data delay that is not acceptable for low-latency trigger systems.

The module presented here is being developed for the transition radiation detector (TRD) of ALICE. It is an FPGA-based system utilizing PCI and 12 fibre-optical transceiver interfaces, realized as a CompactPCI plug-in card.

The experimental requirement driving the development of the presented module is the ALICE TRD trigger. Local online tracking data is shipped off of the detector modules situated in 6 layers via 1080 fibre-optical links. The trigger decision requires tracking over the 6 TRD layers and full event reconstruction in less than 2 microseconds. This demands for high-speed computation and low-latency transmission along the complete data path. To perform the FPGA-based tracking algorithm for different regions of the detector, 90 of the presented modules will be used.

The Compact-PCI (cPCI) specification describes an interface that is basically an adoption of the PCI specification to the 3U/6U sub-rack module form-factor. This form-factor is widely used in industrial and also high-energy physics applications. By implementing a 64 Bit wide 33 MHz cPCI interface, the presented module easily interfaces to COTS components like cPCI CPU boards and power supplies. This interface can be used not only for system management and testing, but also for medium-bandwidth data transmission in experimental test setups.

For high-speed data reception, the module features 12 separate serial interfaces implemented as SFP (small form-factor pluggable)sockets on the front panel. By utilizing the SFP form-factor, a wide range of commercially available SFP fibre-optical transceivers can be used. In the present version of the board, a data rate of up to 2.4 GBit/s per link is supported. The resulting total incoming data rate is 2.9 GByte/s. Three independent 8-Bit wide source synchronous LVDS interfaces allow for low-latency connection to other modules via backplane.

The main FPGA used on the board is a Xilinx Virtex-4 FX chip. This series of FPGAs provides not only up-to-date performance but also integrated multi-gigabit serializer/deserializer (serdes) blocks and PowerPC processor blocks. The integrated serdes blocks provide a fast and flexible interface of the serial inputs to the FPGA fabric. A second FPGA is used for system management and control tasks. Three identical 36-Bit wide QDR2-SRAM chips provide a high-bandwidth memory of 55.3 MBit size which can be used for event buffering. Running at 120 MHz DDR, the total memory bandwidth is 51.8 GBit/s. This is enough to sink the incoming peak data rate.

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Session Classification: Parallel session B6

Track Classification: Triggering

Contribution ID: **55** Type: **Oral**

Evolution of the TRT backend and the new TRT-TTC board

Thursday 15 September 2005 16:50 (25 minutes)

The Transition Radiation Tracker, made of 370'000 cylindrical straws, is a combined tracking and electron identification detector, part of the ATLAS Inner Detector at CERN's LHC. The back-end electronics, which are in charge of the communication with the front-end boards mounted all around the detector, are made up of two types of 9U VME boards. One type is the ROD boards, collecting, compressing and synchronising data from the front-end electronics. The second type is the TRT-TTC boards, transmitting the timing, trigger and control signals to the on-detector electronics using a special protocol. The current back-end of the TRT and its evolution will be presented, as well as the new TRT-TTC board.

Summary

The Transition Radiation Tracker, made of 370000 cylindrical straws, is a combined tracking and electron identification detector, which is part of the ATLAS Inner Detector at the CERN LHC. The TRT on-detector electronics is made of 2 types of custom asics, handling the analogue signals from the straws, providing a ternary encoded output (ASDBLR), binning the incoming tracking discriminator signal into 3.25ns bins and storing up to 6 microseconds of level 1 storage (DTMROC). This on-detector electronics is joined to the off-detector electronics via patch-panels in charge of data distribution.

The off-detector is comprised of three types of modules: the Timing,Trigger and Control (TTC) module, the ReadOut Driver (ROD) and the ReadOut Buffer (ROB). The ROD is a VME 9U module responsible for compressing the data and checking the synchronisation of the data coming from 240 DTMROCs. After processing the signals, the data is sent out to the ROB via SLINK transmitters.

The TRT-TTC is a VME 9U board responsible for the transmission of the timing and trigger signals (LHC bunch clock, Bunch Crossing Reset, Level1 Accept trigger, Event Counter Reset, test pulse for calibration) to ROD and on-detector electronics. It is also responsible for the communication with the front-end boards (register configuration, regular check of the registers contents). This is done using a special serial protocol, transmitted over up to 100 meters of cables via LVDS drivers and a special equalisation scheme. Each link between the TRT-TTC and the front-end communicates with up to 15 DTMROCs, and each TRT-TTC controls 40 links. One TRT-TTC is associated with two RODs in the same subrack, and controls 4/32 of one side of the TRT Barrel, or 2/32 of one end-cap.

To ensure complete coverage of the TRT detector, 50 TRT-TTC boards and 100 RODs will be produced.

The system must be modular to allow different partitions of the TRT to operate autonomously during the commissioning or the debugging phase of the experiment.

The TRT back-end electronics has recently been re-specified to conform to the above description and ensure that the volume taken up by the electronics is halved. This redesign consisted in overhauling the transmission schemes and the technologies of the system (use of optics, transmission of I2C signals over 100m of cables, ⋯). Some

of the interesting challenges that were identified during this phase will be discussed.

The new scheme of the TRT back end and its evolution will be presented, as will the new TRT-TTC board.

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Session Classification: Parallel session A6

Contribution ID: **56** Type: **Oral**

Design and Performance of the IceCube Electronics

Monday 12 September 2005 17:00 (45 minutes)

The first sensors of the IceCube Neutrino Observatory were deployed at the South Pole in January 2005 –60 modules on one string at depths from 1450 to 2450 meters and 16 modules in eight tanks at the surface. We present an overview of the electronics for IceCube and demonstrate their performance with experimental data obtained for cosmic ray muons. Analog waveforms of pmt signals are digitized and time stamped in themodules. Photon arrival times are determined to a precision of 4 nanoseconds for modules connected to the surface by twisted-pair copper wires nearly 3 km long.

Summary

Construction of the IceCube Neutrino Observatory reached a milestone in January 2005 with the deployment of the first deep-ice string of IceCube sensors and the first elements of the surface air-shower array, IceTop, located directly above IceCube. The completed Observatory will instrument a cubic kilometer of deep ice with at least 70 new strings plus the existing 19 AMANDA strings.

The major scientific goal of the Observatory is to detect both diffuse and point sources of high-energy neutrinos coming from galactic and extra galactic regions - in essence, to map the high-energy neutrino sky and contribute to the understanding of the origin of the ultra high energy cosmic rays.

IceCube incorporates novel electronic features that are suited for the requirement that it detect high-energy muons (E>100 GeV) and cascades at a remote location using sensors that are inaccessible once deployed. Electrical power is at a premium at the South Pole, making low power consumption in the sensor modules a priority. A robust system is required for long-term reliability at temperatures down to -55oC and to survive the stress of deployment, the subsequent refreezing of the ice around the modules, and the presence of electromagnetic interference from other installations.
At the same time, high quality of information from each event has to be combined with autonomous operation and calibration.

PMT signals are digitized using a custom integrated circuit called the Analog Transient Waveform Digitizer, or ATWD. The ATWD is a switched-capacitor array (128 samples deep) having four channels. Launched by a discriminator on the PMT signal, it digitizes (10 bits) all 128 samples simultaneously after waveform capture. The sampling rate is adjustable and set at 300 megasamples/s. With three ATWD channels set at different gains, dynamic range exceeds 150 photoelectrons for a time interval of 15 ns.

A combined FPGA and CPU (Altera Excalibur) and on-board memory are central to the system's operation, providing logic, timing, fast signal processing, data handling, and communication with the surface via ADCs and DACs. PMT signals receive a coarse time stamp from a stable (df/f < 10-10/s) local oscillator running at 20 MHz. This clock is calibrated within a few nanoseconds against a master clock on surface. The calibration procedure is automatic and repeats at typically ten-second intervals, with negligible consumption of bandwidth. A single copper twisted pair with a total

bandwidth of one Mbit/s serves two modules. Adjacent modules are connected to each other by a short twisted pair, which enables a local time coincidence. This effectively eliminates the consumption of bandwidth that would arise from sending the ˜800 Hz of PMT noise to the surface.

System performance is evaluated by detecting the cosmic-ray muons that penetrate from the surface to the detector below. Analysis of these events, as well as events induced by LED flashers in each module, indicate that the intrinsic time resolution is ˜4 ns. These results will be presented along with data indicating that the first IceCube string and IceTop surface modules are performing according to design and expectation.

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Session Classification: Plenary session P1

Contribution ID: **57** Type: **Poster**

The Sorter Electronic Boards for the Endcap Cathode Strip Chamber System at CMS

We report on the design and development of two electronics boards for the Endcap Muon Cathode Strip Chamber detector at CMS. One, the Muon Port Card, performs sorting "3 best patterns out of 18"and another one, the Muon Sorter, performs sorting "4 best patterns out of 36". The selected output patterns are sent to a higher level of the trigger system in a ranked order. Both boards are based on Xilinx FPGA devices. The functionality of the sorter boards and results of recent bench, integration and beam tests are presented.

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Contribution ID: **58** Type: **Oral**

Operational Experience with the CDF Run II Silicon detector

Tuesday 13 September 2005 10:10 (25 minutes)

The CDF Silicon Vertex detector consists of three subdetectors: SVX-II, ISL and L00. Altogether it consists of 8 layers of Silicon with more than 750000 readout channels. This detector is essential for CDF's high precision tracking and is vital for the forward tracking capabilities and the identification of heavy flavor decays. After four years of data taking in Run-II and a delivered luminosity of almost 1 fb-1 a summary of the operational experiences with a silicon detector at CDF is given.
Besides being very important for the tracking, the Silicon detector also plays a vital role in Level 2 decision of the CDF Trigger system. Results from off-line reconstruction showing the detector resolution and tracking efficiency are presented as well. Finally aspects of the longevity of this Detector and the impact on the CDF physics program are presented.

Summary

The Run-II Upgrade of the Tevatron increased the center-of-mass energy from 1.8 to 1.96 TeV as well as the luminosity. The goal for Run-II is now around 8 fb-1. To take advantage of this, a larger Silicon detector was designed. The SVX-II increases the coverage of the interaction region by a factor of two and adds the capability of having 3D hits. It consists of six bulkheads, each one consists of 12 wedges. Each wedge consists of 5 layers of double-sided silicon. To increase the impact parameter resolution, the L00 was added. It is mounted on the beam pipe inside of the SVX-II. It consist of radiation hard single sided silicon and has 48 ladders altogether. The ISL extends coverage in eta and adds additional tracking points as a link between SVX-II tracks and the Central Outer Tracker. The ISL consists 296 double-sided ladders arranged in three barrels, the two forward barrels having two layers, the central barrel having only one.

The readout chips and the DAQ are common for all detectors. The central component of the readout is the radiation hard 128 channel SVX3D chip. It consists of an analog frontend with a 46 capacitor cell deep pipeline which samples the data every 132 ns and a digital backend containing ADCs. The clear separation of the two parts allows the deadtimeless operation of the chip. Five ladders are connected to one Portcard, which serves as an interface between the ladder and the DAQ/power supply side. It distributes the DAQ commands to all attached ladders,as well as low and high voltage. It also converts the data from the chip into an optical signal, which is feed into the VME based DAQ. The cooling and power supply interlock systems are as well shared between all three subdetectors.

Commissioning off the whole system started in 2001 and it took significant effort to become operational. Problems encountered included:

-Complications during the installation
-A lack of testing for the cooling system under operational conditions. The

blocked ISL cooling lines remained undetected. Clearing them
was a challenging task.
-The common-mode noise in L00 severely affected its performance.
-The optical readout system turned out to be very sensitive in matching
transceivers and receivers.

These problems have been addressed Currently 92% of the ladders are
powered and 84 % deliver data without errors. During operation some new failure
modes were found and studied.
-Loss of wire bonds due to Lorentz forces on the wire bonds. Synchronous trigger
conditions resonated the wire bonds, which lead to failure.
This has been mitigated by a dedicated resonance detection system.
-Beam incidents damaging the chip.
-Single event upsets in the power supplies and DAQ boards in
the collision hall.

The silicon sensors are operated at a S/N of about 11-15 depending on the
ladder type. With this high S/N, the single hit efficiency is
above 99 %. As luminosity increases, a continuous effort is taking place to
make Silicon readout as fast as possible. A concern for longevity is the
amount of radiation damage to the system. With the current luminosity
prospects for Run-II, the damage to the sensors is the prime concern and a
continuous effort takes place to measure the radiation damage the system has
already accumulated.

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Session Classification: Plenary Session P2

Contribution ID: **60** Type: **Poster**

Advanced Automatic Testing and Calibration System for ATLAS CSC on Detector Electronics.

The ATLAS muon spectrometer will employ Cathode Strip Chambers (CSC) to measure high momentum muons in the extreme forward regions [1]. The on-detector electronics for the ATLAS CSCs performs amplification, analog buffering, and digitization of the charge signals from individual cathode strips. We present production test architecture for on chamber electronics comprising of custom highly programmable 192 channels pulse generator, and a PCI technology based advanced data acquisition and control system: Read out and Test Amplifier Shaper Module (ASM), PCI Acquisition and Control (RATPAC). We also report progress on production and testing of the electronics.

Summary

I. Introduction:
The CSC system is designed to measure high momentum muons in the extreme forward regions (pseudorapidity 2.1 < |⊠| < 2.7) of the ATLAS detector [1]. Its principle of measurement is to determine the hit coordinates by interpolating charge deposited on adjacent strips. Those strips are coupled to the preamplifier and shaper ASIC designed in Agilent Technologies 0.5 μm CMOS technology. Second set of on detector signal processing electronics module, called Amplifier Shaper Module II (ASM-II) is responsible for analog storage, digitization of AC-coupled preamplifier outputs and transmission of the digitized data to off detector Readout Device (ROD). Those modules are currently under production and testing phase. Production testing involves functional testing and calibration of 30720 channels on each type of modules, effectively 61440 channels in total. An automatic testing and electronics calibration system is developed at BNL. The system has two main hardware components and LabView based Data Acquisition and Control Software (DACS). Hardware includes a Highly Programmable 192-channel Charge Injector (HPCI) and Peripheral Component Interconnect (PCI) Acquisition and Control, Read out ASM and Test (PACRAT) custom designed printed circuit boards (PCB).

II. HPCI

HPCI is programmable via parallel port on a Windows PC to configure any random combination of 192 channels. Programmability is incorporated in the DACS. Amount of injected charge is controlled by on board 12 bit Digital to Analog Converters (DAC), programmable via DACS. HPCI fits in a standard 19”test rack and the pack of ASM-I and ASM-II modules can be easily plugged into the front panel for testing.

III. PACRAT
PACRAT is a PCI Version 2.1 compliant data acquisition and control PCB. It supports PCI to and from local data transfers up to 70 Mb/sec. It has two independent DMA channels with scatter-gather capability. It is supported by low level PCI drivers for MS Windows and Linux. PACRAT contains two high speed 4MB Static Random Access Memories (SRAM) banks. It has two HDMP-1024 Giga bit link (G-link) receivers to receive data from and one HDMP-1022 G-link Transmitter to send readout control signals to the ASM-pack under test.

IV. DACS
DACS is a Lab View based interface program developed to control and acquire data

from PACRAT, and also send signals to HPCI. The program also runs real time display and statistical analysis on ASM-Pack outputs. It records calibration data for every ASM-Pack into the production database.

V. Status
Complete setup for testing ASM-packs is functional and being currently used for production testing and production test results will be available by the time of the conference.

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Presenter: Mr JUNNARKAR, Sachin (Brookhaven National Laboratory)

Contribution ID: **61** Type: **Oral**

Advanced Front End Signal Processing Electronics for ATLAS CSC System: Status and post production performance.

Thursday 15 September 2005 15:15 (25 minutes)

The ATLAS muon spectrometer will employ Cathode Strip Chambers (CSC) to measure high momentum muons in the extreme forward regions [1]. Preamplification of the charge on the strips is performed in the Amplifier Shaper Module I. Amplifier Shaper Module II performs the analog buffering, digitization of the charge signals from individual cathode strips and multiplexes the data into two fiber optics links running at 1 Gbps each. We present the design architecture of the complete front end electronics chain and its performance. We also report on the production and testing status of overall on detector electronics.

Summary

I. Introduction:
Cathode Strip Chambers (CSC) form the first station of the endcap muon spectrometer in the ATLAS experiment. The CSC system consists of 32 four-layer readout planes of 192 x- and four-layer readout planes of 48 y-strips each. Each CSC is served by 5 front end electronics packs called Amplifier Shaper Module Packs (ASM-Pack), which consist of two ASM-I and one ASM-II printed circuit boards (PCB). ASM-Pack together employs 4 different custom designed Application Specific Integrated Circuits (ASIC) fabricated using Agilent Technology (AT) 0.5 μm CMOS, Single Poly, Linear Capacitor, Triple metal process, along with a switched-capacitor array analog memory [2] in a radiation-hardened 0.8□m CMOS process and various COTS components. Both PCBs use radiation hard electronic circuits consistent with the ATLAS radiation policies.

II. ASM-I
A CMOS multi-channel ASIC was developed for charge amplification and signal shaping. Bipolar shaping and 70 ns shaping time were chosen to minimize the effects of noise and pileup. In the 25-channel Preamplifier/Shaper, the NMOS input FET of the preamplifiers, DC feedback circuit and pole-zero compensation circuits were optimized to provide lower parallel and series noise to the front-end signal chain, staying within the allocated power budget [1].
Each ASM-I consists of 4 of the above mentioned ASICs processing signals from 96 cathode strips and its output is AC coupled into ASM-II for analog storage, digitization and transmission to off-detector ReadOut Driver (ROD)[3]. The ASM-I also consists of CERN developed LHC-7913 voltage regulator from ST microelectronics and three stages of Electro-Static Discharge (ESD) protection for each channel.

III. ASM-II
ASM-II serves total of 192 channels from two ASM-I. For analog storage, the HAMAC Switched Capacitor Array (SCA) ASIC [2] is used. This chip originally developed for the ATLAS liquid argon calorimeter, has a separate "muon"mode which allows it to function as a 12-channel, single gain memory rather than the 4-channel, tri-gain mode used in the calorimeter. SCA cells are written at 20 MHz and read-out upon level 1 trigger to a 12 bit Analog to Digital Converter (ADC) AD9042 at 6.67 MHz. ASM2MUX, a digital multiplexer ASIC, converts 24 bits from two ADCs at 6.67 MHz

into 4 bits out at 40 MHz. Control signals and clocks for SCAs and ADCs are distributed through MC10H116 Positive Emitter Coupled Logic (PECL) buffers, differentially to keep digital noise to a minimum. Custom clock fan-out ASIC is used to distribute clocks to ASM2MUXs and on board Giga bit optical links (G-Link). Seven LHC-7913 voltage regulators on ASM-II distribute power to ASM-I and ASM-II. The data from the chambers are transmitted to and control signals for readout of the board are received from off detector ROD over G-Links, consisting of AT HDMP-1022, AT HDMP-1024 and SDX-19-4-1-S optical transceivers. Sparsification, event building, and other tasks involved in resolving the hit co-ordinates with a resolution of approximately 60 μm are performed on the ROD [3]. The RODs are also responsible for generating the fast clock and control signals and distributing them to the ASMs, which function as slaves.

IV. Status:
Production of the front end electronics for the ATLAS CSCs is nearing completion. Post production results will be available at the time of the conference.

[1] P. O'Connor "Readout Electronics for a High-rate CSC Detector"Proceedings of the 5th Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA 20 - 24 September 1999
[2] D. Breton et al., "HAMAC, a rad-hard high dynamic range analog memory for ATLAS calorimetry", PROCEEDINGS of the Sixth Workshop on Electronics for LHC Experiments Krakow, Poland, 11 - 15 September 2000; P. O'Connor "Adapting the Liquid Argon Calorimeter SCA for use with CSC BNL"2-Feb-99: http://atlas-csc.inst.bnl.gov/Adapting_LAr.pdf
[3] I. Gough Eschrich "Readout Electronics of the ATLAS Muon Cathode Strip Chambers". In press.

Authors: Mr KANDASAMY, Anand (Brookhaven National Laboratory); Dr O'CONNOR, Paul (Brookhaven National Laboratory); Mr JUNNARKAR, Sachin (Brookhaven National Laboratory)

Presenter: Mr JUNNARKAR, Sachin (Brookhaven National Laboratory)

Session Classification: Parallel session B5

Track Classification: Tracking

Contribution ID: **62** Type: **Oral**

Irradiation tests of the complete ALICE TPC Front-End Electronics chain

Tuesday 13 September 2005 14:40 (25 minutes)

The ALICE TPC Front End Electronics will be operated in a radiation field of up to 800 hadrons/cm2sec. SRAM-based FPGAs are used on the Front-End Cards (FEC) and the Read-out Control Units (RCU). Several irradiation tests of all components on the cards have ensured that the components selected are able to withstand the radiation environment, but have also shown that single event upsets will occur in the FPGAs. As system stability and endurance are major concerns, effort has been put into making the design radiation tolerant, for instance by using the active reconfiguration option as given by the Xilinx Virtex-II pro FPGA. The radiation tolerance of the final system will be verified by irradiation in a neutron beam at TSL

Summary

One single node of the TPC Front End Electronics chain consists of up to 26 Front End Cards (FECs) connected to a Read Out Control Unit (RCU). A Detector Control System (DCS) board and a Source Interface Unit (SIU) of the DDL sit on top of the RCU board. The DCS-board is in charge of monitoring and controlling the system, while the RCU, SIU and the FECs are part of the data-path of the system. Each card is equipped with an industry standard SRAM based FPGA and peripheral components.

SRAM-based FPGAs are chosen because this technology offers great flexibility, but as the Front End Electronics will be operated in a radiation environment of up to 800 hadrons/cm2sec, single event upsets in the configuration memory is a major concern.

Several beam tests have been performed so that the best suited components for a radiation environment are chosen. Proton beams at Louvain, at the Cyclotron in Oslo and at TSL in Uppsala have been used to test Altera, Xilinx and Actel FPGAs, as well as different power regulators and other components. The number of single event upsets in the FPGAs has been carefully registered, and the results of these tests have been important in the choice of FPGA in the final hardware design. The beam tests that typically last for about hours are performed with much higher intensities than what the system will be exposed to in real-life. This gives a dose that is equal or higher to what the electronics is exposed to during the lifetime of the experiment, giving a test of the endurance of the components.

Because the RCU board is part of the data-path, it is of high importance that single-event upsets will not interrupt the operation of the firmware. To minimize the risk of this, a Xilinx Virtex-II Pro FPGA was chosen because it offers an option of active reconfiguration. Active reconfiguration means that the configuration memory of the FPGA can be refreshed without having any effect on the operation of the firmware in the FPGA. It is also possible to read back the configuration data and validate it with the original bit-stream. On the RCU, this feature is supported by adding an auxiliary flash based FPGA and a Flash memory, both which are radiation tolerant. The configuration files are stored on the flash memory and the auxiliary FPGA communicates with the configuration pins on the

Xilinx FPGA, configuring the FPGA either from the Flash memory or the DCS board.

Beam tests of the DCS-board itself has been performed with a proton beam at TSL in Uppsala. The complete setup, including FECs, RCU, DCS, SIU and Trigger system will be tested using a lower intensity neutron beam at TSL in order to verify the radiation tolerance. At this beam test the system will run normal operation with data-taking, and the software and firmware used are fully functional prototype versions of the final design.

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Presenter: Mr RØED, Ketil (Faculty of Engeneering, Bergen University College, Norway)

Session Classification: Parallel session A2

Contribution ID: **63** Type: **Poster**

Optical Multiplexer Board Final 9U Design for ROD/TileCal System

TileCal is a redundant data acquisition system. Two optical fibers carry the same data from front-end electronics to ROD system. This is necessary because of radiation phenomena could cause malfunctions inside front-end electronics, and bit and burst errors over data ready to be transmitted to ROD motherboard. Unfortunately, ROD card has only one input connector for each data, because the original design responds to initial specifications.
Optical Multiplexer Board final module has been designed to readout redundant output data from FEBs and send correct data to motherboards of the RODs. The motherboard design is a 9U VME64x slave module which has eight channels.

Summary

TileCal is the hadronic calorimeter of the ATLAS experiments. It consists, electronically speaking, of 10000 channels to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the data acquisition system (DAQ) following the assertions of a three level trigger system.
In the acquisition chain, place is left for a system which has to perform pre-processing and gathering on data coming out after a good first level trigger before sending them to the second level. This system is called the Read Out Module (ROD).
TileCal is a redundant data acquisition system. Two optical fibers carry the same data from front-end electronics to ROD. This is necessary because of radiation phenomena could cause malfunctions inside front-end electronics, and bit and burst errors over data ready to be transmitted to ROD card. Unfortunately, ROD card has only one input connector for each data, because the original design responds to initial specifications.
Our primary target is to improve error tolerance, designing a pre-ROD card, called Optical Multiplexed Board (OMB), able to analyze two fibbers, both of then carrying the same data, to provide the correct one to the ROD input.
The interest of this project was justified in February 2003, when a preliminary study appeared. This proposal shown a solution for OMB based on exhaustive on-line analysis of the data carried by both of the fibbers, using FPGAs for implementation. This architecture was called as “MiniROD“, because it follows a ROD-like design
Universidad de Valencia –IFIC (Spain) team showed the greater interest to deal with this project, to make a first prototype to study technical viability. In particular, the main goals are:
• Fibberoptic switching to take advantage of redundancy
• Obtain real (production) costs
• Have a development platform (hw - sw)
• Try different alternatives for data error analysis (CRC, etc.)
A new functionality for OMB was proposed by IFIC team. Since they have design responsibilities about ROD project, it was suggested a function mode called “Data Injector Mode”, to use the OMB like data pattern injector towards ROD for test and

verification uses.
Optical Multiplexer Board final module has been designed to readout redundant output data from FEBs and send correct data to motherboards of the RODs. The motherboard design is a 9U VME64x slave module which has eight channels.
This project started in October 2004. The construction of a final 9U OMB prototype is about to finish today. It is anticipated to have it on time for verification next testbeam at CERN in Summer 2005.

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Contribution ID: **67** Type: **Poster**

Test Station for the LHCb Muon Front-End Boards

This document describes hardware and software of a station developed to test the LHCb Muon Front-End Boards (FEBs) for MWPC and GEM chambers. Such boards are made up of two Amplifier, Shaper and Discriminator (ASD) ASICs and a read-out and control ASIC, accessible via I2C based data transfer protocol. Such station allows bench tests of front-end readout circuitry using the same facilities which will be used for their supervision, more a charge injection and a custom read-out boards, and a Win API C program (to control and analysis data), achieving a user friendly system which will be utilized in the course of chambers and readout electronics tests. The main parameters to be considered are: data transfer operation, board connectivity, sensitivity, offset, and noise. A brief summary of the first results obtained during its development and implementation is also featured.

Summary

The LHCb Muon System will be made up of 7500 16-channel Front-end Boards (FEBs), each hosting 2 Amplifier-Shaper-Discriminator (ASD) ASICs, called CARIOCA (Cern And RIO Current-mode Amplifier), and a supervisor ASIC (DIALOG, DIagnostics, time Adjustment and LOGics). On a FEB, called CARDIAC (CARioca and DIAlog Connection), two CARIOCAs are managed by a DIALOG, which is also the first recipient of the channels output by CARIOCA, in the readout chain. The LHCb Muon chambers and circuits are currently entering the production stage and most of their testing procedures require usage of FEBs. The system described has been developed to test and measure the FEB characteristics in a stand-alone setup, to allow a flexible adjustment of their parameters during an on-chamber characterization. Possible future improvements include: a database of FEBs characteristics and an on-site testing facility, both for control purposes.

The system allows testing, measurement and diagnostics of several FEB parameters by means of charge injection, alternative FPGA based read-out equipment, I2C data transfer and signal analysis. Various algorithms have been implemented to perform a thorough test of the readout apparatus: connectivity, register access, offset, noise, sensitivity. A noise rate-versus-threshold algorithm (rate-method) is being evaluated, as a solution to verify the ASD response in the field; this last test is going to be implemented in the FE Control System where it should undergo verification.

The main building blocks of the set presented are 4 boards and a Win32 API to a C program. Data transfer is ensured by CANopen and I2C protocols. The CANopen protocol is handled by a commercially available Kvaser PCI adaptor while a VME 6U module (Service Board, SB) implements the I2C protocol. A SB relies mainly on 4 replicas of a module called ELMB (Embedded Local Monitor Board, based on Atmega128 microcontroller) and a Flash Memory based FPGA by Actel. A different card, accessible via I2C, has been implemented to inject charge in the range of a few fC (Injection Board) into the ASD, and finally, a board based on the same FPGA as the SB is used to read the signals generated by the FEBs under test (Counting Board). The Injection Board contains 16 channels and its circuitry permits to set the

injected charge by means of writing into its DAC registers, to mask out some chosen channels, to adjust injection rate and to inject either positive or negative charge. A Counting Board receives differential signals from the FEBs and processes data by means of counters and it transfers data using a simple I2C implementation. This test station can test either kind of FEBs, on MWP and GEM chambers in the LHCb Muon subdetector and the first prototype has been manufactured and characterized. We present here its circuitry and results to show its implemented features and discuss its future possibilities.

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Contribution ID: **68** Type: **Poster**

Performance Studies of the radiation hard 0.25µm BEETLE frontend chip for the LHCb Silicon Tracker

The BEETLE frontend chip is a 128 channel radiation hard analog read-out chip using commercial 0.25µm CMOS technology designed by the ASIC lab in Heidelberg. The BEETLE is used at the LHCb experiment, currently under construction at the Large Hadron Collider at CERN. It operates at 40 MHz and saves events into a pipeline with a maximum latency of 160 clock cycles.
We summarise here the results of a series of testbeam experiments on prototype ladders for the LHCb Silicon Tracker with a 120 GeV/c π^- beam. The performance of the BEETLE frontend chip is studied with respect to the highly constrained requirements for LHC.

Summary

The BEETLE frontend chip will be used to read out silicon strip detectors in the main tracking devices of the LHCb experiment, e.g. Vertex Locator (VELO), Pile-Up, Inner Tracker (IT) and Trigger Tracker (TT). The BEETLE design foresees a variable shaping time in order to adopt for the different geometries and hence strip capacitances of the silicon sensors to be read out. The total capacitance at the input node can be as high as 57pF as it is the case for the TT-station. Simulation studies show that a S/N ratio higher than 12 at a signal remainder in the next bunch crossing, 25 ns later, of less than 30% and 50% for the Inner Tracker and the TT-station, respectively, is required. In addition to the variable feedback resistance in the shaper, the feedback resistance in the preamplifier can be changed, as well as their bias settings.
We explored this parameter space with respect to noise, signal remainder, crosstalk and undershoot. These parameters are highly dependent on the total capacitance at the input node of the BEETLE preamplifier. By varying the trigger latency high statistics pulse shape scans were performed at different BEETLE settings.
Four ladders with different geometries were tested at the same time. Two were consisting of multigeometry sensors, on which three regions could be fully illuminated. This allowed to study the shaping performance as a function of both the internal BEETLE settings and the total sensor capacitance at the input node. An analytic function was derived to model the response of the BEETLE frontend in order to derive the various parameters. The detailed understanding of the response of the BEETLE frontend chip is important for the commissioning of the Silicon Tracker.
The fast read-out requirements imply the risk of signal loss by ballistic deficit. Bias voltage scans were performed for different shaping times to study whether full charge collection efficiency for all ladder thicknesses under test is achieved.
We found that the BEETLE performs well according to its requirements. In addition we gained a deeper understanding on the various sources of noise and crosstalk in our measurements. These studies were completed with additional laboratory measurements using a 1063 nm Nd:YAG laser diode and simulation studies.

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Contribution ID: **69** Type: **Poster**

Full custom Quad Ported Memory

The Quad Ported Memory (QPM) is the data memory for the four MIMD CPUs in the TRAP Chip. Which is part of the trigger system for the ALICE Transition Radiation Detector (TRD).
The QPM has 1024 data words each data word consists of 39 bits (32 data bits, plus 7 hamming bits) and is quad ported - each CPU can access the memory, reading or writing completely independent of the CPUS, which are connected to its other ports. It operates with 120 MHz and needs 0.58 mm2 area on the chip. It's implemented in a 0.18 µm CMOS process with six metal layers. The VDD voltage is 1.8 V and the power consumption is for all four ports working 39,6 mW and for no ports active 0,02 mW. The multiport architecture eliminates global busses and arbitration required for memory access, while saving area and power.

Summary

The Quad Ported Memory (QPM) is the data memory in the TRAP Chip.
The TRAP chip is a part of the ALICE Transition Radiation Detector (TRD). The TRD operates as trigger and tracking detector in the ALICE experiment. Therefore there are nearly 1.2 million analog data channels which are digitized at 10 MHz by 10 Bit ADCs within 2 µs. On this Data stream of 13 TByte/s a trigger decision has to be made within 6 µs. In the Trap Chip the pre-amplified analog data are digitized and digital filtered and preprocessed. Each TRAP Chip handles 18 channels plus 3 neighboring channels. In a second stage the TRAP chip performs a straight line fit on a subset of the data. Each Chip has four MIMD CPUs to compute four straight line fits in parallel. The QPM is the data memory for the four MIMD CPUs. The results of the straight line fit (called tracklet) are shipped to the Global Tracking Unit (GTU) which merges tracklets and gives the final trigger decision. 64224 Trap Chips will be used and integrated in the TRD.
The QPM has 1024 data words each data word consists of 39 bits (32 data bits, plus 7 hamming bits) and is quad ported - each CPU can access the memory, reading or writing completely independent of the CPUS, which are connected to its other ports. It operates with 120 MHz and needs 0.58 mm2 area on the chip. It's implemented in a 0.18 µm CMOS process with six metal layers. The VDD voltage is 1.8 V and the power consumption is for all four ports working 39,6 mW and for no ports active 0,02 mW. The multiport architecture eliminates global busses and arbitration required for memory access, while saving area and power.
The QPM consists of bit-cells, address decoders, write units, read units and the control logic.
The bit-cells are based on a normal six transistor SRAM bit-cell, but to allow multiple accesses the normal two pass transistors are supplemented with another 6 pass-transistor. So that each of the four ports has two pass-transistors. Also the size of the inner transistors is increased to ensure that the cell is strong enough to cope with all four ports simultaneously. The bit-cells are arranged in 128 rows and 312 columns. In each case 8 columns are combined and represent one of the 39

bits in the read or write data. This happens to save area and to get a better aspect ratio.
Each of the four ports has an independent address decoder. In every address decoder the higher 3 bits of the address selects one of the 8 columns and connect them to the write or read unit via analog multiplexers. The other 7 address bits select one of the 128 rows, by enabling the pass-transistors of the addressed bit-cells.
For each word bit there are four write units (one per port), which can overwrite the addressed bit-cells with the write data.
The read unit detects the stored value in the addressed bit-cells.
This is done in two steps. First the read unit is precharged, so that there is a good balance in the read unit.
Then the pass-transistors of the addressed bit-cells are enabled. Depending on the stored value they disturb the balance in one of two possible directions. A latching amplifier detects this unbalance, amplifies it and latches it until the next precharging.
Via amplifier buffers this values is given to the data-outputs and represent the read data. There are as many read units as writ units.
A single control unit controls the timing of addressing, writing,and reading. It contains two programmable delays, to cope with process variations.
The test results will be presented at the Workshop.

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Track Classification: Custom Integrated Circuits

Contribution ID: **70** Type: **Oral**

Quality Assurance System for the Endcap Module Hybrids of the ATLAS Semiconductor Tracker

Wednesday 14 September 2005 14:15 (25 minutes)

The quality assurance system for semi-industrial production scale of multichip hybrid circuits is presented. The hybrids are parts of the silicon strip detector modules of the Semiconductor Tracker (SCT) of the forthcoming ATLAS detector. The hybrid houses the readout and data transmission ASICs, providing the full functionality needed for binary readout of double-sided silicon strip detector modules. The hybrids are assembled in the industry using pretested components. The full quality assurance testing, including visual inspection, electrical testing and burn-in tests, is performed in the institutes of the SCT collaboration. The testing procedures and test results are presented.

Summary

The paper presents the quality assurance system used for qualification of the hybrids for the endcap silicon strip detector modules of the ATLAS Semiconductor Tracker (SCT). The two endcap parts of the SCT detector comprise 1976 detector modules. The required production scale ads new challenges to the quality assurance, which are not present during development and prototyping phase. The hybrids mentioned above are sophisticated electronic circuits used for readout double-sided modules built of silicon strip detectors. The bare silicon chips are mounted onto a flexible kapton printed circuit board, wrapped around a low mass carbon composite mechanical support together with passive components. The chips glued and wire-bonded on the hybrid are the twelve ABCD3T readout chips as well as the DORIC and the VDC data transmission and optical link driver chips, providing in total 1536 readout channels, with their data transmitted over two independent optical links.

The electronics mounted on the hybrids provides extraction, amplification, and discrimination of charge signals from silicon strip detectors, data derandomising and data compression as well as transmission of data to an external data acquisition system. The system design of the detector is fault-tolerant by design at many levels and many of the components may fail without rendering large detector portion unusable. The test chain of the components comprises the tests done for the individual components (ASICs and PCBs), functionality tests and parameterisation done after the assembly, and the burn-in test designed for catching possible infant mortality in the ASICs and other components on the hybrids and ensure long-term stability of the component. The hybrids were assembled in industry, where basic functionality and reception tests were performed. Further QA tests were performed by the SCT collaboration.

The test procedures were designed for maximising the rejection rate of faulty components and, in the same time, minimising the testing time. The test routines are composed of the series of visual test, electrical tests, and thermal cycling tests. The mechanical defects and most of the assembly errors are detected by visual inspection. The electrical functionality and parametric test use extensively the testability function built into the ABCD3T front-end ASICs. Tests are performed using the automated test software and custom-designed VME hardware, which makes it possible to run the tests at high speed without overloading the control PC. In

addition to finding and marking the defected channels the analogue parameters of each of the channels are measured and calibration factors are saved in the conditional database for further use. The burn-in test is performed at elevated temperature to speed up the development of possible infant mortality defects, and the final characterisation of the parameters is done at the nominal working temperature of the ATLAS SCT.

The QA testing of endcap hybrids was conducted at three sites: the AGH University of Science and Technology in Krakow, the Freiburg University in Germany and the Rutherford Appleton Laboratory in the UK. In the paper we will present the QA procedures, example of test results and statistical summary for the entire production.

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Session Classification: Plenary session P5

Contribution ID: **71** Type: **Oral**

Swift integrated signal processing architectures for CMOS sensors equipping future vertex detectors.

Friday 16 September 2005 11:55 (25 minutes)

Monolithic Active Pixel Sensor (MAPS) using standard low cost CMOS technology available from industrial manufacturers, have demonstrated excellent tracking performances for minimum ionising particles. The need for highly granular, thin and radiation tolerant pixel arrays equipping the vertex detector foreseen at the future International Linear Collider (and elsewhere) drive an intense R&D effort, aiming to optimize the intrinsic sensor performance and to obtain an appropriate swift and low noise electronics architecture for on-chip data processing. Besides this main issue, work on radiation tolerance and backthinning of the sensors is under way. The state of art of these developments will be exposed, emphasizing the main micro-circuit architectures under study and their critical design issues.

Summary

Future experiments at the International Linear Collider (as well as at RHIC and FAIR) call for highly granular, thin, radiation tolerant, fast and multi-layer vertex detectors installed very close to the interaction region. As compared to existing devices (CCDs, hybrid pixels), CMOS Monolithic Active Pixel Sensor (MAPS) may offer an attractive trade-off between granularity, material budget, radiation tolerance and read-out speed for high precision minimum ionizing particle (MIP) tracking. This type of sensor integrates the sensing element and the processing electronics on the same substrate. It is fabricated using standard CMOS processes available through many commercial microelectronics foundries. The device ability to provide charged particle tracking has been demonstrated on a series of MIMOSA (Minimum Ionizing MOS Active sensor) chip prototypes [1].

The detection of charged particles with a CMOS sensor relies on a key element made of an Nwell/P-substrate diode. The latter collects, through thermal diffusion, the charge generated by the impinging particle in the thin, mostly undepleted, silicon layer underneath the readout electronics (i.e. epitaxial layer). The charge collected by each diode is directly converted to an electronic signal at the pixel level. The particle tracking performance is limited by the leakage current of the charge collecting diode, which increases with temperature and absorbed radiation dose. As shown by existing MIMOSA prototypes, the sensors can be designed in order to provide a sufficiently high signal-to-noise ratio (S/N) to allow for a spatial resolution of about 1.5-2.5 μm and a detection efficiency in excess of 99%.

The signal processing (fully on-chip) micro-circuits is shared between the pixel volume and the edge of the sensor. The ambitioned sensitivity and S/N performance is best achieved by integrating a maximum of signal processing functionalities inside the pixels. This is accomplished by integrating low noise amplifiers, memories and correlated double sampling (CDS) circuits inside each pixel, translating into a high charge-to-voltage conversion factor and reduced fixed pattern noise. The required read-out speed is obtained by grouping the pixels in short columns processed in parallel. Each column is equipped with an ADC and sparsification micro-circuits integrated on the sensor edge. The design of the latter is guided by minimal surface and power dissipation requirements (in order to

minimize the material budget). Various signal sensing and processing architectures developed for future high precision vertex detectors (International Linear Collider, STAR upgrade, CBM, etc ⋯) will be presented. Their performances extracted from tests realised with a 55Fe source and MIP beams (CERN-SPS) will be shown and discussed. Besides this main issue, other current R&D topics will be addressed, such as the thinning of the sensors to a few tens of micrometers, due to their thin sensitive volume (typically ˜10µm).

Finally, an outlook will be provided on the next prominent steps of the micro-circuits design R&D.

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Session Classification: Plenary session P9

Contribution ID: **72** Type: **Oral**

Evaluation of the Radiation Tolerence of SiGe Heterojunction Bipolar Transistors Under 24GeV Proton Exposure

Tuesday 13 September 2005 14:15 (25 minutes)

For the potential use in future high luminosity application in HEP (e.g. the LHC upgrade), we evaluated the radiation hardness of a candidate technology for the front-end of the readout ASIC for silicon strip detectors. The devices were test transistors of various geometries manufactured in the first generation, IBM SiGe 5HP process. Current gain as a function of collector current has been measured at several stages: before and after irradiation with 24 GeV protons up to fluences of 1016 p/cm2, and after annealing at elevated temperature. The analog section of an amplifier for silicon strips typically has a special front transistor, chosen carefully to minimize noise and usually requiring a larger current than the other transistors, and a large number of additional transistors used in shaping sections and for signal-level discrimination. We will discuss the behavior of both kinds of transistors, with a particular focus on issues of noise, power and radiation limitations.

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Session Classification: Parallel session A2

Contribution ID: **73** Type: **Oral**

Pixel Multichip Module Development at Fermilab

Thursday 15 September 2005 11:50 (25 minutes)

The efforts of the Pixel Detector R&D group at Fermilab have been concentrated on meeting the requirements of the pixel detector for the BTeV experiment. In BTeV, the pixel detector would be located close to the beam, and all collected data would be read out for use in the lowest level trigger for track and vertex reconstruction every beam crossing. We present the results of the characterization of several preproduction pixel multichip modules. These devices were characterized for threshold and noise dispersion at different operating temperatures. The pixel modules were tested for bump-bond connectivity and calibrated with an X-ray source.

Summary

The Pixel Detector R&D group at Fermilab has been developing a pixel detector to meet the stringent requirements of the BTeV experiment. This pixel detector would be composed of 60 pixel planes of approximately 100x100 mm2 each, assembled perpendicular to the colliding beams and installed less than one centimeter from the beam. The planes in the pixel detector are formed by sets of pixel-hybrid modules of different lengths, each composed of a single active-area sensor tile and of one row of readout integrated circuits (ICs).

The BTeV pixel detector module is based on a design relying on a hybrid approach. With this approach, the readout chip and the sensor array are developed separately and the detector is constructed by flip-chip mating the two together. This approach offers maximum flexibility in the development process, the choice of fabrication technologies, and the choice of sensor material.

The building block of the pixel detector is the pixel multichip module, which is composed of three layers. The bottom layer is formed by a low mass high-density interconnect (HDI). The back of the pixel readout IC is in thermal and electrical contact with the HDI, while the top of the pixel readout IC is flip-chip bump-bonded to the pixel sensor. The readout IC pads are wire-bounded to the HDI. The large number of signals in this design imposes space constraints and requires aggressive HDI design rules, such as four impedance-controlled signal layers with 50μm width trace and 50μm trace-to-trace clearance.

The pixel detector would be employed for on-line track finding in the lowest level trigger system and, therefore, the pixel readout ICs would have to transmit data for all detected hits. This requirement imposed a severe constraint on the design of the readout IC, the hybridized module, and the data transmission to the data acquisition system.

Recent characterization results of several preproduction pixel multichip modules are presented in this paper. These preproduction modules were characterized for threshold and noise dispersion using an analog test pulse injected into their preamplifiers. The connectivity of the bump-bonds was tested using a radioactive source (Sr90), and the absolute calibration of the modules was achieved using X-ray sources. The pixel detector would be built at room temperature and operated at -5C, implying a significant thermal variation. For this reason we characterized the

electrical and mechanical performance of the pixel module at different operating temperatures ranging from -15C to 40C. Preliminary tests show that the preproduction pixel module meets or surpasses the electrical and mechanical requirements of the pixel detector for BTeV.

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Session Classification: Parallel session A4

Contribution ID: **74** Type: **Oral**

Trigger Region Unit for the Alice PHOS calorimeter

Thursday 15 September 2005 17:15 (25 minutes)

The electromagnetic Photon Spectrometer (PHOS) of ALICE measures electromagnetic showers up to 100 GeV with PbWO4 crystals and APD's placed a cold zone of -25 C. Readout regions of 448 crystals are combined as coherent trigger regions via analog signals which are processed by one FPGA-based, Trigger Region Unit (TRU). The signals are *22 analog sums with 100 ns shaping time, connected over equal length flat cables from 14 FEE digitizer boards to a centrally placed TRU board with an FPGA which receives all signals from the trigger region after 8 bit, 40 MHz conversion. Both level-0 and level-1 trigger algorithms are executed within the FPGA, consisting on charge summing over sample times and over 4*4 crystal windows. Due to external latencies, the level-0 decision is due after 300 ns processing time, whilst 5 us are available for more refined level-1 decisions. The trigger outputs are transmitted as 40 MHz Yes/No signals to the central trigger processor. The 10 layer TRU cards have been designed around a 50 kilogate Xilinx VirtexPro FPGA, with external reconfiguration logic, allowing to detect and correct single event upsets during operation. In view of further applications in Alice, the TRU is equipped with a level-0 multiplicity input and 1 Gbit/s serial outputs for building hierarchies of TRU triggers. Eight TRU cards are embedded together with 112 FEE cards inside the closed PHOS modules, necessitating water cooling for both TRU and FEE cards via surrounding copper cassettes.

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Session Classification: Parallel session B6

Contribution ID: **75** Type: **Poster**

The reflective memory board demonstrator of the SPARC control system

The demonstrator of the reflective memory board for the communication between the third and the second level PCs of the SPARC accelerator control system is presented.
The main building blocks of the reflective memory board are: a 32 bit x 66 MHz Master/Target PCI interface with DMA capabilities, a fiber optic full-duplex high-speed link and a 1 MByte Synchronous Static DPRAM.
The reflective memory mechanism is implemented in a fully transparent way in both directions. A message passing and remote interrupt generation procedure from one PC to the other is implemented too.

Summary

The SPARC accelerator under construction at the Frascati National Laboratories is dedicated to the realization of a Self Amplified Spontaneous Emission Free Electron Laser (SASE FEL).

The SPARC control system is a multiprocessor system divided in three hierarchical levels based on commercial and industrial PCs. The first consolle level implements the operator interface, the second supervisor level manages the control system shared memory and the third hardware level controls and monitors the machine.

The demonstrator of the reflective memory board for the communication between the third and the second level PCs is presented.

Each third level reflective memory board has an associated 1 MByte memory zone in the PCI memory space which is mirrored in a transparent way to the corresponding second level reflective memory board.

The reflective memory board is implemented on a standard 32 bit x 66 MHz PCI printed circuit board and can be logically divided in five building blocks: a Master/Target PCI interface with DMA capabilities, a serdes controller with data parity check, a DPRAM interface and reflective memory controller, a fiber optic full-duplex high-speed link and a 1 MByte Synchronous Static Dual Port RAM.

The PCI interface, the serdes controller and the DPRAM interface were implemented with an Altera Acex 1K 100 FPGA, for the DPRAM the 1 MByte Cypress CY7C0853V was chosen and the high speed link was implemented using a Texas Instruments TLK2501 serializer/deserializer circuit togherter with the Agilent HFBR-5720AL SFP optical transceiver for a maximum throughput of 160 MByte/s for each direction.

The reflective memory mechanism is implemented in a fully transparent way in both directions. If a location in the PCI memory space of the board is modified its data content is serialized from 32 to 16 bit and transmitted along the optical fiber, togheter with an header indicating the destination memory address, the memory transfer size and some control bits and a footer with a parity check.

The data received on the other side of the optical fiber are deserialized, checked for transmission errors and written on the on-board DPRAM.
In this way the receiving PC has always an up-to-date copy of the 1 MByte PCI

memory space of the transmitting PC.
In case of error a retrasmission request message is sent to the transmitting PC along the optical fiber.

The data from the transmitting PC are stored on the on-board DPRAM until they are requested, thus reducing PCI bus traffic.
The DPRAM interface and reflective memory controller logic is able to check data packet consistency too. In this way data corruption problems occurring when the RX PC is reading a memory block during a data transfer from the high-speed link can be avoided.

With the same mechanism used to mirror data from one PC to the other a message passing and remote interrupt generation procedure is implemented too.

Two different low level drivers were realized: a driver for linux operating system and a windows driver suitable to control the board with a LabView program.

The board can be connected both in a point to point and ring configuration.

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Presenter: Mr SABENE, Maurizio

Contribution ID: **76** Type: **Oral**

The TRAcklet Processor chip for the ALICE TRD

Tuesday 13 September 2005 15:30 (25 minutes)

The ALICE TRD has over 1,2 million analog channels that will be digitized at 10MSPS with 10-bit resolution. We have developed a TRAcklet Processor (TRAP) ASICs implementing 22 extra low power ADCs, digital filters, four RISC processors with shared memory, slow control serial interface and fast parallel 4-in 1-out readout tree ports.
Together with the preamplifier chip they build a low-cost custom Ball Grid Array (BGA) Multi Chip Module (MCM), which is directly soldered on the readout board.
Fully automated Wafer- and MCM- tester were developed. The TRAP design is finalized and the production is started.

Summary

The ALICE Transition Radiation Detector (TRD) consists of 6 layers of drift chambers and radiators, arranged in a barrel geometry in the central part of the ALICE heavy-ion experiment at LHC. It is designed to track all charged particles and to perform electron identification. It has the unique capability to provide a fast electron trigger within 6 us after the collision. The TRD has more than 1.2 million analog channels, which are digitized at 10 MSPS with 10 bit resolution. The high number of channels implies that the analog and most of the digital processing must be done within the detector. The analog amplification and shaping is implemented as a 0.35 um AMS analog chip (PASA). The ADCs and the digital part of the MCM are implemented as second chip in a 0.18 um UMC process. Both chips build a low-cost Ball Grid Array (BGA) Multi Chip Module (MCM), which looks like a commercial BGA chip. The ALICE TRD detector uses about 65000 such MCMs.

The signals from the PASA are digitized by 21 10 bit ADCs at 10 MSPS. The ADC data pass through several filter stages: correction for nonlinearity in PASA/ADC, pedestal and gain correction, tail cancellation, crosstalk suppression.

The position within one time sample is reconstructed using the charge sharing in a group of three adjacent pads. The about 20 space points are subject to a straight line fit. Some part of the calculations is done during the drift time, the rest later in the four RISC CPUs.
The CPUs write the resulting track data as 32 bit word to the parallel output of the chip. Within 600 ns all this information is collected and shipped to the global tracking (GTU).
The root of the readout tree for a group of about 64 MCMs is connected to a 2.4 Gbit optical transmitter. It combines the track segments of the different detector layers into tracks within 2us.

The four CPUs have common quad ported data memory and individual

instruction memory blocks. In order to save power a global state machine properly gates the LVDS cells and all clocks in the design. A special designed slow control serial network is used for all configuration of the chip (registers, memories). It runs at 24 Mbits/s and can address up to 126 chips in a daisy chain. An FPGA board with RISC processor capable of running Linux with Ethernet interface acts as a configuration master.

For the production of the TRAP and the MCM fully automated Wafer- and MCM- testers were developed.

We have working chips and their designs are ready for production.

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Session Classification: Parallel session A2

Track Classification: Tracking

Contribution ID: **77** Type: **Poster**

A Megahertz Trigger Farm with a Data Flow Control System

Addressing the needs for high-transaction, low-latency, high-selectivity trigger systems at LHC, a solution for a high-performance scalable trigger processing farm based on commodity computing nodes interconnected with a ring-based network is proposed. Running such a massive parallel system at input rates above megahertz requires flow control to prevent congestions at the receiver from ever occurring. A hardware data flow control system comprising a centralized scheduling unit and a custom serial network interconnecting the scheduler and a scalable number of distributed feeding nodes has been realized. It has been measured the maximum input data rate for 128 byte packets is in excess of 2 MHz.

Summary

With their high number of channels, high event rates and studies of rare events, the experiments at the LHC apply new requirements to data acquisition systems. A solution for a high-performance scalable trigger processing farm based on commodity computing nodes interconnected with a ring-based network implementing a 2-D torus topology is proposed. The system is capable of processing small data sets of less than 200 byte at input rate of more than a megahertz. Key system features are high transaction rate, low maximum latency and scalability. Data transport is implemented completely in hardware, thus excluding any CPU overhead.

Transfer of single event data consists of multiple remote memory write transactions executed by distributed feeding nodes against one and same remote computing node.

Such a many-to-one system is prone to congestions at the receiver since simultaneous reception of data from multiple sources at the destination leads to overflow in the receiver's input queues and subsequent retry traffic, which results in considerable system performance degradation. The maximum input data rate in a 30 nodes system prototype with a basic flow control mechanism realizing static destinations allocation has been measured to be limited up to about 1.3 MHz. A more sophisticated data flow control system has been realized, which led to significant performance increment.

The flow-control system employs mainly on two devices: a centralized scheduling unit, which realizes dynamic allocation of free computing nodes such that no congestions in the system occur, and a custom scalable point-to-point serial network that interconnects the scheduler with the feeding nodes to initiate transfer of data to the right destination at the right time.

By reason of the input data rate (a microsecond), the scheduler has

been designed completely in hardware. Considering the requirements for performance and scalability, and the limited edition, the scheduler has been implemented in a big FPGA. Furthermore, the device has been realized as a PCI expansion board to be easily integrated into the system. The same custom-made multipurpose PCI card has been used to implement the DMA engines needed in the feeding nodes. The card has found a number of other applications throughout the system prototyping and test phases.
The communication channel between the scheduler and the transmitting nodes is implemented using LVDS signaling over standard STP cables as this solution has been found most suitable to realize the desired box-to-box fast, cheap, simple and reliable communication.
The maximum input data rate in a flow-controlled system prototype has been measured to be 2.14 MHz, and the number of retries in a transmitting node transferring 128 byte packets at the maximum input data rate has been measured to be zero.
Measurements in an intentionally congested system have shown intensive retry traffic and odd behaviour. It has been proven that the maximum data rate in a properly flow-controlled heavy-loaded system is limited by the transmitter's maximum data throughput but not due to congested receivers.

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Contribution ID: **78** Type: **Oral**

Beam Phase and Intensity Monitor for the LHCb experiment

Thursday 15 September 2005 17:40 (25 minutes)

The LHC RF clock is transmitted over kilometres of fibre to the experiments where it is distributed to thousands of front-end electronics boards. In order to ensure that the detector signals are sampled properly, its long-term stability with respect to the bunch arrival times must be monitored with a precision of <100ps. In addition it is important to monitor the LHC bunch structure and the trigger conditions by measuring the intensity of each bunch locally in the experiment.
For this purpose a beam phase and intensity acquisition board (BPIM) is being developed for the Button Electrode Beam Pickups which will be installed on both sides of all the LHC interaction points. The board measures the two quantities per bunch, and processes and histograms the information in an onboard FPGA. The information is read-out by the Experiment Control System and directly fed to the LHCb Timing and Fast Control system.

Summary

The LHC bunch clock frequency of 40 MHz is transmitted to the experiments via a network of optical fibres which is partly based on non-phase-stabilized fibres. In the case of the LHCb experiment the non-phase stabilized distance is about 4.6km. In LHCb the bunch clock is locally distributed by the Timing and Fast Control system to all the detector front-end electronics where it is used to sample the detector signals. In order to sample the detector signals, which typically have a maximum plateau of a nanosecond, at the optimum point, the timing system provides several means of making a complete timing alignment at the level of 50ps. Since the LHC fills are expected to last for more than ten hours, it is of extreme importance that the phase of the LHC clock remains stable with respect to the bunch arrival times.
However, several effects such as temperature variations influence the phase. Measurements show that the time drift on the transmission fibres could be as large as 200ps over a period of 24 hours, and up to 8ns have been observed over a period of a year. Clearly the phase must be monitored and regular timing alignments must be performed.

In order to monitor the bunch arrival times with respect to the clock a special Button Electrode beam pickup will be installed 180m away from the interaction points on each side. Since the pulses of the four buttons of each pickup will be summed, the signal per crossing becomes independent of the position of the beam and thus also allows measuring the currents of the bunches. This is of high interest since the LHC bunch structure can be monitored and the bunch currents can be correlated with the actual physics triggers.

The current paper proposes a beam phase and intensity acquisition board (BPIM) capable of performing the two measurements per bunch crossing. The analogue unit of the board consists of a separate circuit for the phase measurement and the intensity measurement. Since the shape and the amplitude of the pulse will vary, the phase measurement circuit contains a special pulse detect circuit which is

independents of the shape, and the intensity measurement circuit contains a programmable gain amplifier. The digital processing of the board is based on an FPGA which performs response linearization, averaging and histogramming in the memory of the FPGA of the measurements. The control interface is based on an embedded Credit-Card-sized PC from Digital Logic. The controller has Ethernet and is one of the standard interfaces to the Experiment Control System in LHCb. The control of the analogue circuits, such as gains and thresholds, is handled through the FPGA. In addition to reading out the measurements via the control interface, they are also output on the front-panel of the board at 40MHz with LVDS. The latter allows directly interfacing the board to the Timing and Fast Control system in order to add the bunch current information to the data of each event.

The board is in development. A first full design has been made and simulated. One of the authors* has also implemented and tested the design in the context of an intensity monitor for the CERN PS accelerator.

(* G. Kasprowicz)

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Session Classification: Parallel session B6

Contribution ID: **79** Type: **Oral**

ATLAS Level-1 Trigger Timing and Monitoring

Tuesday 13 September 2005 11:50 (25 minutes)

The ATLAS detector at CERN's LHC will be exposed to proton-proton collisions at a bunch-crossing rate of 40 MHz. In order to reduce the data rate, a three-level trigger system selects potentially interesting events. Its first level is implemented in electronics and firmware, and aims at reducing the output rate to under 100 kHz. The Central Trigger Processor (CTP) combines information from the calorimeter and muon trigger processors, and makes the final Level-1 Accept (L1A) decision.

The CTP is a central element in the timing setup of the experiment. Several strategies are presented for timing-in the experiment, which is done with respect to the Level-1 trigger, with respect to the experiment, and with respect to the world.

Furthermore, the monitoring of the Level-1 trigger is described. As trigger rates are very sensitive to beam conditions (luminosity, backgrounds) and detector performance (e.g. noisy cells), the Level-1 trigger needs to be carefully monitored, which guarantees correct functioning of the Level-1 trigger system and is vital for correct and meaningful data taking.

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Session Classification: Parallel session B1

Track Classification: Triggering

Contribution ID: **81** Type: **Oral**

Recent Progress in Field Programmable Gate Arrays

Friday 16 September 2005 09:45 (25 minutes)

In step with Moore's Law, FPGAs are continuing their rapid progress. IC technology makes circuits smaller and faster, while 300 mm wafers with low defect density reduce the cost. Innovative chip structures support adaptation to conflicting user demands, and combine with flip-chip packaging to improve the electrical characteristics.
This paper describes several new or enhanced dedicated sub-circuits that improve density and performance, and often reduce power consumption.
The growing user community expects better tools, larger core libraries, and competent technical support.
FPGAs have found their way into most digital systems and increasingly also into cost-sensitive consumer applications.

Summary

Three pillars of progress:
1. Technology, 2. Architecture and Circuits, 3. Software and IP.

Technology:
90 nm CMOS technology on 300 mm wafers with ultra- low defect density. A third, intermediate gate oxide thickness reduces leakage current.
Thin oxide for the 1.2 V core logic (fast, but high leakage).
Medium oxide for configuration storage and pass transistors (slower, but much lower leakage).
Thick oxide for I/O circuits with Vcc = 2.5 to 3.3 V.

ASMBL (Application Specific Modular Block Architecture) arranges specific circuit elements in specific vertical columns. Lets chip design and software create sub-families with a different mix of logic, BlockRAMs, multiplier-accumulators, microprocessors and multi-gigabit transceivers. I/O is now distributed, good for flip-chip packaging. Each I/O pin has adjacent ground and Vcc balls for a smaller return-current inductive loop, thus reducing ground bounce and ringing.

Architecture and Circuits:
Fast, expandable 48-bit adder/accumulator with 18 x 8 multiplier input uses significantly less power. Can be concatenated for up to 48-tap FIR filtering, while maintaining 500 MHz speed. Can also be used as a fast 36-bit adder, register, or counter, and the multiplier can be used as a barrel shifter.

Dual-ported BlockRAM expandable to 512 x 72 bits with Hamming error correction. Built-in FIFO controller can be clocked at up to 500 MHz from independent write and read clocks. Asynchronous arbitration for FULL and EMPTY and programmable "dipstick". Optional fall-through mode for first data entry.

ChipSync Input/Outputs:
Today's high-speed I/O must use clock-forwarding or Source Synchronous clocking, routing the clock together with the data. Operates up to 1 Gbps, but requires that clock and data be properly aligned at the receiver. The ChipSync structure, available on every Virtex-4 pin, provides a programmable delay with stable 75 ps granularity, intended to align the clock exactly with the data eye opening.

ChipSync on each pin also acts as serial-to-parallel and parallel-to-serial data converter and appropriate clock divider It supports word alignment through its Bitslip feature.
ChipSync can also be used to measure incoming pulses with 75 ps precision.

Multi-Gigabit Transceivers:
Serial data-communication demands speeds of up to 11 Gbps. The Virtex-4 MGTs convert between 32/40 bit parallel data @ up to 300 MHz and serial I/O @ up to 11 Gigabits/sec. Self-contained transceiver blocks have programmable FIFOs, 64B/66B code converters, output pre-emphasis and input equalization, able to communicate directly over 40 inches of pc-board backplanes.

Microprocessor and Ethernet Controller
One or several industry-standard PowerPCs are integrated into the FPGA fabric, can use their instruction and data caches for ultra-compact controller applications, or use BlockRAm or external RAM.

Software and Intellectual Property:
200,000 users demand capable, efficient and user-friendly tools for synthesis, placement and routing, and for design simulation and debugging. They also expect extensive libraries and validated cores to choose from, as well as competent and timely support by hotline engineers, by field applications engineers and in user newsgroups.

FPGAs have come a long way, and now provide vital subsystem solutions in most digital systems, even in cost-sensitive high-volume applications.

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Session Classification: Plenary session P8

Contribution ID: **82** Type: **Oral**

Production Testing and Quality Assurance of the CMS Preshower Front-end Chips - PACE3

Tuesday 13 September 2005 16:50 (25 minutes)

PACE3 is the 32-channel large dynamic range front-end amplifier, shaper and analogue memory for the CMS Preshower detector. Around 4300 PACE3, designed in 0.25micron CMOS, are required for the detector. Production of the chips has been completed and the packaged chips (fpBGA) evaluated using a custom testbench equipped with a ZIF socket under LabVIEW control. The tests are described and results presented on overall yield, digital functionality and analogue performance. Comparisons are made between chips and between wafers, as well as performance variations as a function of die position on the wafers.

Summary

The CMS silicon Preshower is a fine grain detector placed in front of the endcap Electromagnetic calorimeter. Its primary function is to detect photons with good spatial resolution in order to perform π0 rejection. The detector comprises around 4300 silicon sensors, each measuring 6.3cm x 6.3cm divided into 32 strips, with strip capacitance in the region of 50 pF. Each sensor is attached to a single PACE3 front-end chip, which performs amplification and shaping of the signals from the silicon, followed by voltage sampling into an on-chip analogue pipeline memory 192 cells deep.

PACE3 is composed of two separate ASICs called Delta and PACE-AM. Delta performs the amplification and shaping and can operate in two gain modes: high gain (HG) for calibration with single minimum ionizing particles (MIPs: 1 MIP=3.6fC) and low gain (LG) for normal physics running where a high dynamic range is required (1-400 MIPs). PACE-AM is the analogue memory, FIFO and output multiplexer etc. and includes a large amount of digital logic. Upon reception of a trigger signal, three memory locations (containing the sampled analogue signals from the sensors) are blocked and their addresses written to a FIFO. The data readout is asynchronous with the trigger. Up to 16 triggers can be stored in the memory without overflowing the FIFO.
Both ASICs are packaged in single 196-pin 1mm-pitch fpBGA. Each chip incorporates a number of registers and DACs, programmable via i2c. These include registers that hold unique laser-blown identifiers (IDs) for every ASIC. The IDs contain information on production lot, wafer number, reticle position and chip position within the reticle.
Fast timing/trigger signals are supplied via LVDS.

The packaged chips are tested using a custom testbench equipped with a ZIF socket under LabVIEW control. A large number of digital tests are performed, including scan chains, tests of all bits in all registers, the skipping mechanism, the blocking and unblocking of memory locations etc.
The response of the PACE3 to reset signals is tested, along with measurements of power consumption in “sleep”and “run”modes.
A programmable amplitude internal injection signal is provided and used to test each readout channel (and measure channel-to-channel variations). This injection signal also allows the measurement of dynamic range, signal-to-noise and, coupled with a

programmable delay circuit (provided on the testbench), the timing characteristics. The PACE3 programmable latency facilitated the measurement of memory uniformity. The absolute analogue performance of the PACE3, in terms of noise, timing and dynamic range, depends significantly on the Delta input capacitance –i.e. the presence or not of the silicon sensor. For these tests no sensor was present, so a qualitative analysis only could be performed (The good chips are subsequently mounted on PCBs and bonded to sensors. At this stage a quantitative analysis of the analogue performance is made), but this was sufficient to be able to find pathologically bad chips.

The main components of the testbench were an FPGA –to provide LHC-like fast timing and control signals, and a microcontroller –for slow control via i2c and data readout through an on-board 12-bit 40 MHz ADC. The testbench was connected via RS232 to a commercial PC running dedicated LabVIEW software. The chip IDs are used to create data directories that store the results of each test. These files, about 300kbytes per PACE3, are subsequently sent to the CMS ECAL Construction Database – CRISTAL. In addition, summary files are also produced by the software and stored in CRISTAL. The complete set of tests takes around 3 minutes per PACE3.

Many thousands of chips have now been evaluated, from an initial engineering run (2 wafers, providing ˜600 chips) and a subsequent production run (48 wafers). The yield has been measured to be better than 80%. A majority of the failures are due to short-circuits that result in no possible communication to the chip. This was easily (and quickly) identified due to out-of-spec power-on consumption. A few percent of chips exhibited problems with the digital functionality; for those passing only a tiny fraction exhibited out-of-spec analogue performance. Indeed the analogue performance is extremely uniform between chips and wafers.

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Session Classification: Parallel session A3

Contribution ID: **83** Type: **Oral**

Configuration of the ATLAS trigger

Tuesday 13 September 2005 11:25 (25 minutes)

The ATLAS detector at CERN's LHC will be exposed to proton-proton collisions at a rate of 40 MHz. In order to reduce the data rate, only potentially interesting events are selected by a three-level trigger system. Its first level is implemented in electronics and firmware, and aims at reducing the data output rate to about 75 kHz. The second and third trigger levels are based on software and reduces the rate to about 200 Hz.

To prepare the full trigger chain for the online event selection according to a certain strategy, a system is being set up that provides the corresponding information to all parts of the trigger chain, e.g. values for hardware registers in level-1 or steering parameters of high-level trigger algorithms. The same information is used to configure the offline trigger simulation. In this presentation an overview of the system is given and its main components are discussed.

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Session Classification: Parallel session B1

Contribution ID: **84** Type: **Oral**

System Tests of the ATLAS Pixel Detector

Thursday 15 September 2005 11:00 (25 minutes)

The innermost part of the ATLAS (A Toroidal LHC ApparatuS) experiment at the LHC (Large Hadron Collider) will be a pixel detector, which is presently under construction. Once installed into the experimental area, access will be extremely limited. To ensure that the integrated detector assembly operates as expected, a fraction of the detector which includes the power supplies and monitoring system, the optical readout, and the pixel modules themselves, has been assembled and operated in a laboratory setting for what we refer to as system tests. Results from these tests will be presented.

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Session Classification: Parallel session A4

Contribution ID: **85** Type: **Oral**

Performance characteristics of COTS 10Gb/s Optical Links for SLHC Experiments

Tuesday 13 September 2005 17:15 (25 minutes)

We report on the evaluation of Commercial Off-The-Shelf (COTS) optical transceivers for use in future readout and control systems of upgraded detectors for SLHC. The critical performance metrics and operational constraints on the required inputs – notably the reference clocks –will be described. Measurements of these performance metrics on samples of COTS small form-factor XFP transceivers operating at line-rates of 10Gb/s will be reported.

Summary

The detector systems currently being produced and installed in the LHC experiments all rely heavily on the optical transmission of both readout and control data. Data rates for transmission between the counting rooms and the detectors currently reach up to 1.6Gb/s for radiation-tolerant data links. The upgrading of the LHC luminosity at Super LHC (SLHC) will lead to an increase of the particle interaction rate and thus to an increase in the amount of data to be transmitted by the detector readout systems. It is thus pertinent to assess the possibilities of increasing the data transmission speeds available on individual optical data channels. With the target of reading-out an upgraded Tracker of the CMS detector at SLHC, we have begun evaluation of commercial data transmission components operating at the emerging 10Gb/s data transmission protocols such as 10Gigabit Ethernet (10GbE).
Standardization within the telecom and datacom industry has led to a Multi-Source Agreement (MSA) for a small formfactor transceiver of type XFP. The XFP MSA Group has created a specification for a module, cage hardware, and IC interfaces for a 10 Gb/s hot-pluggable module converting serial electrical signals to serial optical signals.
The specification aims to be protocol-agnostic, operating over a range of bit-rates (9.95 –11.1 Gb/s). This range would allow the matching of rates derived from a 40MHz or 80MHz bunch-crossing frequency at SLHC.
The measurement protocols, including eye-diagram measurements, required to assess the performance of such highspeed data links will be outlined. These will be decomposed into measurements pertaining primarily to the system, the transmitter and the receiver parts. Data will be shown for COTS XFP samples. Finally, the requirements for operation will be outlined and compared to the typical environment found in currently implemented optical data transmission systems in HEP.

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Presenter: Dr TROSKA, Jan (CERN)

Session Classification: Parallel session B3

Contribution ID: **86** Type: **Oral**

The Front-End Electronics System for the CMS Electromagnetic Calorimeter

Thursday 15 September 2005 14:00 (25 minutes)

CMS designed an high precision electromagnetic calorimeter, to be operated reliably in the high radiation environment of the CERN Large Hadron Collider (LHC), inside the 4 T magnetic field. Innovative solutions were developed to place the front-end electronics within the detector with the advantage of minimizing external noise, while reducing the number of optical links to send data to the off-detector readout. The final system architecture will be reviewed in detail.High resolution, over the wide energy dynamic range, was obtained with studies in an electron test beam.

Summary

The general purpose Compact Muon Solenoid (CMS) experiment is now well into the construction of its very high performance, homogeneous electromagnetic calorimeter (ECAL), made of about 76000 lead tungstate scintillating crystals(36 super-modules of the barrel and eight quadrants of the endcaps).
The low light yield (˜ 50 photons/MeV) requires photodetectors with internal gains, while the strong temperature dependence both of the crystal response and of the photodetectors (1/LY dLY/dt ˜ -5%/C), imposes to control and stabilize the detector temperature with high precision (< 0.1 C).To achieve the best energy resolution measuring electrons and photons, over a wide energy range (˜100 MeV to ˜1.5 TeV), the contributions by fluctuations of shower development, by instrumental and calibration limits must be minimized. To cut down external noise, much of the readout electronics has been mounted within the detector, with severe constraints on radiation hardness, high speed (40 MHz), wide dynamic range (90dB). The system architecture of the readout electronics was revised and heavily changed during the past two years. The trigger primitive generation, the digital pipeline, and the primary event buffers are implemented in the front-end, reducing by an order of magnitude the number of optical data links to carry data off the detector. Full custom-integrated circuits were developed in 0.25 um CMOS technology, intrinsecally radiation hard, using a single 2.5 V supply and a low power consumption (< 3 W/channel). A Multi-Gain PreAmplifier (MGPA - 3 gains 1:6:12) amplifies each photodetector signal as the input of a 12 bit multi-channel ADC.
The output of the ADC corresponding to the highest unsaturated gain, together with the information of the amplifier gain, is stored in a pipeline before the Level 1 accept signal allows it to be read from the DAQ. The basic element of the on-detector architecture is the 5x5 crystals Trigger Tower, where 25 channels are read, amplified, digitized and stored into the pipeline of the FENIX (Front-End New Intermediate data eXtractor)ASIC chips. A Mother Board distributes HV to the photodetectors, and LV from the LVRB (Low Voltage Regulator Board) to the five VFE (Very Front-End) boards. Each VFE, containing five MGPA and five ADCs, receives the signals from a row of five crystals to be shaped and digitized, while reading

photodetectors'leakage currents and crystal temperature using a Detector Control Unit (DCU). A FE (Front-End) board with seven FENIX chips stores and processes the digitized data during the Level 1 trigger latency of 3 us. Both trigger data and digitized data from the triggered event are transmitted to the off-detector electronics, the so called Upper Level Readout (ULR), through serial digital 800 Mb/s data links.A well developed clock and control link transmits the Level 1 trigger decision as well as slow control for configuration. A full barrel supermodule with the final on-detector electronics has been tested on an electron beam to measure the front-end electronics performance.

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Session Classification: Parallel session A5

Contribution ID: **88** Type: **Oral**

Study of serial powering of ATLAS silicon strip sensors

Thursday 15 September 2005 12:40 (25 minutes)

Serial powering of silicon detectors can dramatically reduce the number of power cables. This will relax space constraints, reduce material, and minimize power losses in cables. A study of the power efficiency of a serial powering scheme for silicon strip detector modules is performed. Numerical results are presented as a function of the number of modules, supply voltage, and cable resistance. Serial powering results in a significantly higher power efficiency than a conventional parallel powering scheme for typical particle physics applications. First tests with four ATLAS SCT silicon strip modules powered in series show encouraging results.

Summary

The readout electroncs of silicon detector modules are conventionally powered in parallel, with a separate analog and digital power line and supply for each module. This scheme offers the advantage of an independent voltage control over each module and minimizes conductive interference between modules. The price to pay is the large number of power cables, an increase of material in or near the tracking volume, and the increased heat load through power losses in the cables.

An alternative approach –serial powering of modules from a single current source, was proposed for application in the ATLAS pixel detector and prototyped with encouraging results [1]. Serial powering of silicon detectors can dramatically reduce the number of power cables in typical particle physics experiments. This is particularly relevant in the context of a future SuperLHC silicon detector, which will likely have five to ten times more channels than the current LHC detectors. In addition to reducing the number of cables, serial powering can also lead to higher power efficiency, defined as the ratio of power consumed by the readout electronics to the total power delivered.

A study of the power efficiency of a serial powering scheme for silicon strip detector modules was performed. Numerical results as a function of the number of modules, supply voltage, and cable resistance are presented. It is shown that serial powering results in a significantly higher power efficiency than a conventional parallel powering scheme.

Tests with four ATLAS SCT silicon strip modules powered in series have been performed using commercial voltage regulators and AC-coupled LVDS drivers. While we follow the concept developed in [1], the hardware is different, most notably the readout chip and the preamplifier input capacitance. The test results indicating encouraging module performance are presented.

Two critical issues for the success of serial powering are the possibility of increased noise through interference effects, and the danger of losing a chain of serially connected modules in case of a single failure. Redundancy schemes and chip specification issues related to serial powering will be discussed.

References:

[1] T. Stockmanns, P. Fischer, F. Hügging, I. Peric, Ö. Runolfsson, N. Wermes,
Nucl. Instr. and Meth. A 511, 174-179 (2003).

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Session Classification: Parallel session A4

Contribution ID: **89** Type: **Oral**

Radiation Tolerant Source Interface Unit for the ALICE Experiment

Tuesday 13 September 2005 14:15 (25 minutes)

The ALICE Detector Data Link (DDL) is a high-speed optical link designed to interface the readout electronics of ALICE sub-detectors to the DAQ computers. The Source Interface Unit (SIU) of the DDL will operate in radiation environment. Tests showed that configuration loss of the ALTERA APEX II FPGA device used earlier on the DDL SIU card is only marginally acceptable. We developed a new version of the SIU card using ACTEL ProASIC+ device based on flash memory technology. The new SIU card has been extensively tested using neutron and proton irradiation. In this paper we present the SIU card and describe the results of irradiation measurements.

Summary

The ALICE Detector Data Link (DDL) is a high-speed, duplex, point-to-point optical link designed to interface the readout electronics of all the ALICE detectors to the DAQ computers in a standard way. The DDL consists of the Source Interface Unit (SIU), an optical cable up to 300 meters, and the Destination Interface Unit (DIU). The DDL provides enough bandwidth to transfer data from the detectors at 200 MB/s. The SIU will be attached to the Front-end Electronics, hence it will be exposed to the radiation caused by the interacting particles. According to the latest simulations, the highest radiation level for the SIU card is expected at the inner radius of the TPC detector, where the total ionizing dose is 1.3 krad and the 1 MeV equivalent neutron fluence is 1.47 × 10ˆ11 neutrons/cm2 for 10 years of operation. The hardware consists of three main, and several auxiliary components. The full-duplex optical transceiver makes the conversion between the optical serial data and the high-speed differential electrical data. The electrical transceiver performs data conversion serial-to-parallel and parallel-to-serial. The DDL protocol and additional logic functions are implemented in a programmable logic device (FPGA). The components of the SIU card have been extensively tested. The results show that the TID effects have little impact on the components used. The single event effects (SEE), however, can provoke two different types of error. High-energy particles may change the content of the registers or the user memory therefore increases the single-bit-error rate. According to the measurements, this error rate increase is negligible compared to the bit-error rate always present during optical transmission. In addition, the particles may as well alter the content of the configuration memory cells of the SRAM-based FPGA device used on the prototype cards. This type of error may cause functional interrupt at a rate, which is only marginally acceptable.
We developed a new version of the SIU card using alternative logic device, namely the ACTEL ProASIC+ device family based on flash memory technology. We carried out two series of tests to investigate the configuration loss in radiations environment. The first series of measurements was carried out in TSL, (Uppsala, Sweden) using protons at energy of 150 MeV and 180 MeV. The 2nd series of

measurements was done at ATOMKI (Debrecen, Hungary) using thick target p+Be neutrons with spectrum extending up to En=14 MeV. The methods and results of the measurements are shown in this paper.

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Session Classification: Parallel session B2

Contribution ID: **90** Type: **Poster**

Services for the read-out of the ATLAS TRT

The read-out of the ATLAS TRT requires about 30000 digital links working at 40 Mbits/s. For cost reasons it
was not possible to use fibre optics technology in the tracker volume of ATLAS. LVDS links using very thin
twisted pair lins (36 AWG) have been implemented up to a point where a small number of optical Gbits links
are used.
Complex harnesses, including the small twisted pairs, the low and high voltage cables have been designed
and are currently being fabricated.
The paper will focus on the difficulties encountered to run high speed links on very thin cables and show how
they were specified and validated. Then the production process and its status will be presented.

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Contribution ID: **91** Type: **Poster**

B-field monitoring of the Alice magnetic fields,

In view of the forthcoming magnetic field measurements (July-September 2005) of the Alice magnet system, a prototype for monitoring the magnetic field was build and tested in the laboratory and will be validated during the mapping of the magnetic fields. The total magnetic field volume to be measured comprises the L3 solenoid and
Muon arm dipole magnets. Hall and NMR probes will be installed in both magnets and connected to a central monitoring system. The present paper describes the prototype front-end configuration together with its PVSS control software and first results.

Summary

A series of measurements are planned in the near future, with the purpose of mapping
the magnetic fields of the ALICE magnets. The magnetic field measurement volume comprises the volume of the L3 solenoid magnet together with the volume of the muon arm dipole magnet. Measurements will be performed for two settings of the magnetic field, i.e. 0.2 and 0.5 Tesla, in the L3 solenoid, a fixed setting in the dipole magnet and both polarities for the two magnets. Hall and NMR probes will be use for monitoring. The present paper is describing the prototype build for these tests.
The "Hall probes"–56.5*56.5 cm2 sensor cards produced by NIKEFH for the ATLAS experiment- are connected via flat cables to a MTD-DCS CAN module designed to support read-out of multiple B field sensors. The MDT - DCS is a CANOpen driven module and contains an ELMB board. The MTD-DCS module is connected via CANbus cable to a KVASER PCI CAN card installed in a PC. For the present prototype, PVSS II v3.1 control software was written and implemented. The control application communicates with the MTD-DCS hardware via the ELMB OPC server (an ATLAS software product, based on the CANOpen protocol 2.0). The paper will describe the hardware and software setup in detail together with results and measurements.

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Presenter: Dr POPESCU, Sorina (IFIN-HH/CERN)

Contribution ID: **92** Type: **Oral**

The Readout, Fast Control and Powering Architecture for the CMS Preshower

Thursday 15 September 2005 15:15 (25 minutes)

The CMS Preshower detector (ES) comprises ondetector and offdetector components of the readout and control system, as well as the powering system and optical links. The fast control system is largely built around the one originally conceived for the CMS Tracker (FEC, DOH, CCU etc.) whilst the readout part profits from developments made for the CMS ECAL (DCC, GOH, AD41240). There are two ESspecific ASICs: PACE3 (frontend preamp/ shaper/analogue memory) and Kchip (data concentrator). Two custom ondetector PCBs have also been developed: the frontend hybrid (containing the PACE) and the system motherboard (containing all power regulators, digital chips, optical components and ADCs). The full architecture is presented, along with results from system tests.

Summary

The CMS silicon Preshower is a fine grain detector placed in front of the endcap Electromagnetic calorimeter. Its primary function is to detect photons with good spatial resolution in order to perform pi0 rejection. The detector comprises around 4300 silicon sensors, each measuring 6.3cm x 6.3cm divided into 32 strips, with strip
capacitance in the region of 50 pF. Each sensor is attached to a single PACE3 frontend ASIC, which performs amplification and shaping of the signals from the silicon, followed by voltage sampling into an onchip analogue pipeline memory 192 cells deep. Upon reception of a first level trigger the analogue signals are multiplexed out of the PACE3 to a 12bit 40MHz ADC (AD41240). The Kchip ASIC then takes the digitized data from up to 4 PACE3, reformats the data and transmits them to
the offdetector readout boards (ESDCC) via Gigabit Optical Hybrids (GOH). The PACE3 is situated on a PCB bonded to a silicon sensor mounted on a ceramic support and an aluminium tile (to allow overlapping in one direction of adjacent sensors) to form a micromodule . This PCB also contains a DCU chip for calibration of the PACE3, and connects to the System MotherBoard (SMB) via an embedded polyimide cable. Four types of SMB are used, connecting to 7, 8 or 10 PACE3. The SMBs contain the ADCs, Kchips and GOH boards, as well as a set of control chips the CCU, LVDSmux4P, PLL, QPLL, DCU, LVDSbuf used for setup of the ASICs and distribution of the fast timing signals (clock, trigger). Up to 12 SMBs are connected together via polyimide cables to form control rings . Each ring communicates with the offdetector VME modules (Clock and Control System CCS) via Digital Optical Hybrids (DOH) placed on two adjacent SMBs (for redundancy purposes). The low voltage is supplied to the system by CAEN Easy3000
series modules through voltage regulators situated on the SMBs. Each SMB contains a control regulator (CR) for supplying the control chips, and a group of readout regulators (RR) for the PACE3, ADCs, DCUs, Kchips and GOHs. The CAEN system can

control the CRs and groups of RRs to allow the switching on/off of relatively small units within the ES whilst still maintaining the integrity of the control rings whenever possible. The micromodules are connected to the large ES lead absorber plates. The possibilities of commonmode pickup by these plates, as well as the possibilities of return current flow through them, have necessitated a precise grounding and shielding scheme. With exception of the ESDCC, which is still in the development phase, all components of the ES electronics system have been prototyped and most are in full production. System tests have been performed with excellent results in terms of functionality and performance.

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Session Classification: Parallel session A5

Contribution ID: **94** Type: **Poster**

Test Station for the CARIOCA FE-chip of the LHCb Muon Detector

This document describes the hardware and software of a Front-End Electronics Test (FEET) Station developed to test and characterize the LHCb Muon Front-End (FE) ASIC, which processes the signals generated by Multi-wire proportional chambers and GEM detectors. The CARIOCA (Cern And Rio Current-mode amplifier) is an 8-channel Amplifier, Shaper and Discriminator with Base Line Restoration (ASDB). It has entered production phase during the current year. A total of approximately 20000 chips will be produced and they will require individual testing, before final assembly on Printed Circuit Boards (PCB). The ASIC design is fully customized for the LHCb muon chambers and, besides, it is almost entirely analog, what raises difficulties to the adoption of commercial test systems. CBPF has proposed and eveloped a test bench
with the following features: variable and bipolar charge injection, custom read-out, rate and time measuring circuitry, power consumption control and a LabVIEW management program. This system detects open or dead channels as well as short circuits, and measures noise, sensitivity, and the time width of the LVDS output signal. Results for the first thousand chips measured are also shown.

Summary

The LHCb Muon Group has developed the CMOS ASIC CARIOCA to readout its Multiwire Proportional Chambers (MWPC) and GEM detectors, using the radiation hard IBM 0.25um process. Each ASIC holds 8 identical current-mode ASDB channels with individual input thresholds. The Muon detector contains around 120000 physical channels, requiring production of 20000 front-end chips, roughly. CARIOCA has been developed to process MWPC cathode and anode signals (positive and negative charges) and two different versions have been implemented to overcome the requirement of MWPC and GEM detectors operation. The test station has been devised to accomplish bipolar tests and to measure characteristics of both CARIOCA versions. All tests should be carried out before chips are soldered to PCBs in order to minimize potential over-costs related to loss of time and rework activities if a significant proportion of FE boards is found to be defective. Each PCB will have on board two CARIOCAs and another (digital)ASIC developed to receive the 16 channels generated by the two amplifiers.

The current test station permits users to perform measurements, run diagnostics, to acquire statistical data of all important ASDB parameters using several techniques, which will be shown in depth. Various algorithms have been implemented to achieve a systematic test procedure for the detector read-out apparatus. The parameters under test are: power consumption, channel response, offset, sensitivity, time-walk and pulse width.

The main building blocks of FEET are a charge injector, a read-out and counting device, a Time to Digital Converter (TDC) custom circuit, a National Instruments data acquisition (NI-DAQ) PCI board and an integrated LabVIEW program. The Injection Board (IB) contains 8 channels and its circuitry permits a fine tuning of injected charge (in the range of few fC) and of ASD threshold values, it can also mask out any chosen group of channels, control the injection rate and finally

inject either positive or negative charge as required. A Counting Board receives differential signals from the ASIC under test and processes data by means of 8 individual counters (all synchronized to IB signals); it transfers data to a local computer via the NI-DAQ board and its functionalities are based mainly on a Xilinx FPGA implementation. The custom TDC module uses a commercial IC to digitalize the time of the CARIOCA input and ouput pulse transitions, allowing the measurement of the CARIOCA response time and output pulse width with a resolution as low as 120ps; data transfer is carried out via parallel port EPP standard.

This testing station, with its development approaching completion, has suggested and put into evidence parameters to be looked into with more accuracy, and served also to establish procedures for a practical implementation of an easy to use bench station.
Tests of chips from the non recursive engineering run are under way, and will provide the parameters for rejection of the chips from the production run.
Circuitry, algorithms and statistics results will be presented.

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Contribution ID: **96** Type: **Poster**

Multiplexed Channel Readout in a cosmic rays test station

LHCb Muon Chambers (MWPC) testing will be carried out in a number of steps, and final characterization will be performed in a station detecting cosmic rays, with all the equipment in place. We have designed a Multiplexer board, which can reduce by more than a factor of four the number of channels to be acquired, using time multiplexing: signals are delayed with respect to each other by a fixed amount, via cascaded delay cells within an FPGA. A fully functional readout system can be put together using Multiplexers, capable of reading up to 576 channels utilizing only one 128-channel multi-hit TDC module.

Summary

The LHCb muon detector is approaching the installation phase of all its subsystems and adequate test coverage of all parts and units is a key requirement. A testing station based on cosmic rays can prove to be an invaluable tool to point out performance issues and to perform a highly accurate quality control of chambers tested. It allows control of operation of elements like Front-End Boards and the Experiment Control System, evaluating efficiency and time resolution of fully assembled units.
We designed an apparatus in order to receive data from, and to control in parallel six chambers, all fitted with Front-End Boards and generating a total of 576 channels to be read with a 128-channel multi-hit TDC. In order to perform track reconstruction for muons crossing the 6 chambers, all signals must be read at the same time, calling for time multiplexing in order to reduce the number of lines. Applying selected multiple amounts of delay to channels, joining and sending them to a multi-hit TDC module, is how time multiplexing is carried out.
A fundamental parameter in the LHCb muon detector is time resolution: MWPCs have been designed in such a way as to maintain detection efficiency higher than 99% within the 25ns LHC bunch crossing period, with a time resolution of the order of 3ns. For this reason delay granularity has been set to a value of 100ns, thus avoiding overlaps of data belonging to different events. Jitter caused by the delay lines can worsen time resolution of measurements: the total value of all contributions should remain below 1ns. Jitter evaluation on devices showed a total contribution of about 800ps to the total figure. Results of measurements will also be included.
Multiplexers are 6U 12HP modules, with four programmable logic devices (Xilinx Spartan IIe XCV300) on board, and are based on an 8-layer printed circuit. On-board FPGAs are capable of applying selected delays to channels via a custom designed macrocell, which is replicated inside the device. Disabling selected channels is a beneficial feature in case of noise or faults, and it is made possible by an I2C interface implemented on each FPGA. Each Multiplexer is capable of receiving 128 logical channels and of merging them into 32, before their final transmission to a multi-hit TDC.
The testing station uses four Multiplexers, each receiving signals from chambers

fully instrumented with Front-End cards (called CARDIAC); its trigger system is based on two layers of scintillators with a contribution to total jitter of 2ns.
Such an apparatus has been assembled and is currently utilized as a last stage in performance evaluation. Fully instrumented chambers in groups of six are tested with no significant deterioration of time resolution and the system can function as a fully operational readout system for a maximum of 576 channels in spite of its small scale and low cost.

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Contribution ID: **97** Type: **Oral**

A radiation-tolerant LDO voltage regulator for HEP applications

Tuesday 13 September 2005 15:05 (25 minutes)

We have developed a radiation-tolerant Low Drop-Out (LDO) voltage regulator for applications in High Energy Physics experiments. The regulator outputs a fixed voltage of 2.5V, it provides a maximum current of 300mA with a drop-out as low as 150mV. The circuit incorporates over-current, over-voltage and over-temperature protection, and it can be disabled via a dedicated input pin. Manufactured in a commercial quarter-micron CMOS technology, it is available in a very compact 4.9x6x1.6mm 16L-EPP-SSOP package.

Summary

The distribution of power in the LHC experiments represents a real engineering challenge, given the global requirements in terms of power needs, available cooling capacity and limited material budget. The picture is complicated further by the radiation environment, which dictates that all electronics installed inside the experiments need to be radiation tolerant, and by the intense magnetic field that forbids the use of switched converters in many locations.
One solution that is often used is the distribution of low-voltage from supplies located in areas safe from radiation hazards via cables that can be up to 100m long.
This implies large currents to flow in the cables, determining sometimes large voltage drops across the cables. To regulate the voltage locally, linear regulators are used in proximity of the electronics circuits to be powered. These regulators dissipate power into heat that has to be evacuated by the cooling system, therefore it is mandatory to reduce their power dissipation as much as possible (increasing their efficiency). In this respect, relatively low-current regulators can be more effective than circuits that can provide larger currents because they can operate at much lower drop-out voltages, which effectively increases their efficiency. Such linear LDO regulators, capable of drop-out voltages of 100-200mV, are very common in the marketplace, but no radiation-hard component with these characteristics can be found at affordable cost.
With this in mind, we have started in 2004 the development of a radiation-tolerant LDO regulator using the same commercial quarter micron CMOS technology used by a large fraction of the ASICs for the LHC experiments. Aimed at regulating the voltage required by these circuits, it can provide in its first version a fixed output voltage of 2.5V (and a variable version will be easily derived). The circuit can supply currents between 0 and 300mA, with a drop-out voltage of 150mA for the maximum load. Designed with radiation-tolerant layout approach (Enclosed Layout Transistors and guardrings), it has been developed to stand total dose levels of several Mrad.
The regulator is protected against over-voltage, over-current and over-temperature events by automatic detection mechanisms. It can operate safely with input voltages

up to 3.5V, after which the regulator is automatically disabled. In case of over-temperature, the circuit is disabled as well, whilst in case of over-current the output voltage drops while the current is limited to a pre-defined maximum value.
The regulator can be disabled via a dedicated input pin in case of need.
Due to its limited current capability and its low drop-out voltage, hence low power dissipation, it can be packaged in a very compact 4.9x6x1.6mm 16L-EPP-SSOP package, which can easily be integrated in close proximity to the circuit(s) it has to power.
For stability, it requires small surface-mount capacitors in the 3-6□F range.
A prototype version of the regulator has been produced, packaged and received for testing in April. The first measurements indicate that the circuit meets the specifications in terms of line and load regulation, and the full characterization, including radiation tests, is now starting.

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Presenter: Dr FACCIO, Federico (CERN)

Session Classification: Parallel session A2

Track Classification: Power Management and Conversion

Contribution ID: **98** Type: **Oral**

A Tracking Detector for Triggering at SLHC

Friday 16 September 2005 11:30 (25 minutes)

We report on preliminary design studies of a pixel detector for CMS at the Super-LHC. The goal of these studies was to investigate the possibility of designing an inner tracker pixel detector whose data could be used for selecting events at the First Level Trigger. The detector considered consists of two layers of 50x50 □m2 pixels at very close radial proximity from each other so that coincidences of hits between the two layers amount to a track transverse momentum cut. This cut reduces the large amount of low momentum data expected at SLHC whilst it keeps the tracking efficiency very high for high transverse momentum tracks

Summary

Currently groups of researchers are actively discussing possible scenarios of upgrades of the LHC machine. According to the most financially realistic scenario the LHC will be upgraded to provide proton beams of an order of magnitude larger intensity (1035 cm-2 sec-1) colliding at twice the frequency (80 MHz) of the present design but have the same centre of mass energy. This machine design is commonly referred as the Super LHC and it is expected to be operational after 2015.
A consequence of this design is that the backgrounds due to minimum bias events will increase by at least a factor of 5. This imposes severe requirements on the CMS detector.

The occupancy of a tracking detector at SLHC has been calculated using a Monte Carlo. As an example a pixel detector of 1.28cm□1.28cm with 256□256 pixels 50□50□m2 each positioned at radius of 10 cm away from the beam will suffer from a background of 4 hits/12.5nsec dominated by low momentum particles. This is clearly an enormous rate of data to be transported out of the detector and be used for the trigger decision. Hence, there is an urgent need for a tracking detector that has the capability to reject the large amount of low momentum background locally.

A two layer pixel detector has been simulated using PYTHIA. The radial separation is of the order of 1-2 mm. The two layers can communicate with each other electronically and several algorithms have been explored which put the hits from the two layers in coincidence using fixed search windows. The effect of the layer reparation versus data reduction and window size has been extensively studied. It has been demonstrated that the data can be reduced by several orders of magnitude without and lose of tracking efficiency for high transverse energy tracks.

Authors: Mr FOUNTAS, Costas (Imperial College); Mr JONES, John (Imperial College London)

Presenter: Mr JONES, John (Imperial College London)

Session Classification: Plenary session P9

Contribution ID: **99** Type: **Poster**

A Tracking Trigger for CMS at SLHC

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Investigations on the possibility of designing a First Level Tracking Trigger for CMS at the SLHC based on the data of the inner tracking detector are presented. As a model for the inner tracking detector we have used the current CMS pixel detector with the same pixel size and radial distance from the beam. Extensive simulation studies have been performed using the full CMS simulation package (ORCA/OSCAR). Using these MC samples an electron trigger has been designed which uses both the calorimeter energy depositions and the pixel detector data. Results on the tracker occupancy and the electron trigger performance are presented.

Summary

It is foreseen that the LHC will be upgraded to provide proton beams of an order of magnitude larger intensity (1035 cm-2 sec-1) colliding at twice the frequency (80 MHz) of the present design but having the same centre of mass energy. This machine design is commonly referred as the Super-LHC and it is expected to be operational after 2015. A consequence of this design is that the backgrounds due to minimum bias events will increase by at least a factor of 5. This imposes severe requirements on the CMS detector. One of the most challenging tasks for SLHC will be the inclusion of the inner tracker data in the First Level Trigger, the so called First Level Tracking Trigger. Based on the HLT studies published in the CMS DAQ TDR, a tracking trigger system is needed that provides every 12.5 nsec: (1)Track-stubs and preliminary vertices from the vertex detector data. (2)Track-stubs based on the outer tracker data.

The Trigger considered in these studies should be free of dead-time. Hence, it has to read data every 12.5ns and use a digital pipeline to process them. To reduce the output data rate electrons, muons, taus, and jets found using the calorimeter and muon triggers are correlated with track stubs and vertices found by the tracking trigger.

Using the CMS Monte Carlo and reconstruction programs OSCAR and ORCA minimum bias events have been generated corresponding to luminosities up to 1035 cm-2 sec-1. These samples have been used to estimate the occupancy of the inner tracking detector at SLHC. The occupancy has been estimated under realistic conditions of inactive material and a 4 T magnetic field. This gives the first picture of the challenge facing a tracking trigger at SLHC.

An electron tracking trigger has also been simulated. This trigger is using the electron objects found by the Calorimeter First Level Trigger in coincidence with stubs found using the inner pixel detector. The performance of such a trigger at SLHC conditions has been studied using simulated decays of a heavy Higgs boson to four electrons.

Author: Dr FOUDAS, Costas (Imperial College)

Co-authors: ROSE, A. (Imperial College); Prof. HALL, Geoff (Imperial College); Mr JONES, John (Imperial College)

Presenter: Dr FOUDAS, Costas (Imperial College)

Contribution ID: **100** Type: **Oral**

The LHCb VELO Detector Modules

The LHCb VELO detector consists of two halves, each equipped with 21 sensor stations. Each station consists of a Carbon Fibre support and a double-sided hybrid module equipped with 32 Beetle readout chips and R and Phi measuring sensors. The modules are designed to operate in a vacuum, transfer 32 watts to the cooling system whilst maintaining the silicon at −7 degrees and provide mechanical alignment and stability at the level of 10um. The design and the development steps leading to production modules will be described.

Author: Mr SMITH, Nigel Anthony (associate)

Presenter: Mr SMITH, Nigel Anthony (associate)

Contribution ID: **101** Type: **Oral**

THE ALICE CENTRAL TRIGGER PROCESSOR SYSTEM

Tuesday 13 September 2005 12:40 (25 minutes)

The Alice Central Trigger Processor is described. The current trigger concept was introduced in 2001 and allows up to 50 trigger inputs at three different levels: level 0 (24 inputs, 1.2 μs latency); level 1 (20 inputs, 6.5 μs latency); level 2 (6 inputs, 88 μs latency). Up to 50 trigger classes (where inputs and destination detectors are specified) can be used simultaneously. Detailed designs became available in 2005.

The trigger system is implemented using seven types of 6U VME boards. Six types make up the CTP itself; the seventh, the LTU, provides the detector interface and can also be used as a trigger generator.

Summary

The ALICE Central Trigger processor and its requirements have been in development over a period of about ten years. The present trigger concept dates from 2001.

ALICE expects to take data in a number of different running configurations, using various ion-ion beams and also using pp collisions, the latter at a significantly lower luminosity than the other LHC experiments. The principal design aim for the experiment has been to choose detectors that allow the measurement of very high multiplicities (up to 8 000 tracks in the main detector), and this has led us to a set of detectors with somewhat inhomogeneous intervals for detection and readout of signals. These range from a large Time Projection Chamber (TPC), which is sensitive
for a period of 88 μs and which reads out throughout this interval, to triggering detectors (T0 and V0) sampling forward multiplicities, which are able to resolve a single bunch crossing. The ALICE trigger addresses these problems by implementing partitioning of the detector, so each partition has an independent dead time, and through the imposition of a "past-future protection"interval, related to the sensitive time of the detectors, during which only a programmable restricted number of additional collisions can take place.
The trigger handles combinations of up to 50 trigger inputs and runs up to 50 triggers in parallel; these are mediated through the trigger class, a trigger specification combining trigger inputs, trigger output detectors (the detector cluster) past-future protection requirements and certain other flags.

The Central Trigger Processor (CTP) is implemented using 6 different types of 6U VME board, together making up eleven active boards for the CTP. In addition, for each detector there is a Local Trigger Unit (LTU) which receives trigger information for the specific detector from the CTP and provides the interface to the detector, where appropriate through the RD-12 TTC system. The LTU can also be used in standalone mode as a generator of simulated trigger signals. The LTU boards for ALICE have now been produced, and the production of CTP boards will have been completed by the end of September 2005.

Authors: Dr VILLALOBOS BAILLIE, Orlando (University of Birmingham); FOR THE ALICE COLLABORATION, _ (_)

Co-authors: Mr JUSKO, Anton (University of Birmingham); Dr EVANS, David (University of Birmingham); Dr KRALIK, Ivan (Institute for Experimental Physics, Kosice); Dr URBAN, Josef (Institute for Experimental Physics, Kosice); Dr SANDOR, Ladislav (Institute for Experimental Physics, Kosice); Dr JOVANOVIC, Predrag (University of Birmingham); Dr LIETAVA, Roman (University of Birmingham); Mr FEDOR, Stanislav (Institute for Experimental Physics, Kosice)

Presenter: Dr VILLALOBOS BAILLIE, Orlando (University of Birmingham)

Session Classification: Parallel session B1

Contribution ID: **104** Type: **Oral**

Hybrid Design, Procurement and Testing for the LHCb Silicon Tracker

Wednesday 14 September 2005 10:45 (25 minutes)

The Silicon Tracker of the LHCb experiment consists of four silicon detector stations positioned along the beam line of the experiment. The detector modules of each station are constructed
from wide pitch silicon microstrip sensors. Located at the module's end, a polyimide hybrid is housing the front-end electronics. The assembly of the more than 600 hybrids is done at industry.
We will report on the design and production status of the hybrids for the LHCb Silicon Tracker and describe the quality assurance tests. Particular emphasis is laid on the vendor qualifying and its impact on our hybrid design that we experienced during the prototyping phase.

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Presenter: Prof. LEHNER, Frank (Zurich University)

Session Classification: Plenary session P4

Contribution ID: **105** Type: **Oral**

Performances of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger

Thursday 15 September 2005 15:40 (25 minutes)

The ATLAS Barrel Level-1 muon trigger handles data coming from the Resistive Plate Chamber detectors, structured in three concentric layers inside the air-core barrel toroid. The trigger classifies muons within different programmable transverse momentum thresholds, and tags the identified tracks with the corresponding bunch crossing number. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut. The Coincidence Matrix ASIC implements the trigger algorithm and the readout of the RPC detector, processing hit signals coming from up to four detector layers. It finds muon track candidates and generates the output trigger patterns within a latency of a few 25 ns bunch crossing periods, and produces and time tags the readout hit patterns. Due to the different performance needs and limitations in the technology, the CMA input pipeline and trigger logic and the time interpolator run at the working frequency of 320 MHz, the readout part works at 160 MHz while the control part works at 40 MHz. Performances of the ASIC have been studied on different test station, the test results are presented.

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Presenter: Mr VARI, Riccardo (Istituto Nazionale di Fisica Nucleare (INFN))

Session Classification: Parallel session B5

Contribution ID: **106** Type: **Oral**

State of the art design of rigid-flex substrates –A manufacturer's point of view

Wednesday 14 September 2005 09:45 (25 minutes)

GS Praezisions AG has been involved in the LHC project by providing electronic substrates for several experiments such as the CMS front-end hybrids, CMS Calorimeter, ALICE Silicon Pixel Detector MCM and others.

Based on the experience with the designs of the various groups and countries we will highlight the common mistakes, opportunities and challenges in modern PCB design.
We conclude that many design related issues can be prevented if a competent PCB manufacturer is involved at an early stage.

Using proven design rules, the cost performance, manufacturability and product reliability can be significantly influenced. The authors will detail the important design rules regarding build up, choice of materials, layout and surface protection. Advantages and limitations of manufacturing methods like plasma etching and laser drilling as well as direct laser imaging will be discussed.

This will help to avoid problems with implementing front end hybrids for the LHC experiments while pushing the limits of standard PCB design.

Summary

Large scale leading edge experiments such as the LHC, invariably push the envelope of standard electronics. The substrate or PCB is one of the most expensive single component that is designed into such electronics. Coupled with the industrial scale of production, it is inevitable that manufacturer and design team closely cooperate and analyze the risks and trade-offs of aggressive (quick and dirty) design vs. manufacturability.

Direct chip attach boards pose further unique challenges in terms of line pitch and surface preparation. When coupled with flex and rigid-flex design, the complexity increases exponentially, namely because of more processing steps, but also because of the mechanical functions of the board. Linked with harsh environmental conditions such as temperature, vacuum, radiation and vibration standard designs will not live up to the requirements.

This paper will introduce briefly current and future circuit board materials and their respective properties with respect to temperature, vacuum, humidity, radiation and high frequency behaviour. The changes in dimension and absorption of moisture of certain base materials, especially Polyimide, are to be taken into consideration during design.

We will discuss the various stack-up options for rigid, flex and rigid-flex design such as "classical", "bikini" and "book binder" and will touch on the trade-off with respect to price and function. Moreover, the properties of coverfilm and the issue of adhesive squeeze out are covered.

The proper design for mechanical requirements such as flatness, stiffness, bending radius, dynamic stress and torque will be laid out. It will be shown how typical

designs may overlook stresses during assembly. Moreover, ceramic inlays may be a useful method to combine the advantages of PCB technology with those of hybrids.

We will investigate the influence of temperature and its implication to the design of the PCB. Special attention will be given to drilling and cleaning of blind vias and plated through holes in inhomogeneous material stacks in order to prevent barrel cracking and separation from the innerlayer during temperature stress. Laser, plasma and mechanical drilling methods will be compared to each other. The various root causes of delamination during manufacture, assembly and operation will be analyzed and we will present the appropriate counter measures.
These include choice of material, matching copper weight with prepreg or adhesive thickness and proper surface preparation.

Passivation of copper surfaces is important for solderability and bondability of hybrid circuits. GS Praezisions AG will share their knowledge gained in application over a ten year period. Common problems are poor bonding yield, Ni/Au corrosion, Ni/Au cracks, probe marks on bond pads, poor wetting, and whisker building. Some of these problems can be alleviated with improved designs while other will require excellent manufacturing control.

In the advent of ever shrinking geometries, new technologies for art work imaging are inevitable. High density lines need to be combined with ever shrinking vias, posing new challenges for imaging, plating and etching. New technologies in each field including their respective limitations are shown such as stacked vias and laser direct imaging.

In conclusion, we would like to stress that an early cooperation with a competent and experienced manufacturer may push the technological envelope while not compromising on reliability and yield. Sufficient time must be allowed for design review and validation.

Author: Mr PUSCHMANN, Daniel (GS Praezisions AG)

Co-author: Dr BOSE, Frank (GS Praezisions AG)

Presenters: Mr PUSCHMANN, Daniel (GS Praezisions AG); Dr BOSE, Frank (GS Praezisions AG)

Session Classification: Plenary session P3

Contribution ID: **107** Type: **Oral**

My test

this is my abstract

Summary

this is my summary

Track Classification: Tracking

Contribution ID: **108** Type: **Poster**

Final results from the APV25 production wafer testing

The APV25 is the front end readout chip for the CMS silicon microstrip tracker. Approximately 75,000 chips are required and the production phase is now complete. Each chip on every wafer is subjected to detailed probe testing to verify full functionality and performance, and only chips that pass all tests are selected for mounting on detector modules. Over several years more than 500 wafers have been tested and results for all chips have been archived. An analysis of the database allows significant comparisons between chips, wafers and wafer production batches, giving a complete and final picture of the spread in yield and performance experienced in this large scale manufacturing task.

Summary

The APV25 is the 128 channel chip for CMS silicon tracker readout, manufactured on 200 mm wafers in 0.25 micron CMOS technology. A high yield of multi-chip hybrids for detector modules requires comprehensive testing of chips on the wafer.

Each APV channel comprises a low noise front end, a 50 ns CR-RC shaping amplifier, a 192 element deep analogue pipeline, and an analogue pulse shape processing stage (APSP). The pipeline samples the amplifier output at 40 MHz and accommodates the level one trigger latency and buffering of events awaiting readout.
The APSP implements a deconvolution operation on 3 consecutive pipeline samples to achieve single bunch crossing resolution at high luminosities. Analogue output samples are multiplexed onto a single output for subsequent optical transmission to the off-detector data acquisition system. The chip contains system features including bias and calibration pulse generation, programmed via the slow control interface. The on-chip programmable features enable a thorough wafer probe test to be performed leading to a high level of confidence in identifying defective chips.

Approximately 75,000 chips (plus spares) were required to read out approximately 10 million microstrip channels. Wafers were delivered in production lots of up to 25 wafers, each wafer containing 360 viable APV sites. We have previously reported [1,2] on progress and problems encountered during the several years over which this production task has been spread. Because of wafer yield and hybrid production losses we have probe-tested more than 500 wafers (180,000 chips) to obtain sufficient numbers of APVs to complete the tracker construction.

The on-wafer chip tests included detailed verification of both digital and analogue functionality. Digital tests included verification of the slow control interface, and correct operation of the pipeline control logic, and any defect here resulted in rejection. Analogue tests included pedestals, pulse-shape, gain and noise measurements, pipeline uniformity, individual pipeline element storage capability, and power consumption. Performance was verified in all operational modes for all channels. Analogue acceptance thresholds were defined to ensure satisfactory performance for the application. A test time/chip close to one minute, allowed a throughput of 2 wafers/day. All the wafers were tested on a single semi-automatic probe-station.

During testing all chips were identified by wafer name and location on the wafer, maps being produced for subsequent dicing and picking by the hybrid manufacturer.

The test results were stored in a database, allowing us to perform detailed analyses comparing performance between chips, wafers and production batches. The results of these analyses provide insight into the stability of performance achievable from a large-scale manufacturing task extended over several years.

[1] APV25 Production Testing and Quality Assurance, M.Raymond et al, Proceedings of the 8th workshop on electronics for LHC experiments, CERN-LHCC-2002-34, 219-223.
[2] Production Testing and Quality Assurance of CMS Silicon Microstrip Tracker Readout Chips, P.Barrillon et al, Proceedings of the 10th workshop on electronics for LHC experiments, CERN-LHCC-2004-030, 148-152.

Author: Dr RAYMOND, Mark (Imperial College)

Co-author: Dr FRENCH, Markus (Rutherford Appleton Laboratory)

Presenter: Dr RAYMOND, Mark (Imperial College)

Track Classification: Production, Testing, Quality Assurance and Reliability

Contribution ID: **109** Type: **Oral**

Introduction

Monday 12 September 2005 14:00 (15 minutes)

Presenter: LOCAL ORGANISERS

Session Classification: Plenary session P1

Contribution ID: **112** Type: **not specified**

Distributed power in space systems

Monday 12 September 2005 16:15 (45 minutes)

Distributed power systems offer many benefits to system designers over central power systems such as reduced weight and size. Distributed systems also allow the designers to control the quality of power at different loads and subsystems, since DC-DC converters allow close regulation of output voltage under wide variations of input voltages and loads. Distributed power systems also provide a high degree of reliability because of the isolation provided by DC/DC converters; it is very easy to isolate system failures and provide redundancy. These systems are also very flexible and easily expanded.

This talk will address the DC distributed power system of the International Space Station, which is a specific case of this kind of distributed system. It is a channelized, load following, DC network of solar arrays, batteries, power converters, switches and cables which route current to all user loads on the station.
The completed architecture consists of both the 120-V American and 28-V Russian electrical networks, which are capable of exchanging power through dedicated isolating converters.

The presence of DC/DC converters required special attention on the electrical stability of the system and in particular, the individual loads in the system. This was complicated by complex sources and undefined loads with interfaces to both sources and loads being designed in different countries (US, Russia, Japan, Canada, Europe, etc.). These issues, coupled with the program goal of limiting costs, have proven to be a significant challenge to the program.

As a result, the program used an impedance specification approach for system stability. This approach is based on the significant relationship between source and load impedances and the effect of this relationship on system stability. It is limited in its applicability by the theoretical and practical limits on component designs as presented by each system segment. Consequently, the overall approach to system stability implemented by the ISS program consists of specific hardware requirements coupled with extensive system analysis and hardware testing.

Highlights of both experimental and analytical activities will be shown, as well as some lesson learned during the development and operational phase of Modules and payloads.

Author: Prof. CICCOLELLA, Antonio (ESA-ESTEC)

Presenter: Prof. CICCOLELLA, Antonio (ESA-ESTEC)

Session Classification: Plenary session P1

Contribution ID: **113** Type: **not specified**

CMOS Technology Characterization for analog/RF application

Tuesday 13 September 2005 09:00 (45 minutes)

We discuss state of the art and new developments for the characterization of CMOS technologies.
In the first chapter the most important issues of MOS transistor modeling will be shown. Topics like AC/DC modeling, noise modeling and temperature modeling for the MOS transistor will be explained. State of the art MOS transistor models like the BSIM3 and BSIM4 models as well as the newest surface potential and charge based models will be highlighted.
This article touch on a few of the issues that are important for RF design. However the bottom line is the existence of high accurate S-Parameter measurements and frequency dependent SPICE models not only for the active devices like MOS transistor and varractors, also for passive devices like resistors, inductors and capacitors.
CMOS technologies include also additional parasitic devices like PNP bipolar transistors, which should be modeled very carefully for different analog applications like band-gap reverence circuits. And last but not least the very important topic statistical modeling including worst case corner modeling, Monte Carlo simulation, statistical boundary modeling and mismatch parameter will be discussed.

Author: Dr SEEBACHER, Ehrenfried (Austriamicrosystems)

Presenter: Dr SEEBACHER, Ehrenfried (Austriamicrosystems)

Session Classification: Plenary Session P2

Contribution ID: **114** Type: **not specified**

Electronics Packaging Development A never ending challenge

Wednesday 14 September 2005 09:00 (45 minutes)

There is an increased awareness in the semiconductor industry that packaging technology is an essential and integral part of the semiconductor product, and has become a critical competitive factor in many market segments since it affects operating frequency, power, reliability and costs.
Costs pressure over System development investments has created a strong demand in the industry for infrastructures capable to deliver increasingly better cost-performance electronic packaging solutions.
As a result of the rapidly emerging technologies and applications, the definition of exact boundaries between semiconductor, packaging and system technologies is no longer possible and all must be considered concurrently in a system-level approach to optimise the substrate design.
Organic carrier technology for semiconductors devices started to be explored in the late eighties but only in the recent years these packaging development solutions started to be massively utilized as chip carriers. The majority of these technologies originated from Printed Circuit Board manufacturing processes.
Under many technical aspects, organic laminates represent a great cost-performance opportunity but their utilization still requires a continuous "Adapting work"-ranging from design to materials - to the ever increasing requests from the semiconductor industry. This paper analyses the strategies used into organic packages to satisfy these constant new challenges in higher speed, power and I/O density applications.

Author: Mr OGGIONI, Stefano (IBM Vimercate)

Presenter: Mr OGGIONI, Stefano (IBM Vimercate)

Session Classification: Plenary session P3

Contribution ID: **116** Type: **not specified**

Microelectronic WG meeting

Tuesday 13 September 2005 17:40 (1 hour)

Presenter: MARCHIORO, Alesandro (CERN)

Session Classification: Parallel session A3

Contribution ID: **117** Type: **not specified**

Optoelectronic WG meeting

Tuesday 13 September 2005 17:40 (1 hour)

Presenter: VASEY, Francois (CERN)

Session Classification: Parallel session B3

Contribution ID: **118** Type: **not specified**

Optoelectronic WG meeting

Contribution ID: **120** Type: **not specified**

Introduction

Contribution ID: **121** Type: **not specified**

ATLAS SCT hybrid experience

Wednesday 14 September 2005 11:10 (25 minutes)

ATLAS semi-conductor tracker (SCT) has chosen the Cu-polyimide flex circuit, reinforced with a carbon-carbon substrate for its ATLAS SCT barrel modules. We report the successes, and problems encountered and solutions, during the course of production of 2,600 pieces of the hybrid.

Summary

The inner detector (ID), for tracking the charged particles in the 2-Tesla solenoidal magnetic field, of the ATLAS detector at LHC is made of 2 detecting media: silicon and gas. The latter is the transition-radiation tracker (TRT) in the outer regions. The former is further made of 2 types: the pixel for the inner region (PIXEL) and the microstrip detectors for the middle region (SCT). The detector unit of the central barrel region of the SCT is made from the so-called ATLAS SCT barrel module as shown in Figure 1. The strips run horizontally and 6 ASIC's, 128 channels each, sense the strips on the top and the bottom side of the module. The hybrid that carries the ASIC's is the ATLAS SCT barrel hybrid.

The hybrid is set in the centre region in the module such that the geometry allows clear overlapping of the adjacent modules along the strip direction, reducing the input resistance to the front-end transistor to 1/4 compared with the sensing at the end of the strips, thus reducing the input noise. The hybrid is only glued to the cooling tabs at ends and not glued to the surface of the sensors for the minimum damage to the sensors.
The hybrid for one module is made of one-piece of Cu-polyimide flex circuit, from the Input/Output (IO) connectors to the end of the circuit in the bottom side. The flex-circuit was bent 180 degrees for wrapping around the sensors from the top to the bottom side. The area of the ASIC's are reinforced with a carbon-carbon substrate for excellent thermal conductivity, strong mechanical strength, good electrical conductivity, and lightweight. The excellent thermal conductivity is required for removing the heat from the ASIC's. The strong mechanical strength is required for allowing the wire-bonding from the ASIC's to the sensors where no direct supporting underneath the ASIC's exists. The good electrical conductivity reinforces the electrical stability of the ASIC's operation, together with the intrinsic stability of the Cu-polyimide flex circuit. The lightweight means the low radiation length.
The ATLAS uses 2,112 SCT barrel modules in the experiment and required 2,600 hybrids including spares and losses. With 50 pre-series production hybrids, the final design and production readiness review (FDR/PRR) were carried out, with the results of mechanical, thermal, and electrical performances. At around the 10% of series production, the production advance review (PAR) was carried out for monitoring the quality and performance in the series production. The quality and performance of the pre-series and series production were as expected and no serious flaw or trouble was surfaced.
Whole through the production of 2,600 pieces, the Cu-polyimide flex circuit did not

encounter a major problem. The design followed the industry's design rules maximally. Neither breakage of traces nor delaminating of the layers was encountered. There were two minor problems: one was the residue of adhesives and the other was the residue of the solvent on the surface of the circuit, such that these residues weakened the sticking of the wire-bonds. The wire-bond strength was monitored continuously and the weakening of the wire-bond strength fed back to the production process and the problem was quickly removed.
The major problem appeared in a small piece in the hybrid, the so-called pitch-adapter. Since the pitches of the strips (80 microns) and ASIC's (48 microns) were different, the fanning traces were made with pure-aluminium traces on glass substrates. Up to the PAR quantity, the wire-bond strength on these pitch adapter was as expected. At about 15% production, the wire-bond strength started to decrease gradually. Reduction of the strength also associated with the generation of the "whiskers"around the wire-bond feet. The problem was traced to the quality of the aluminium metalisation and the metalisation process was improved subsequently. At around 50%, and again around 70%, of the series production, the yield of acceptable generation of whiskers was decreased. In order to solve the problem, the series production was stopped for a few months each.
A through investigation of the problem traced the source of the problem to the deep inside the aluminium metalisation process. Also the yield varied depending on the wire-bonding machines, possibly due to the shape of the wedges and the frequency and power of the ultra-sonic. The key parameter of the problem seemed to be the hardness of the metalised aluminium. The hardness was revealed to be required harder than the pure-aluminium. However, when it became too hard, it did not allow the wire-bond to stick. The hardness was identified to be a function of the temperature at metal-deposition. After identifying the mechanism and tuning the temperature to be the right range, there were no more problems till the end of the series production.

Presenter: Dr UNNO, Y. (KEK)

Session Classification: Plenary session P4

Contribution ID: **123** Type: **not specified**

CERN hybrid production

Presenter: Mr DE OLIVEIRA

Contribution ID: **124** Type: **not specified**

Round table

Contribution ID: **125** Type: **Oral**

Pixel detectors

Thursday 15 September 2005 09:00 (45 minutes)

Pixel detectors have replaced micro strip detectors as vertex trackers in the innermost part of collider detectors. Hybrid pixel detectors, in which sensor and read-out ICs are separate entities, constitute the present state of the art in the pixel technology being able to stand the extreme requirements at the LHC. A number of trends and further developments, most notably monolithic or semi-monolithic approaches are in development, targeting other tracking, but also imaging applications. The present state in pixel detector development as shown at the PIXEL2005 conference in Bonn, Sept. 2005 will be reviewed.

Author: Dr WERMES, Norbert (Physikalisches Institut)

Presenter: Dr WERMES, Norbert (Physikalisches Institut)

Session Classification: Plenary session P7

Contribution ID: **126** Type: **Oral**

How Microelectronics could benefit the next Generation of Pixel detectors at high luminosity LHC

Thursday 15 September 2005 09:45 (45 minutes)

Author: Mr HORISBERGER, Roland (PSI)

Presenter: Mr HORISBERGER, Roland (PSI)

Session Classification: Plenary session P7

Contribution ID: **128** Type: **Oral**

Implementing Artificial Neural Networks in Mixed-Mode VLSI

Friday 16 September 2005 09:00 (45 minutes)

This talk presents different VLSI models of artificial neural networks ranging from abstract ones using binary neurons to biologically inspired pulse-coupled systems. Circuit examples demonstrating common design principles for optimizing area usage and network speed are shown. The usage of digital communication protocols allows the parallelization of the analog network cores to create large-scale artificial network systems.

A key aspect of neural network research is training. Specific training algorithms for simple and complex electronic neuron models have been investigated. For binary models, evolutionary- as well as liquid-computing has proven to be successful. While these methods operate on a global level, the pulse-coupled systems use a local learning rule inspired by contemporary neuroscience called 'spike time dependent plasticity' (STDP). Therefore the VLSI system allows the investigation of important aspects of natural neural plasticity at a speed several orders faster than biological real time.

Author: Prof. SCHEMMEL, Joannes (Kirchhoff Institut fuer Physik / Electronic Vision(s))

Presenter: Prof. SCHEMMEL, Joannes (Kirchhoff Institut fuer Physik / Electronic Vision(s))

Session Classification: Plenary session P8

Contribution ID: **131** Type: **Oral**

CLOSE OUT

Friday 16 September 2005 12:20 (25 minutes)

Session Classification: Plenary session P9

Contribution ID: **132** Type: **Oral**

Commissioning the LHC machine

Monday 12 September 2005 14:15 (45 minutes)

After a brief reminder of the installation schedule and the performance goals that the LHC aims to achieve, the strategy for commissioning with protons is presented. Dedicated runs with ions and protons are mentioned, and how machine operation may be scheduled through a year is shown. Potential trouble spots during the operational cycle are then highlighted and an estimate of the resultant particle losses given.

Author: Dr BAILEY, Roger (CERN)

Presenter: Dr BAILEY, Roger (CERN)

Session Classification: Plenary session P1

Track Classification: Other

Contribution ID: **133** Type: **Oral**

Characterization and production testing of a quad 12 bit 40 Ms/sec A/D converter with automatic digital range selection for calorimetry.

Thursday 15 September 2005 15:40 (25 minutes)

The AD41240 is a custom made 12-bit 40 MSPS, quad-channel, radiation tolerant analog-to-digital converter for the front-end readout electronics of the CMS ECAL and Preshower detectors. The A/D converter features a special digital circuitry to allow automatic selection of gain ranges when it is used with a multi gain pre-amplifier. This paper describes the design architecture of the A/D converter as well as the characterization methodology that has been employed to access its performance. It presents also the production testing procedures that were carried out on a specially designed testbench capable to perform full DC and dynamic tests on packaged parts in about 10 seconds per chip. A total number of 100,000 components will need to be tested. Cumulative results are reported on yield and performance based on data acquired during the production testing of 50,000 components.

Summary

The digitization of the signals in the CMS Electromagnetic Calorimeter and in the Preshower detectors require a data converter with a demanding combination of wide dynamic range, high speed, good resolution and low power consumption. To avoid the requirements for a very high precision radiation hard ADC the approach has been to use multiple gain ranges to span the overall dynamic range, digitizing and transmitting the signals of only the highest unsaturated range. Thus a 12 bit ADC is sufficient. This approach leads clearly to a simpler system, as the range choice is performed digitally by the converter. The ADC must also be capable to withstand the extreme radiation environment of the LHC experiments. To fulfill these requirements a custom made ADC has been designed and fabricated using a commercial 0.25μm CMOS technology. In order to evaluate the production characteristics of the newly fabricated AD41240 ADC component a special characterization testbench has been developed. The testbench consists of a custom made hardware setup capable to host the device under test and apply the necessary test conditions. Software in Matlab has been developed to analyze the converted data and compute the performance characteristics. Tests were performed under many different conditions to evaluate the behavior under worst case conditions.
For the production testing of the ADCs we have chosen to develop a similar setup as the one used for the device characterization. An easy to use graphical user interface has been developed in Visual Basic in order to automatize the operation of the testbench. Extensive characterization is economically unacceptable in high volume production testing. Therefore a subset of the characterization tests has been chosen that can guarantee that no bad components are shipped. Despite the relatively short test time allocated for this job, a full sample of 512Msamples has been collected for each device and the characteristics of each chip have been extracted by computing the static parameters (INL, DNL) as weel as the dynamic parameters

(SNR, SFDR, THD and ENOB). In addition to this, a standard set of DC parameters (Idd, Vbg, Vcm) have been collected allowing to compare each device to a reference target device.
This paper describes the design architecture of the AD41240 A/D converter, introduces the characterization methodology that has been employed and presents the production test bench that has been developed and operated as well as the test procedures that have been employed.
Devices have finally been selected by applying fairly selective cuts on the distribution of static and dynamic parameters, still allowing us to pass more than 80% of the production chips into real utilization.

Author: Dr KLOUKINAS, Kostas (CERN)

Co-authors: Dr MARCHIORO, Alessandro (CERN); Mr BONACINI, Sandro (CERN)

Presenter: Dr KLOUKINAS, Kostas (CERN)

Session Classification: Parallel session A5

Track Classification: Production, Testing, Quality Assurance and Reliability

Contribution ID: **134** Type: **Oral**

The LHC Machine interface; Status - Challenges - Outlook

Monday 12 September 2005 15:00 (45 minutes)

The impact of particle losses on the operation of the LHC machine and experiments will be discussed. It will be shown how the risk of radiation induced failure to equipment can be reduced via shielding, radiation tolerant equipment designs and on-line radiation monitoring. A number of critical cases for the LHC Machine Experiments interface will be highlighted. Recent data on beam induced backgrounds and radiation at CDF (Fermilab) will be shown.

Author: Dr WIJNANDS, Thijs (CERN)

Presenter: Dr WIJNANDS, Thijs (CERN)

Session Classification: Plenary session P1

Track Classification: Radiation and Magnetic Tolerant Components and Systems

Contribution ID: **135** Type: **Oral**

CMS Tracker Hybrid Experience, a user and a manufacturer perspective

Wednesday 14 September 2005 11:35 (25 minutes)

The CMS front-end hybrid project faced in the past years several difficulties which eventually brought it to the top of the CMS list of critical path items. Instead of relating the technical challenges which had to be surmounted, this presentation will attempt to find the root causes of the encountered difficulties. A CMS user and a manufacturer's point of view will make it clear that technically challenging projects can only succeed through an early and tight relationship between customer and supplier.

Authors: Mr VASEY, Francois (CERN); Mr WYSS, Hans (CICOREL SA)

Presenters: Mr VASEY, Francois (CERN); Mr WYSS, Hans (CICOREL SA)

Session Classification: Plenary session P4

Track Classification: Assembly and Packaging

Contribution ID: **136** Type: **Oral**

CERN hybrid production experience

Wednesday 14 September 2005 12:00 (30 minutes)

The CERN TS/DEM-PMT workshop is specialised in prototype production of many types of circuits for electronic interconnection in the nuclear research field.

During this talk I will present several technologies used in industry and in our workshop, ranging from standard PCBs to MultiChip Modules Deposited (MCM-D). The explanation of the production processes will be followed by an overview of the main technical problems and the limitations related to each of these technologies.

Author: Mr DE OLIVEIRA, Rui (CERN)

Presenter: Mr DE OLIVEIRA, Rui (CERN)

Session Classification: Plenary session P4

Track Classification: Assembly and Packaging

Contribution ID: **137** Type: **Oral**

Compact Data acquisition and Power supply system designed for hostile environment condition concerning radiation and magnetic field

Thursday 15 September 2005 12:40 (25 minutes)

A compact data acquisition and power supply system housed in a water cooled special crate has been designed for the readout of the TOF (Time Of Flight) detector of the Alice experiment at CERN. The Crate contains a 12 slot VME64X bus that houses 2400 multi-hit 25ps TDC channels (TRM), a Trigger Module (LTM), a Clock Distribution Module (CPDM) and a data readout manger (DRM board) with two optical links and Ethernet. The same crate hosts the branch controlled power supply modules for the VME boards and the TOF detector front-end modules. The whole system shall be used close to the TOF detector and will work under moderate magnetic field and radiation (5 KGauss, 1.2 Gy/10 years TID). The TDC boards house TDC chips developed by CERN/ECP-MIC Division (HPTDC). Due to the radioactive environment, an accurate choice of components is required and the VME boards implement protections from Single Event Latch-up and from Single Event Upset.

Author: Mr PETRUCCI, Stefano (CAEN CAEN S.p.A., Via Vetraia 11, Viareggio, Italy)

Co-authors: MATI, A. (CAEN CAEN S.p.A., Via Vetraia 11, Viareggio); TINTORI, C. (CAEN CAEN S.p.A., Via Vetraia 11, Viareggio); SELMI, G. (CAEN CAEN S.p.A., Via Vetraia 11, Viareggio); PIERACCI, M. (CAEN CAEN S.p.A., Via Vetraia 11, Viareggio)

Presenter: Mr PETRUCCI, Stefano (CAEN CAEN S.p.A., Via Vetraia 11, Viareggio, Italy)

Session Classification: Parallel session B4

Track Classification: Radiation and Magnetic Tolerant Components and Systems

Contribution ID: **138** Type: **not specified**

Discussion

Wednesday 14 September 2005 12:30 (20 minutes)

Session Classification: Plenary session P4