Development of FTK Architecture

Fast Hardware Track Trigger for the ATLAS Detector

ATLAS

THE UNIVERSITY OF CHICAGO

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(for FTK collaboration)

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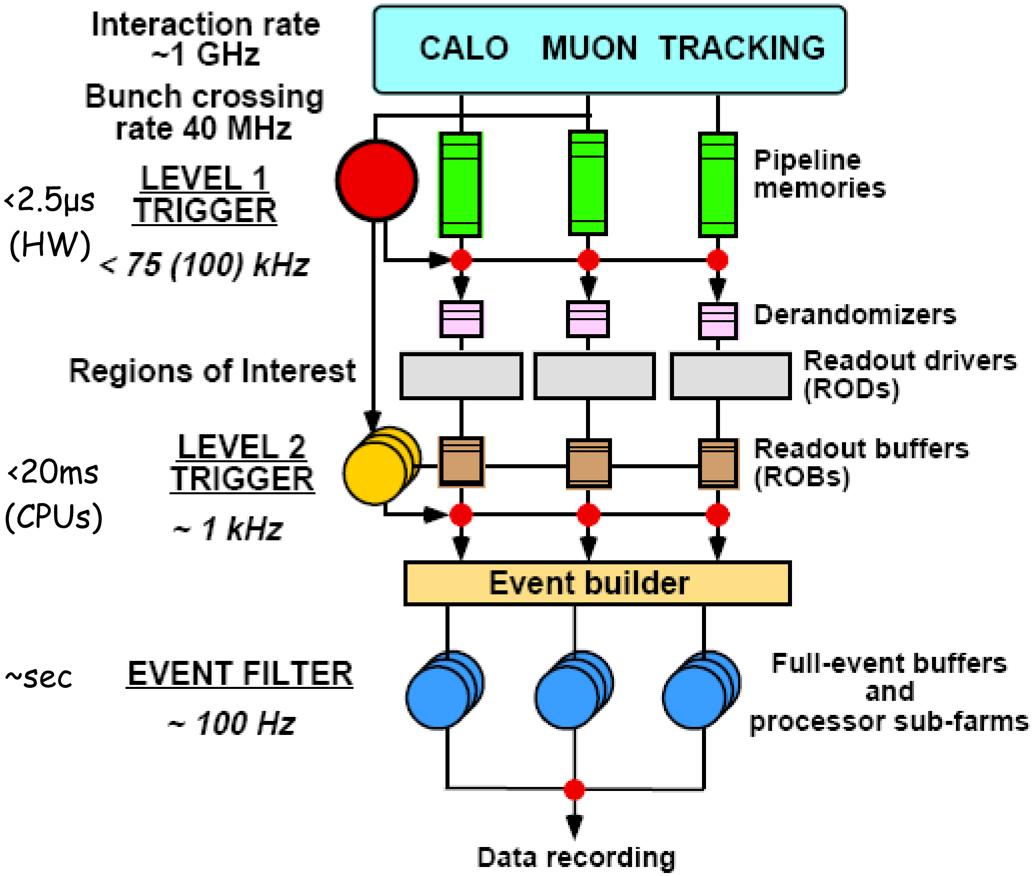
What I will cover

- Introduction
- ATLAS Tracking Detectors
- FTK Approach to Track Finding
- Hardware Considerations
- Expected Performance
- Physics Implications

Introduction I: Motivation

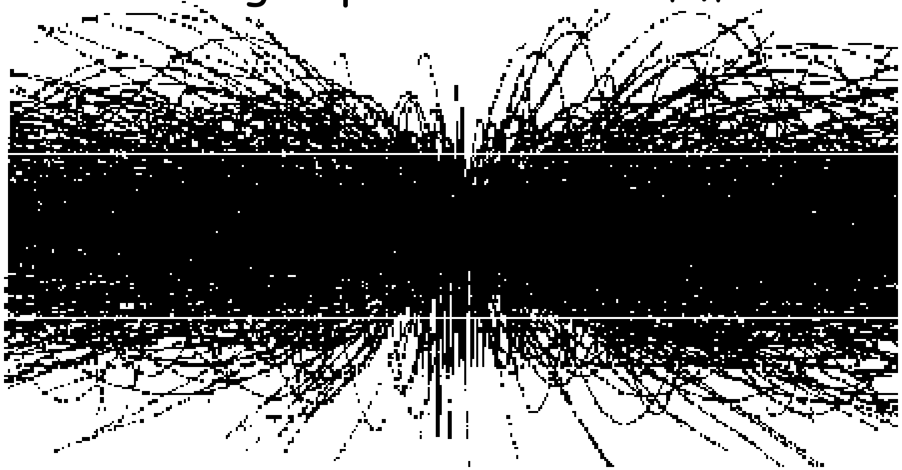


Data store bandwidth requires rate reduction of 5-6 orders of magnitude, achieved via:

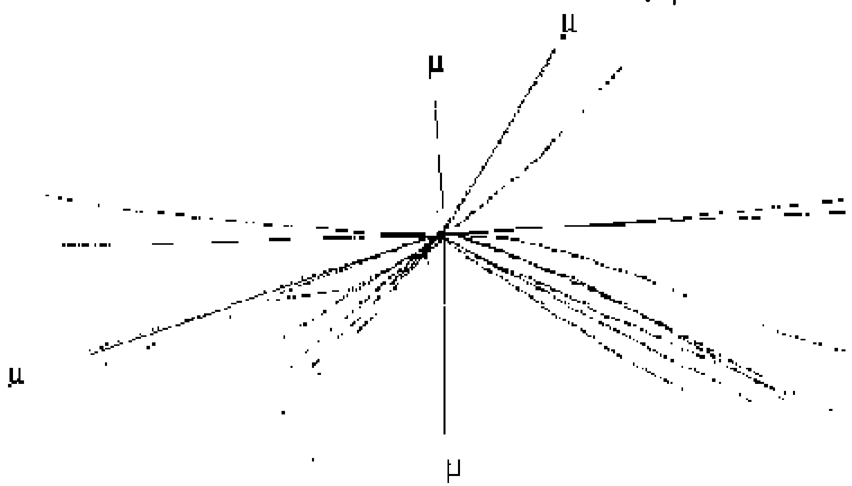
- L1: Muon, jet, EM cluster, E_t-miss thresholds
- L2: +Tracking inside Regions of Interests

30 minbias events + $H \rightarrow ZZ \rightarrow 4\mu$

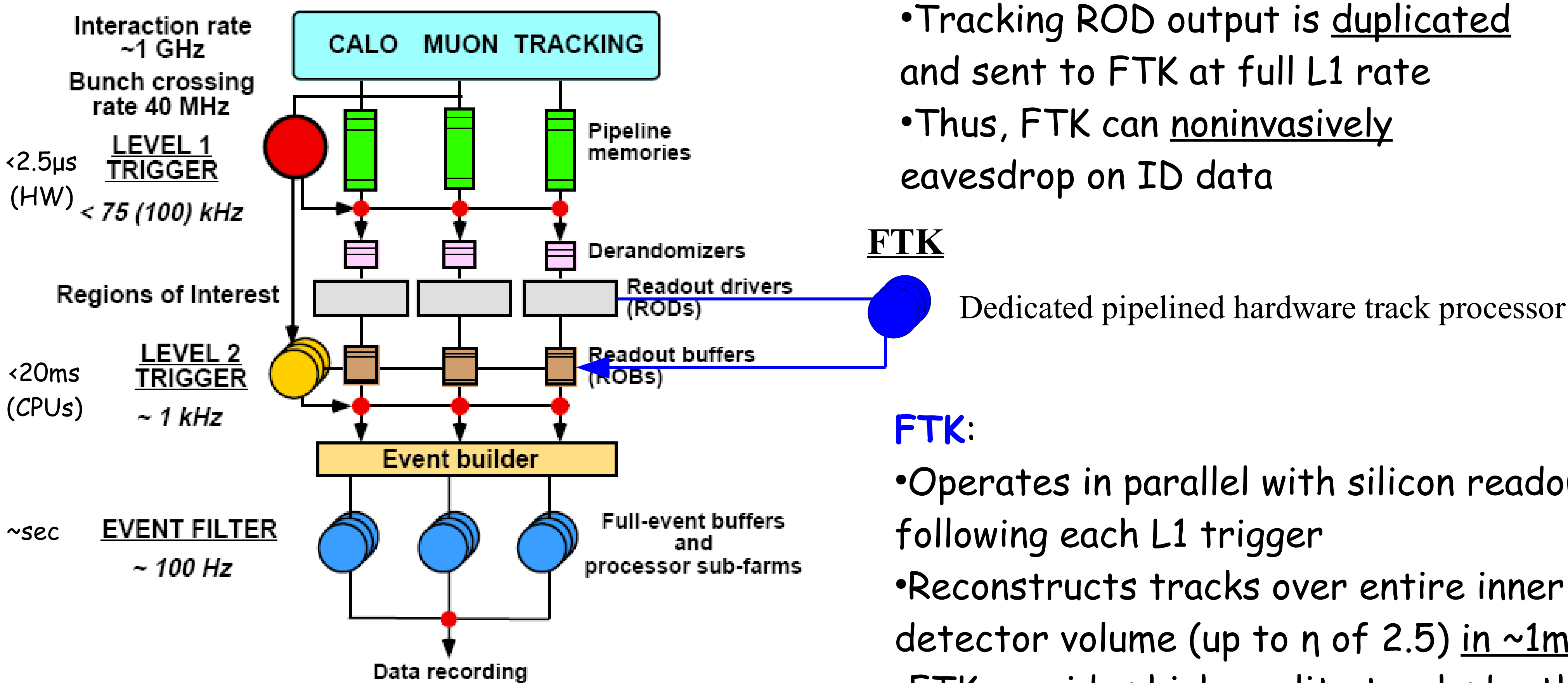
All charged particles with $|\eta| < 2.5$:



Reconstructed tracks with $p_t > 2.0$ GeV



Introduction II: Where FTK fits in



•Tracking ROD output is duplicated and sent to FTK at full L1 rate

•Thus, FTK can noninvasively eavesdrop on ID data

FTK:

•Operates in parallel with silicon readout following each L1 trigger

•Reconstructs tracks over entire inner detector volume (up to η of 2.5) in ~1ms

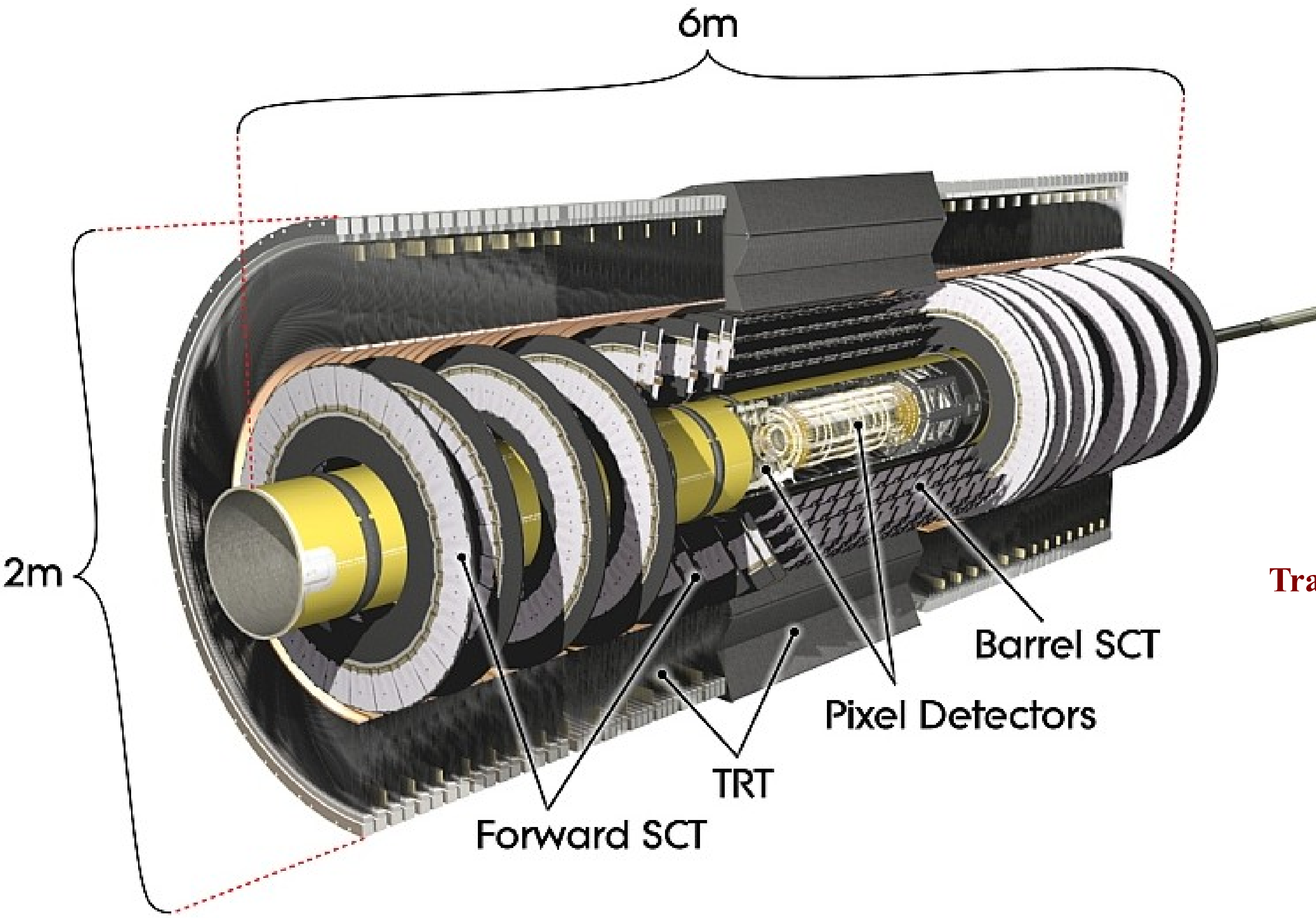
•FTK provides high-quality tracks by the beginning of L2 trigger processing

FTK provides the following benefits:

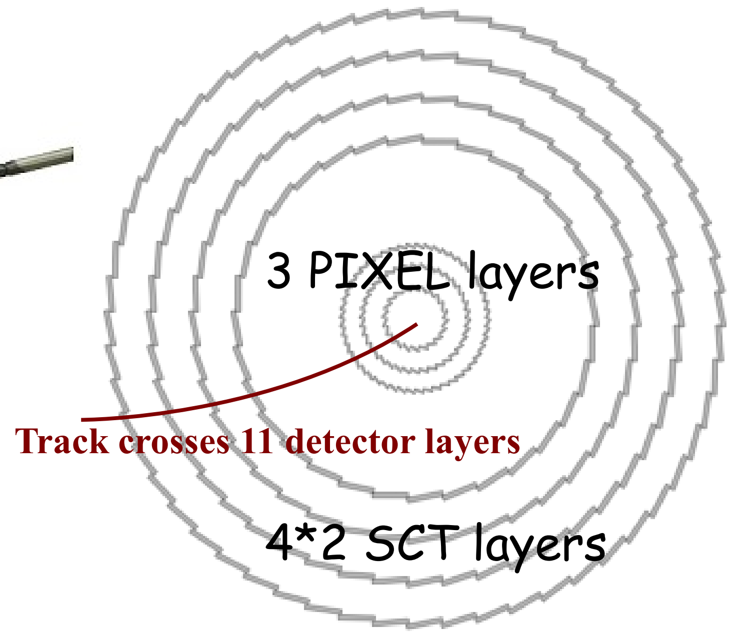
•**L1**: Lower Pt thresholds (since L2 can now reject non-interesting events more quickly)

•**L2**: Freed up from tracking. The extra CPU time is available for more advanced algorithms.

Detectors: Pixel and SCT Trackers



Example:
R-phi view of Barrel region:



Total # of readout channels:

PIXELS: 80 million

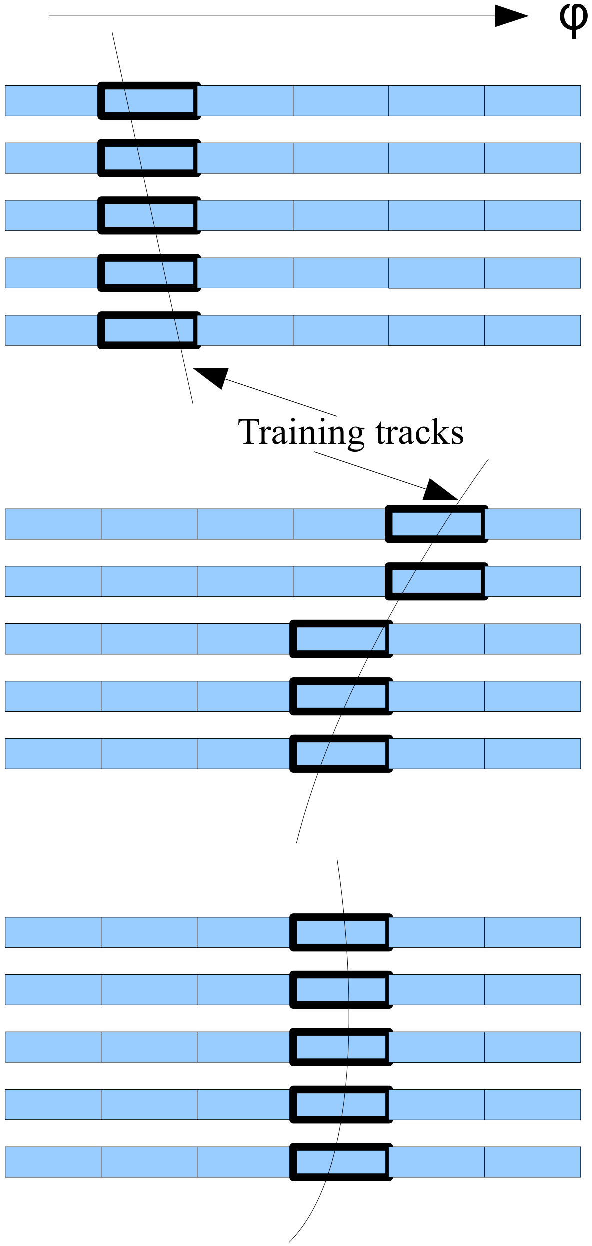
SCT: 6 million

FTK approach I: Associative Memory and Pattern Banks

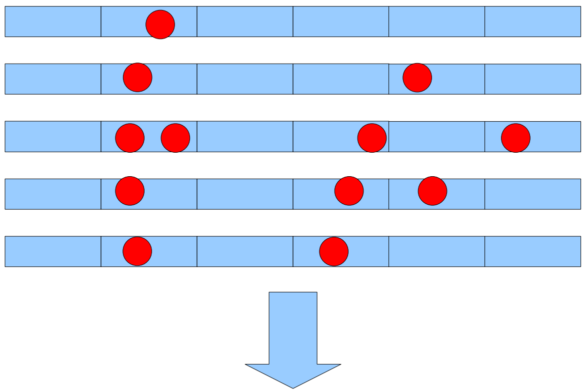
- Luminosities above 10^{34} $cm^{-2}s^{-1}$ combined with 85 million readout channels create a unique combinatorial challenge for tracking
- Even projected CPU farms won't be able to perform **global** track reconstruction within L2 time budget (~ 10 ms)
- FTK offers a viable hardware solution based on associative memories (AM):
  - A massive, ultra-fast lookup table of all **realistic** particle paths through 11 layers
  - Detector hit resolution is reduced to coarse superstrips (SS) a few mm across
  - AM bank is precalculated using MC simulation or training events – see figure:

AM bank containing 3 patterns:

(real FTK system uses 11 layers)

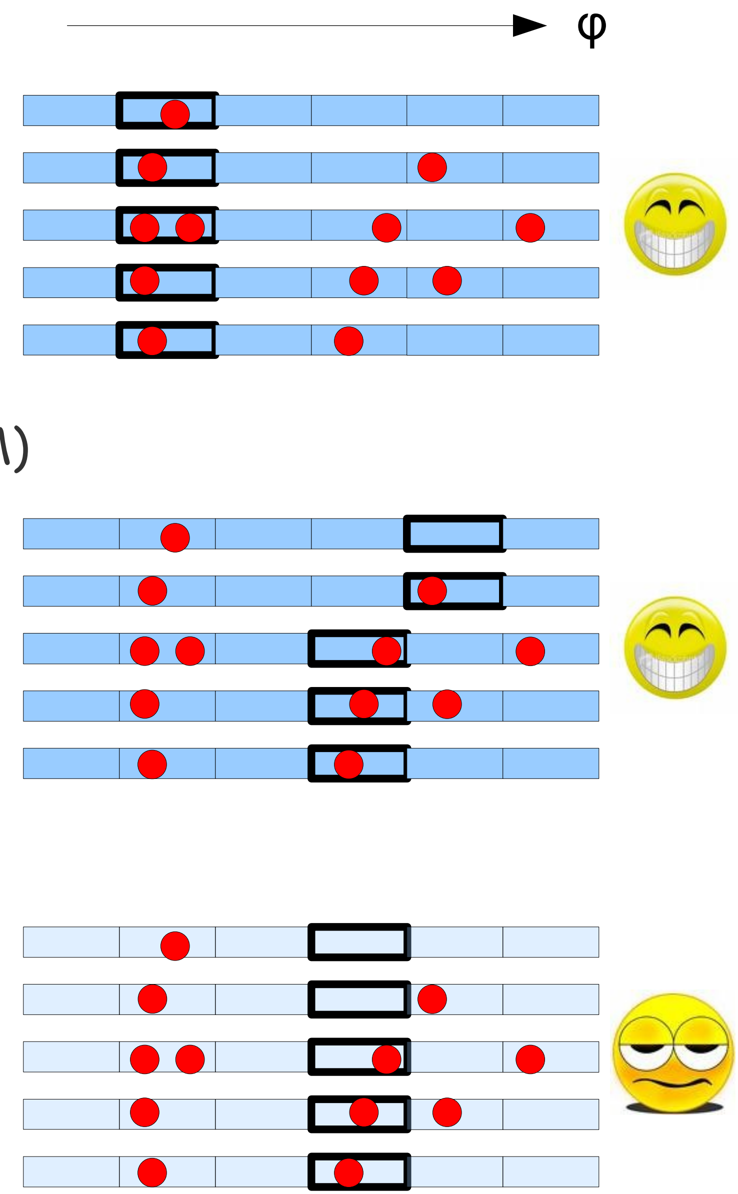


FTK approach II: Pattern recognition with AM's

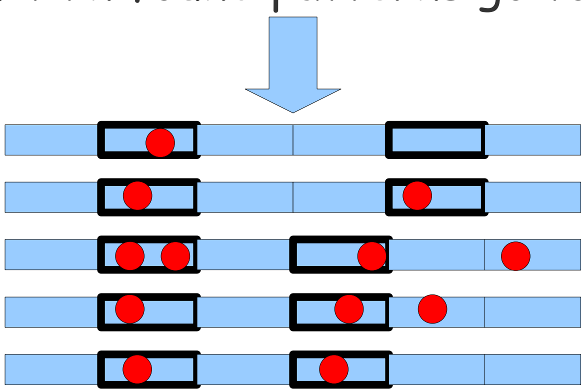


AM bank containing 3 patterns:

(real FTK system uses 11 layers)

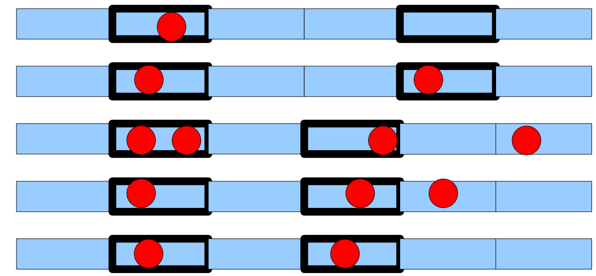


- Detector hits enter the AM board
- Simultaneously compared with all stored patterns (~100M)
  - We also allow matches with 1 missing hit
- Outputs all matched patterns
- Only hits within found patterns go to the next step



FTK approach III: From patterns to final tracks

- **5 track helix parameters** (curvature, d_0 etc) + χ^2 quality cut are computed from **full-resolution hits** within each matched pattern
- Remaining combinatorics (due to multiple hits within a superstrip) is solved by brute-force
- It is possible to group the patterns into **geometric groups** ("sectors"). Within each sector, the relationship between **hit positions** and **track parameters** is approximately **linear**
  - Linear fitting constants for each sector can be precomputed from training data
  - All detector effects (eg, misalignments) are automatically taken into account
  - Scalar products can be done quickly (**1 fit/ns**) using DSP units in modern commercial FPGA's

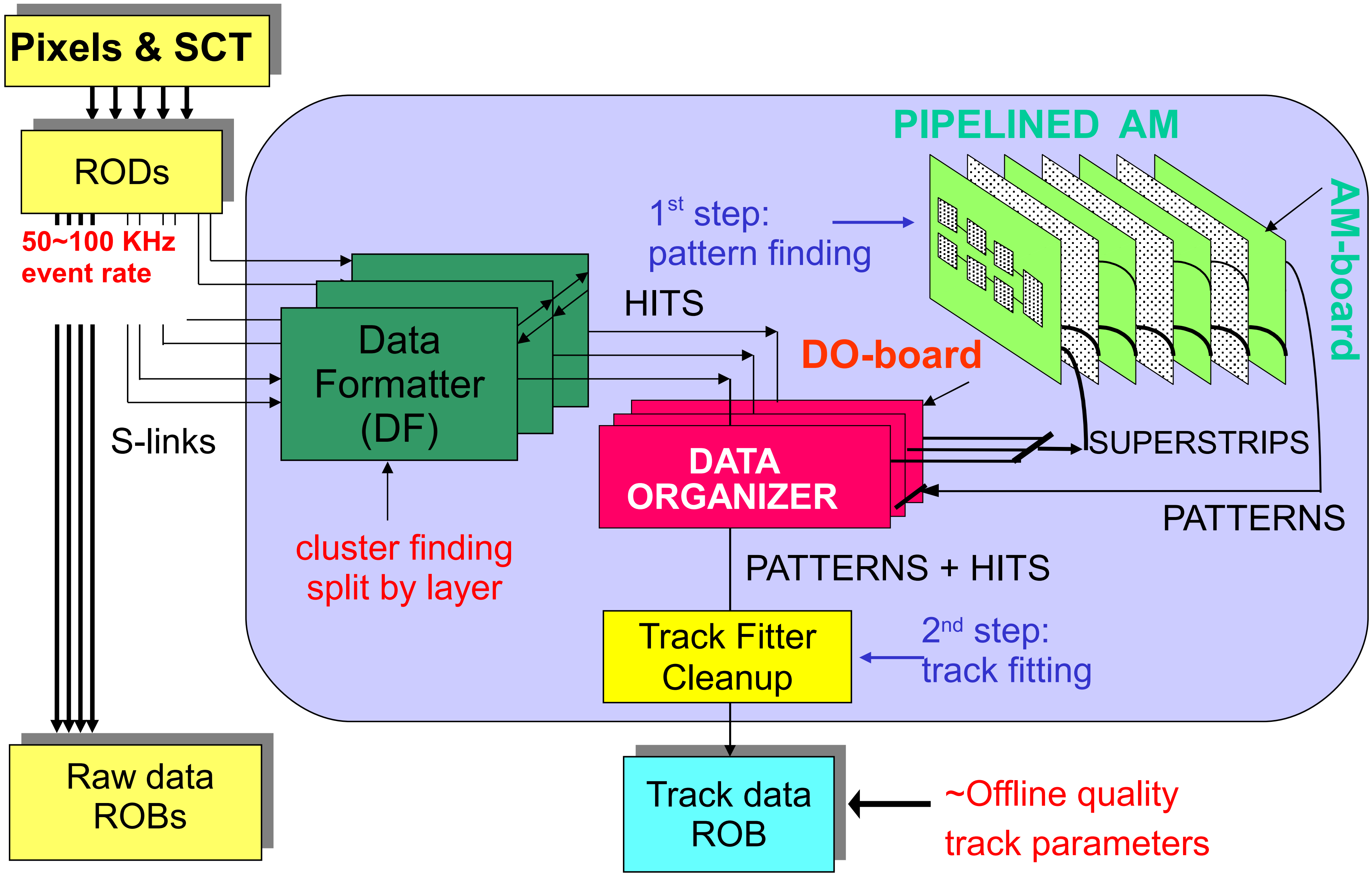


2 fits + 1 fit

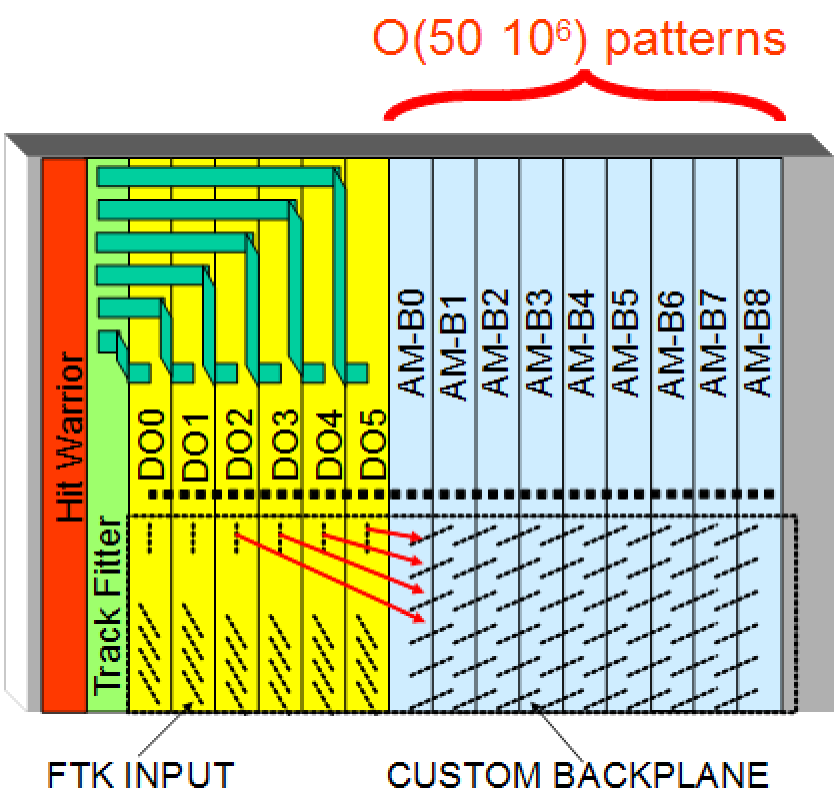
track parameters — *hit coordinates* — *constants*

$$p_i = \sum_j c_{ij} \cdot x_j + q_i$$

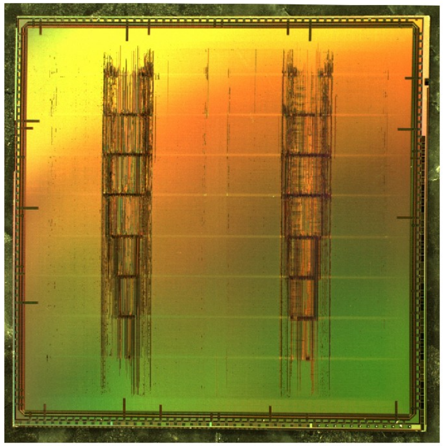
Hardware I: Overview of the System



Hardware II: Crate Structure and AM chip



Current AM chip used at CDF:
0.18 um custom cells with 2500 patterns/chip
IEEE Trans.Nucl. Vol. 53 Pages: 2428-2433

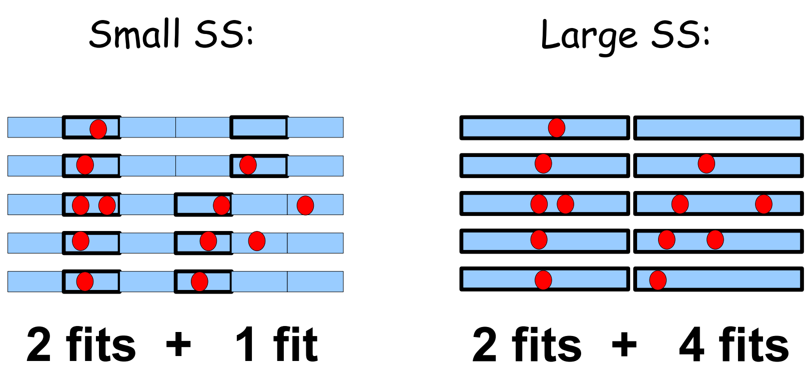


- 8 crates covering different φ regions
- Patterns are split into several boards
- Track fitter board based on CDF design
- Duplicates cleaned up in HW board

- Using standard cells with 90 nm technology → 10k patterns / chip
- If more capacity is needed, we will consider 65 nm technology

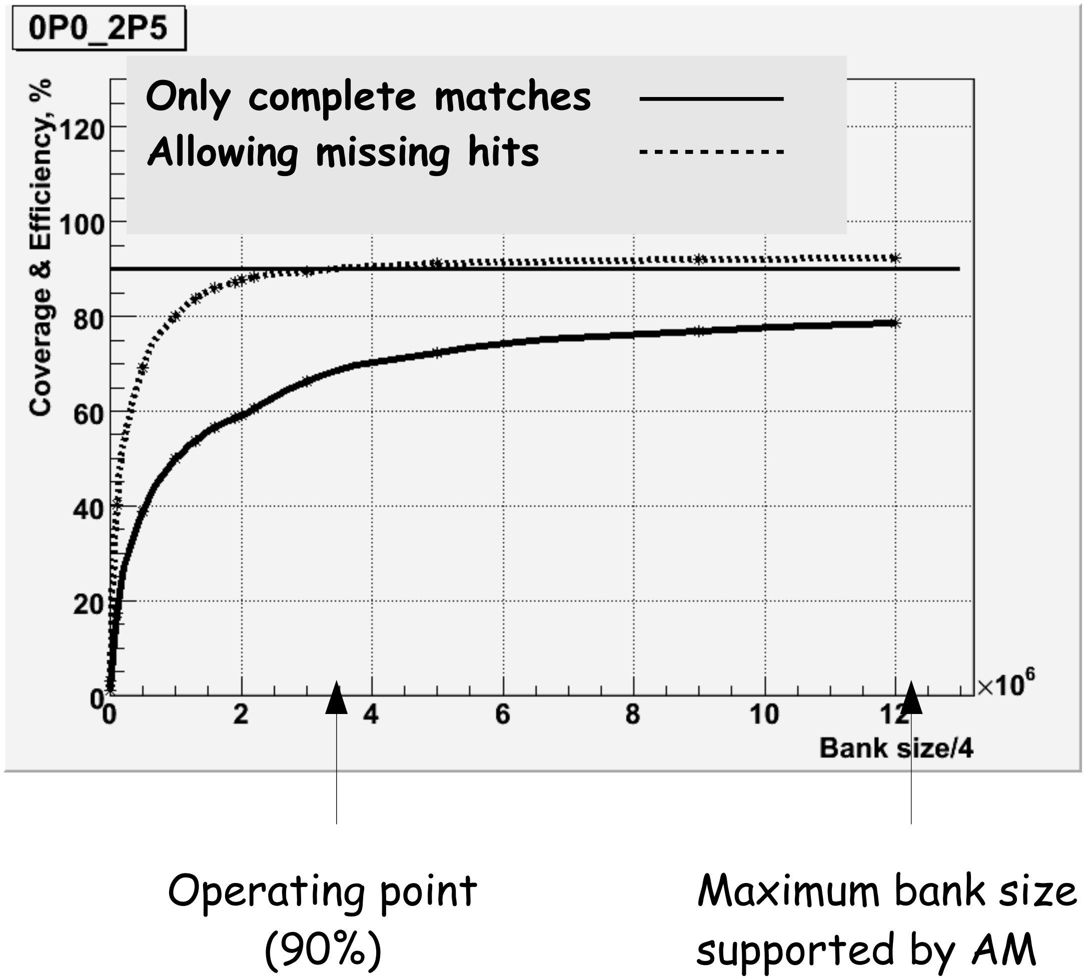
Performance I: Pattern Bank Size and Efficiency

- Pattern bank size strongly depends on superstrip size. It is a balancing act: **coarser superstrips** = fewer patterns, but many more fits:



- If we allow 10/11 pattern matches (when a hit is missing in one layer), efficiency raises much more quickly

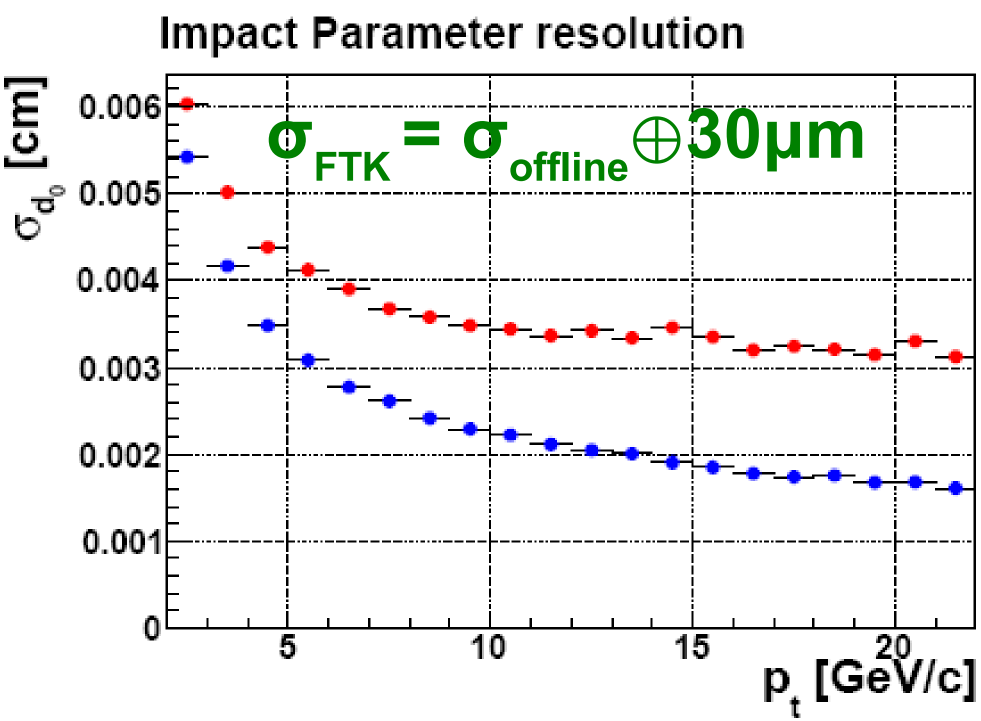
Pattern bank efficiency vs bank size
(all muon tracks with p_t>1GeV)
Pixel SS = 3 mm, SCT SS = 5 mm

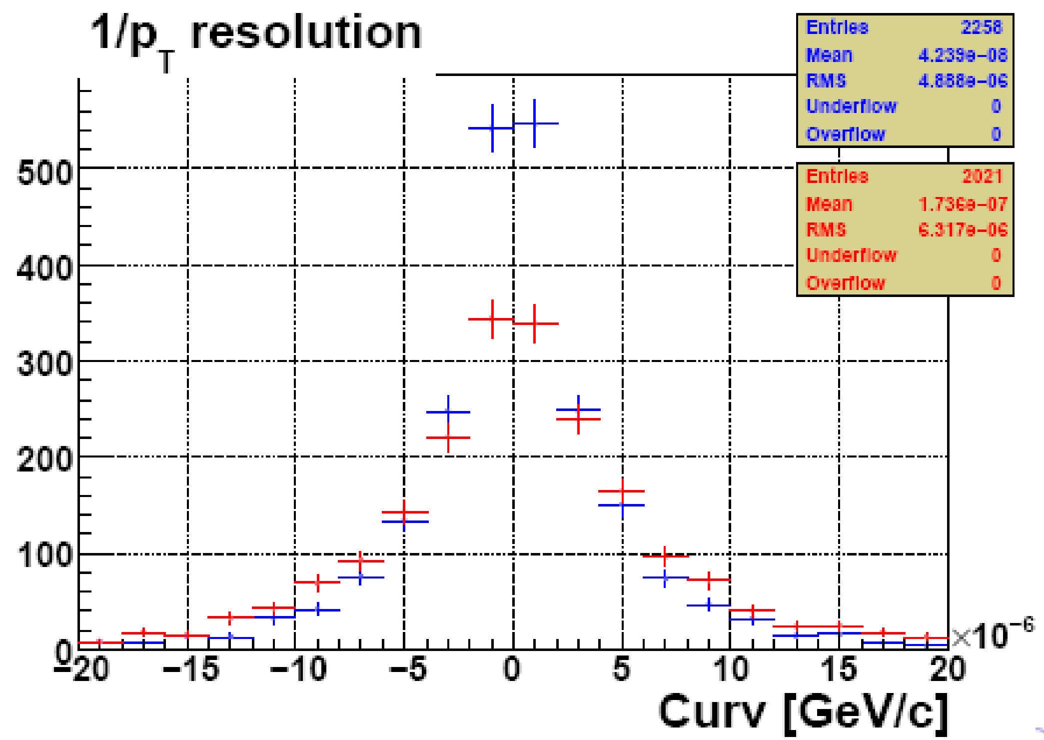


Performance II: Single Muon Events

- We compare FTK-reconstructed tracks with an offline algorithm (IPAT):
  - Resolutions are wrt all truth tracks with $p_t > 1$ GeV and $|\eta| < 2.5$
  - Performances are comparable

Parameter	$\sigma(FTK)$	$\sigma(OFF)$
$1/(2p_T)$ [c/GeV]	$7.4 \cdot 10^{-3}$	$6.6 \cdot 10^{-3}$
ϕ [rad]	$9.5 \cdot 10^{-4}$	$6.3 \cdot 10^{-4}$
d_0 [cm]	$5.3 \cdot 10^{-3}$	$3.3 \cdot 10^{-3}$
$\cot(\theta)$	$2.0 \cdot 10^{-3}$	$1.4 \cdot 10^{-3}$
z_0 [mm]	$2.1 \cdot 10^{-2}$	$1.9 \cdot 10^{-2}$

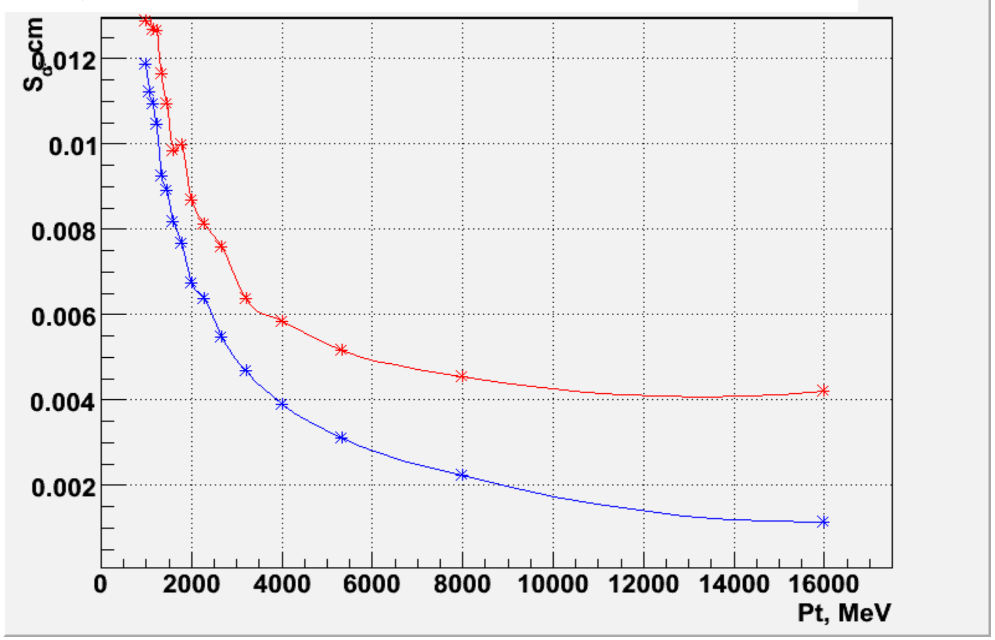




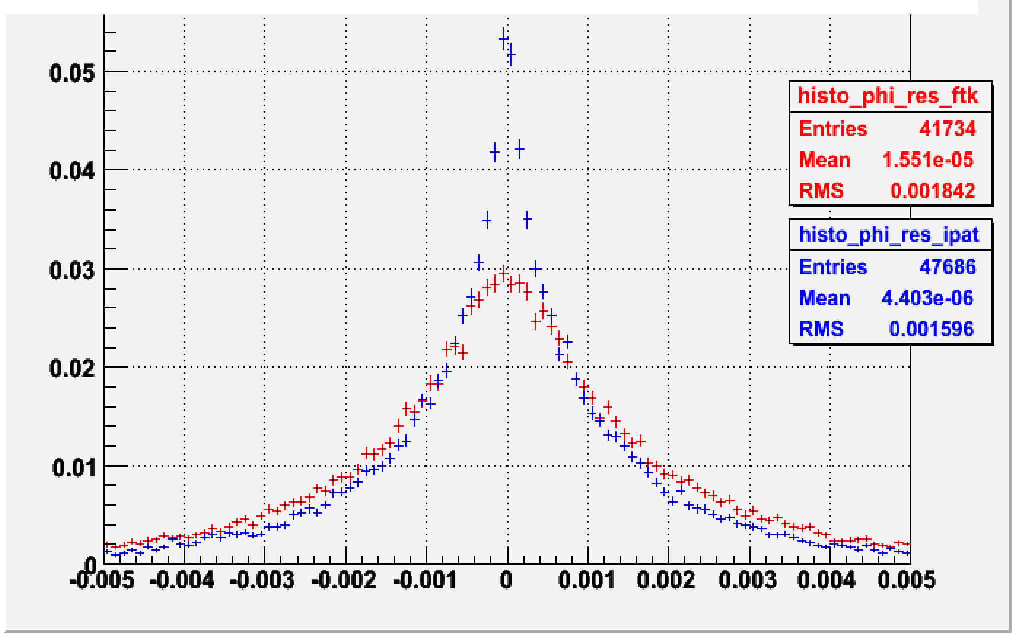
Performance III: WH→bbX @ 10^{34} cm^{-2} s^{-1} events

- FTK and IPAT resolutions are again similar
- Our current timing estimate is about 1 ms for a complex event
- At higher luminosities with their large inner detector occupancy, the # of fits could become excessively large. This can be dramatically reduced by narrowing the superstrip width and modifying the pattern recognition and fit strategy. Studies are underway to find the optimal strategy.

Impact Parameter Resolution, cm

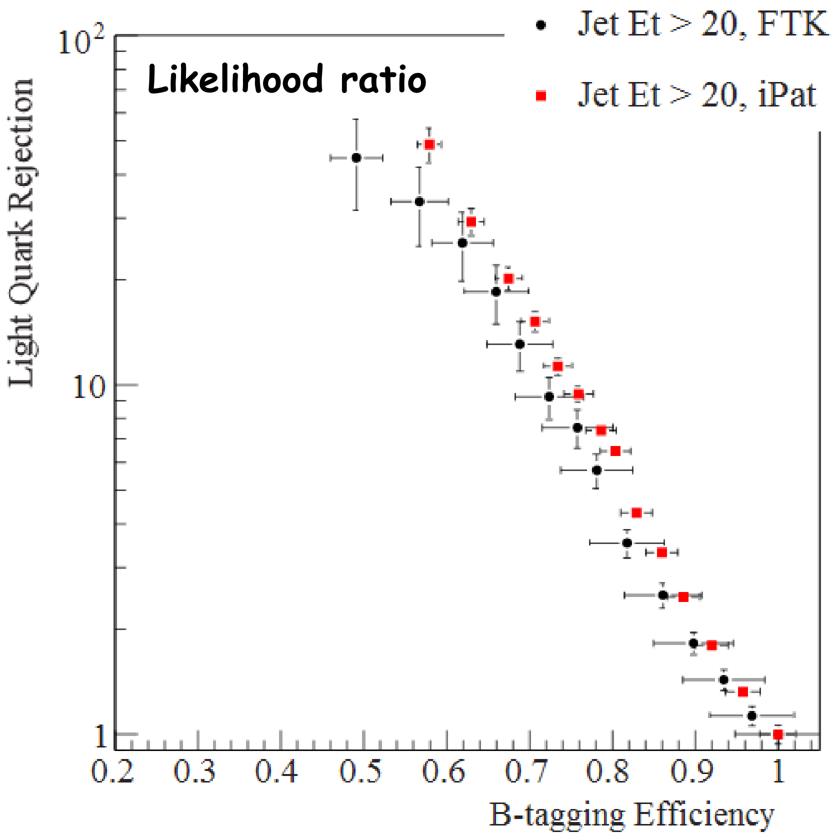


Phi resolution (all p_t)



Physics Implications (Preliminary)

- b-jets
  - Offline-quality b-tagging efficiency and light quark rejection can be achieved by using the savings in tracking time to apply more sophisticated b-tagging algorithms at Level-2.
  - Expanded physics reach for channels with b-quarks in the final state (eg, bbH/A → bbbb)
- electrons and muons
  - Isolation using tracks from the hard scatter vertex can reduce the dependence of lepton efficiency on luminosity
- taus
  - Identification based on an isolation region devoid of tracks surrounding a small cone containing no more than 3 tracks



Summary

- FTK performs global track reconstruction at Level-1 trigger rate
- Using massively parallel Associative Memories, FTK will provide a complete list of 3D tracks at the beginning of Level-2 processing
- Time saved by FTK can be used in Level-2 for more advanced algorithms
  - Bonus: access to tracks outside the Regions of Interest
- FTK easily integrates with current ATLAS DAQ
- Builds on success of Silicon Vertex Trigger (SVT) at CDF

Project timeline:

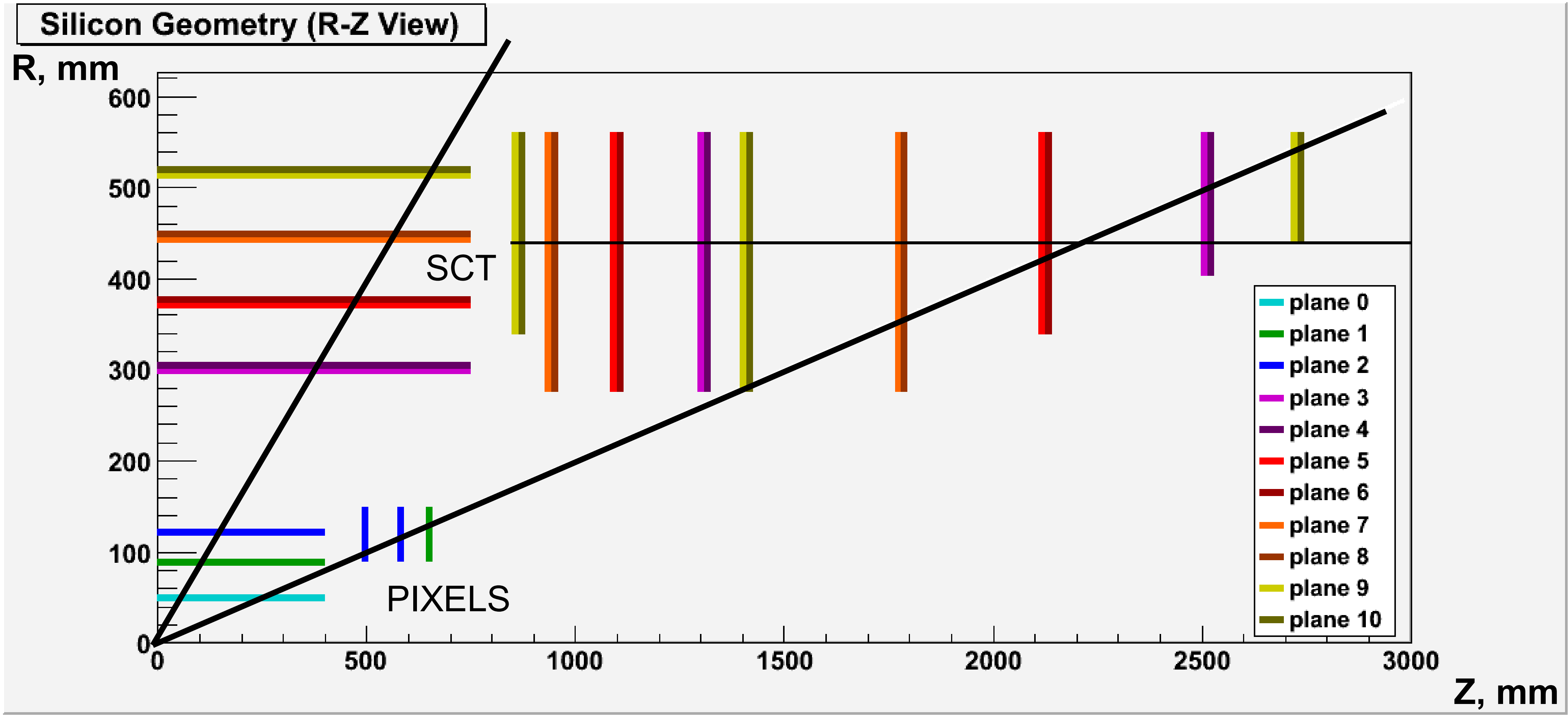
- TDR in the fall 2009
- First board prototypes in 2010
- Completion of the system prior to LHC Phase I shutdown

Backup slides

THANK YOU

Additional information about FTK:
http://www.pi.infn.it/~orso/ftk/

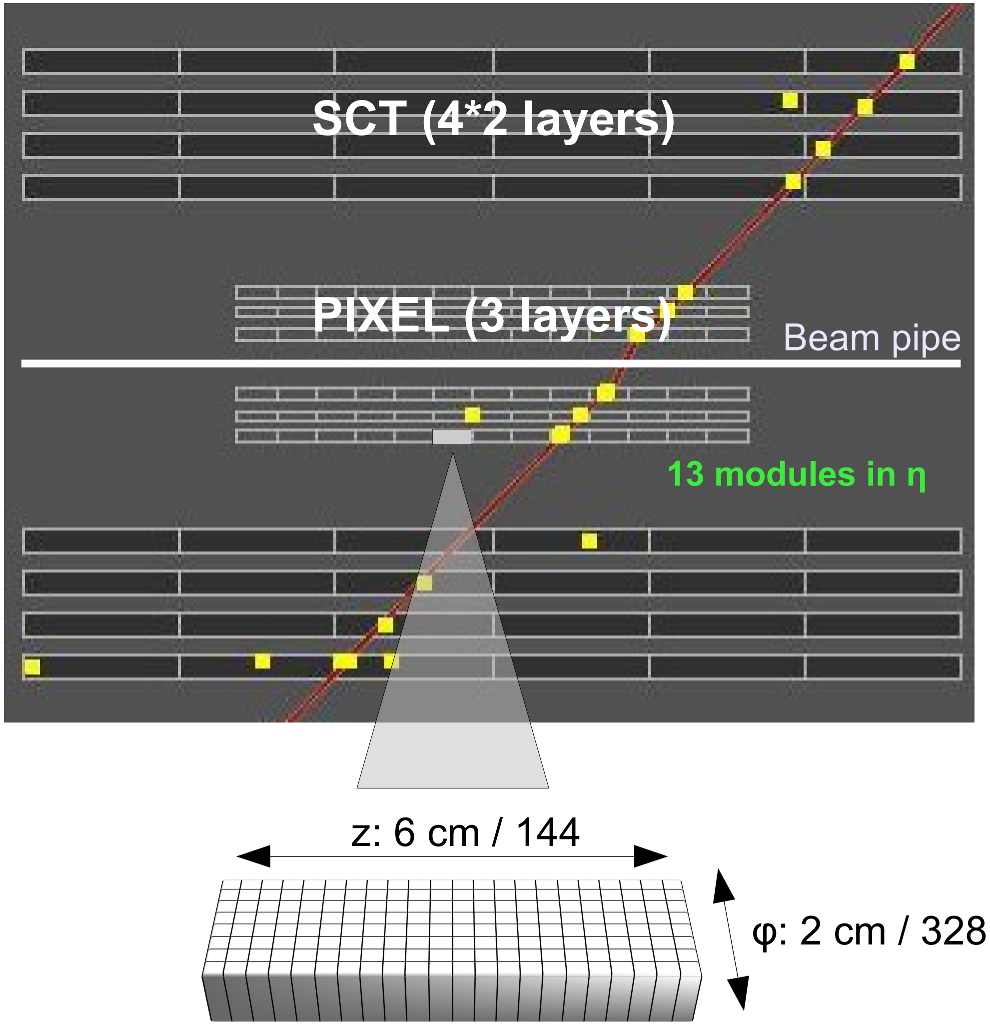
Detectors: 11 tracking layers



- SCT and PIXEL disks are assigned into one of 11 logical layers
- Assignment aims to reduce overlaps and (almost) eliminate gaps
- These 11 layers are used to do <u>pattern recognition</u>

Silicon Tracker geometry (central barrel)

r-z view:



r-φ view: